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FPGA Implementation of Adaptive Absolute SCORE Algorithm for Cognitive Radio Spectrum Sensing with WTM and LFA

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Abstract: Cognitive Radio (CR) is generally a wireless communication system that has the ability to improve the network's system-capacity. Since, the white space or temporally unused spectrum are used to enhance the system-capacity and the important operation involved in the cognition cycle is spectrum sensing. This spectrum sensing supports the Cognitive Radio users to adjust with the environment by identifying the white/vacant spaces without creating any interference to the primary user communication. The traditional filters such as Finite Impulse Response (FIR) filters and median filters used in the spectrum sensing obtains high area utilization in Cognitive Radio. In order to overcome this, an Adaptive Absolute SCORE (AAS) technique is developed based on the FIR for improving the sensing function and radio sensitivity. The area and frequency of the AAS are enhanced by using the Wallace tree multiplier (WTM) and Ladner-Fischer Adder (LFA) in the design of the FIR. The proposed architecture used for the spectrum sensing is named as AAS-WTM-LFA. This AAS-WTM-LFA architecture is developed in the Xilinx tool for different Virtex devices. The performance of AAS-WTM-LFA is analyzed in terms of LUT, slices, flip flops, bonded Input and Output Block (IOB), frequency and power. Additionally, the quality of signal processed through the AAS-WTM-LFA architecture is analyzed as Bit Error Rate (BER) and False Acceptance Rate (FAR). Additionally, the AAS-WTM-LFA architecture is compared with ACS, AAS, AAS-CSLA, AAS-R8-CSA and AAS-R8-CSLA. The number of LUT for AAS-WTM-LFA architecture is 247 for Spartan 6 device, that is less when compared to the remaining architectures.

Keywords: Adaptive absolute score, Cognitive radio, Finite impulse response filter, Ladner fischer adder, Spectrum sensing, Wallace tree multiplier.

1. Introduction

Cognitive Radio (CR) is an intelligent adaptive communication system environment which provides an effective communication with an appropriate combination of radio spectrum [1]. The CR is utilized in various standards of wireless communication such as WiMAX, WiFi, Zigbee and long-term evolution [2]. If Primary User (PU) is inactive, the PU's licensed spectrum is used by the Secondary User (SU) for improving the spectrum efficiency of CR. The major operations processed by the CR are spectrum sensing and adaption [3, 4]. The interference threshold that is tolerated by the PU is doesn't exceeded by the SU for protecting the PU's licensed right. The spectrum opportunities are detected by the SU and other band is accessed for enhancing the utilization of potential spectrum and quality of service [5]. Besides, the spectrum sensing is the task of achieving the information about spectrum usage and presence of PUs in geographical area [6]. In low Signal-to-Noise Ratio (SNR), a vacant spectrum bands are effectively detected by using spectrum sensing in CR. Subsequently, the radio operating parameters are adopted with related to the spectrum bands [7].

Additionally, the CR detects the signals in a multiple/wide frequency bands or single/narrow

frequency band [8]. The FPGAs are generally used to develop the signal processing algorithm in hardware. In each CR unit, the FPGA is used to develop hardware of spectrum sensing. The implementation of spectrum sensing using FPGA has various advantages such as reconfigurable features, achievement of high speed operation due to parallelism and less power consumption [9]. The building blocks are connected by the cross bar corrections in FPGA. Moreover, the FPGA has pipelining and higher parallelism than the digital signal processing [10]. The general challenges faced by the spectrum sensing in cognitive radio, which are given as follows: The sensing of single radio is affected by the hidden terminal problem and the detection performance of spectrum sensing is affected by the shadowing and fading effects [11]. The throughput is decreased and the high probability of sensing busy is caused when the SU randomly chooses the channels for sensing purpose. The lesser throughput of SU creates the negative effects on the CR performance such as higher transmission time and high energy consumption [12]. Some of the FPGA based spectrum sensing techniques in CR are given as follows: maximum-minimum-eigenvalue (MME)-based spectrum sensing [13], selective-sampling technique [14] and spectrum sensing based on the autocorrelation of the received samples [15]. Moreover, this research considers the SCORE algorithm to improve the spectrum sensing of CR. The common types of SCORE algorithms are least square SCORE [16] and cross SCORE algorithm [17]. The main contributions of this paper are given as follows:

- AAS algorithm is used in this research instead of using least square SCORE and cross SCORE algorithm. The sensing capacity of the algorithm is improved and the hardware utilization of the architecture is reduced by utilizing the smaller number of logical elements in LFA and WTM of AAS.
- The efficiency of the FIR filter is improved by integrating the WTM and LFA in the filter design. The WTM and LFA are used in the FIR deign due to its minimum logical area and executing the carry propagation in parallel manner. Since the FIR filter is stable and the implementation of FIR filter is easy than the other filter.
- This AAS-WTM-LFA design is used to achieve higher frequency in CR. This leads to reduce the processing time of the input that is processed through the CR.

The overall organization of the paper is given as follows: The literature survey of the existing researches related to the spectrum sensing in the CR is given in section 2. The proposed AAS-WTM-LFA architecture used for the spectrum sensing in CR is clearly explained in the section 3. The performance analysis of AAS-WTM-LFA architecture for various Virtex devices are given in section 4. Finally, the conclusion is made in section 5.

2. Literature survey

C.S. Karthikeyan and M. Suganthi [18] presented the adaptive self-coherent-restoral (SCORE) based spectrum sensing method for CR. Initially, the desired signal is achieved by using the Adaptive Absolute-SCORE (AAS) algorithm. The extracted signal's spectrum is analyzed to identify whether the signal channel is hooked by a vacant or PU or a SU. The signal and noise are effectively differentiated by implementing this CR in FPGA. An entire vacant channel with low cost function is precisely identified by updating and reconfiguring the algorithm. This adaptive SCORE algorithm gives better performance in highly noisy environment and it gives higher sensing accuracy with less implementation complexity. This work did not implement in the parallel form to achieve higher speed.

A. Martian [19] presented the USRP (Universal Software Radio Platform) SDR (Software defined radio) platforms to develop a process of real-time spectrum sensing in CR. The spectrum sensing process is performed by capturing the RF signal by using USRP platforms. Here, two different USRP platforms are used such as networked series (USRP N210) and X series (USRP X310). The spectral occupancy degree is calculated from the received data stream by using the energy detection spectrum sensing method in real-time spectrum sensor. The signal leakage effects and selection of an adequate decimation rate are used to achieve an accurate sensing information. However, the spread sensing is affected due to the unwanted parasite components created by the direct conversion architecture.

M.S. Murty and R. Shrestha [20] developed the spectrum sensing in CR by using the time domain cyclostationary-feature detector (TCD). This TCD is a reconfigurable and hardware-efficient VLSI architecture. The overall range of subcarrier is supported by the autocorrelator which is incorporated in TCD. Since, the orthogonal frequency division multiplexing uses the subcarriers range. The accuracy of coordinate rotation digital

computer (CORDIC) architecture of TCD is improved by using the overflow/underflow protection. The developed CORDIC architecture has higher hardware utilization compared to the conventional CORDIC architecture.

M. Khayyeri and K. Mohammadi [21] presented the real-valued sparse spread spectrum sensing algorithm in CR, that is named as CR4S. This CR4S algorithm is depends on the sub-sampling solution that utilizes the RF signal's real-valued properties and sparsity of the frequency spectrum for identifying the free bandwidths with lesser computations. In CR, the spectrum sensing is enhanced by using the Fast Fourier Transform (FFT), real-valued FFT, and collaborative spectrum sensing technique. Additionally, the SFFT approach is utilized for changing the time-domain signal to the frequency domain because of the sparsity of the frequency spectrum. This SFFT effectively minimizes the amount of calculations required for FFT calculation. This CR4S obtains only less throughput and operating frequency during the spectrum sensing process.

S. Nareshkumar and K. Bikshalu [22] introduced an Adaptive Absolute SCORE (AA-SCORE) architecture for improving the spectrum utilization efficiency. This AA-SCORE (AAS) architecture is designed based on the FIR filter to reduce the system complexity. The Radix-8 and Carry Select Adder (CSLA) are used for FIR filter design to minimize filter complexity. This AA-SCORE based spectrum sensing in CR is called as AAS-R8-CSLA architecture. In CR, the spectrum sensing performance of the AAS-R8-CSLA is better when compared to the conventional SCORE processor. The CSLA used in the AAS-R8-CSLA consumes more area, due to the utilization of the sum and carry operation in spectrum sensing.

The existing spectrum sensing techniques faces various issues like speed and higher hardware utilization. In this study, the integration of WTM and LFA into the FIR are used to improve the frequency and area. Additionally, the LFA used in the AAS achieves higher speed, due to its parallel computation.

3. Proposed architecture

In this proposed architecture, a FIR based AAS is designed to improve the spectrum sensing of CR. This proposed architecture has 6 major functional blocks such as data generator, modulator, channel, AAS block, demodulator and data checker. The data generated by the data generator are given to the modulation block. In this study, 100 ones are generated in the MATLAB to analyse the spectrum sensing performance. There are three different modulation schemes are used in this architecture such as (BPSK), Quadrature Phase Shift Keying (QPSK) and Quadrature Amplitude Modulation (QAM). Since, the channel used for the CR is Additive White Gaussian Noise (AWGN). Then the AAS-WTM-LFA based spectrum sensing receives the inputs from the channel. Subsequently, the output samples are directly imported from MATLAB to Xilinx Register Transfer Level (RTL) compiler. The block diagram of the AAS-WTM-LFA architecture is shown in the following Fig. 1.

3.1 Adaptive Absolute SCORE architecture

In this AAS architecture, the cross SCORE technique is considered as property restoral technique that is an extended version of least squares SCORE technique. A real property restoral technique is designed by using the numeral innate standpoints. Since, the design of real property restoral method depends on the spectral self-coherence which is obtained by improving the spectral self-coherence in output. The design of AAS architecture are effectively detects the very weak PU signals. This AAS is significantly fast architecture with ease of implementation.

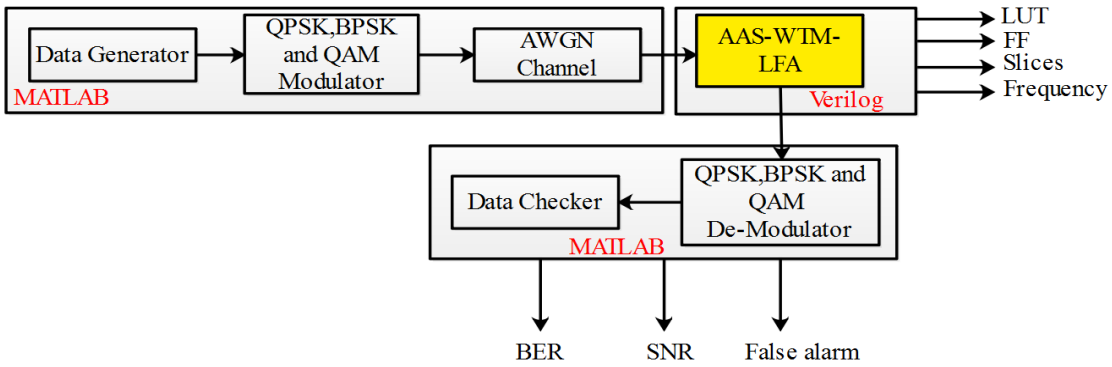

Figure. 1 Block diagram of the AAS-WTM-LFA architecture

Consider, the antenna array is disturbed by the signal of interest and by the interferences. Eq. (1) is used to modulate the received signal vector and the calculation of reference signal is given in Eq. (2).

$$x(t) = as(t) + i(t) \tag{1}$$

$$r(t) = \left[w^{(*)}\right]^{H} u(t) \tag{2}$$

The $u(t)$ specified in Eq. (2) is calculated by using the Eq. (3) and the objective function of the AAS-WTM-LFA architecture is shown in Eq. (4).

$$u(t) = x^{(*)}(t-\tau)e^{j2\pi\alpha t} \tag{3}$$

$$\hat{F}_{sc}(w) \triangleq \left|\hat{\rho}^{\alpha}_{yy^{(*)}}\right|(\tau) \tag{4}$$

Generally, the highest solution of the conjugate objective function is equal to the highest solution of the Adaptive Cross-SCORE (AC-SCORE) objective function. Specifically, the $\left|\hat{\rho}^{\alpha}_{yy^{(*)}}\right|(\tau)$ is maximized, when the w is identical to the dominant mode.

$$\lambda \hat{R}_{xx} w = \hat{R}_{xu}\hat{R}^{-1}_{uu}\hat{R}_{ux}W \tag{5}$$

Where, the $R_{xu} = R^{T}_{xu}$ while the AAS-WTM-LFA architecture is executed in the symmetric condition. Eq. (6) and (7) shows the adaptation done in the AAS structure.

$$R^{T}_{xu} = 0.5(R_{xu} + R_{ux}) \tag{6}$$

$$R_{xx} = 0.5(R_{xx} + R^{T}_{xx}) \tag{7}$$

A simple adjustment to Eigen equation converts the AC-SCORE processor into AAS conjugate, when the symmetric condition is doesn't present in the AAS-WTM-LFA architecture. The cost function is specified in the following Eq. (8).

$$F_{SC} = \frac{|w^{H}\hat{R}_{xu}w^{(*)}|}{\sqrt{[w^{H}\hat{R}_{xx}w][w^{H}\hat{R}_{uu}w]}} \tag{8}$$

Where, the input signal's autocorrelation is represented as R_{xx}; the correlation of reference signal loss among the input signal and reference signal is represented as R_{xu} and the delayed version of input signal is specified as $u(t)$. The flow diagram of the AAS-WTM-LFA architecture is illustrated in Fig. 2.

The AAS utilized in the AAS-WTM-LFA architecture is designed by using the WTM and LFA.

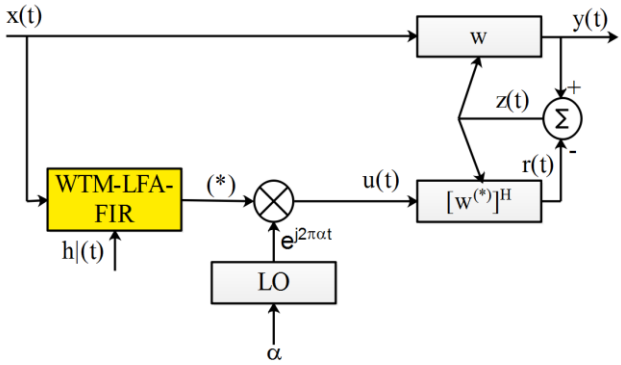

Figure. 2 Flow diagram of AAS-WTM-LFA architecture

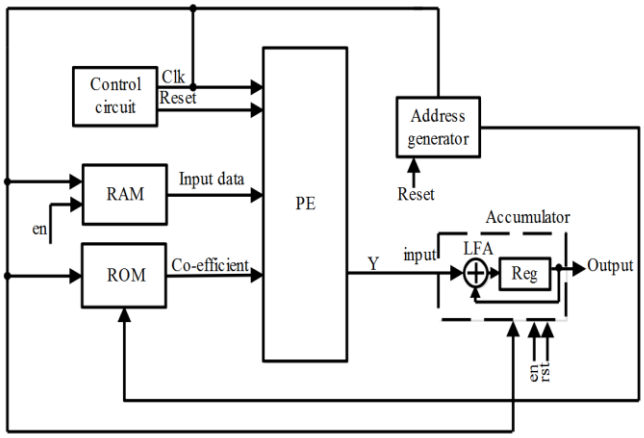

Figure. 3 Architecture of AAS-WTM-LFA

The Verilog is used for designing the FIR filter by using the WTM and LFA. The complexity of the AAS architecture is minimized by integrating the WTM and LFA in FIR filter.

Table 1. Parameters of AAS

Parameter	Description
$x(t)$	Received signal vector
$as(t)$	Desired signal
$i(t)$	Interference vector
$r(t)$	Drilling signal
w	Weighting vector
$\left[w^{(*)}\right]^{H}$	Hermitian transposed weighting vector
$u(t)$	Reference signal
α	Conjucate cycle
τ	Delay
$\hat{F}_{sc}(w)$	Objective function
$\hat{\rho}^{\alpha}_{yy^{(*)}}$	Objective function of AC-SCORE
λ	Sensing threshold
R_{xx}	Autocorrelation of input signal
R_{xu}	Cross correlation of input and reference signal
R_{ux}	Cross correlation of reference and input signal
R_{uu}	Autocorrelation of reference signal

The filter module used in the AAS-WTM-LFA architecture is shown in the Fig. 3 that comprises of address generator, register, accumulator, the control unit, Processing Element (PE), Read Only Memory (ROM), Random Access Memory (RAM) and LFA. The operations processed in AAS architecture by FIR filter are given as follows.

The ROM stores the coefficient data and the RAM stores the input data. The clock signal from the control unit is used to compute the filter output and reset the signal. The reset signal is used to rest the registers in FIR filter. The computation among the input data and filter coefficient are carried out by reading the data from the ROM. Since, the address generated by the address generator is used to perform read operation from ROM. The multiplication of coefficient and filter output are carried out by using WTM in PE and the output from the PE is delivered to the accumulator. In initial stage, the value of zero is hold by the register as well as the WTM multiplies the input address which is provided to RAM input along with coefficient. Then the output of PE is given to accumulator. In 2nd clock cycle, the register has filter output of 1st clock cycle. The initial clock cycle output is provided to the LFA input which helps to add the output of filter. Subsequently, these values are saved in the register to produce filter output and the Verilog output is sent to the demodulator. The parameters used in this AAS architecture are mentioned in the Table 1.

3.2 Wallace tree multiplier

Generally, a WTM [23] is used for performing the multiplication between two integers. The filter operation is performed by considering two values such as RAM output and coefficient of ROM. These two values are given as input to the WTM inserted in processing element. The usage of WTM helps to reduce the propagation delay. The propagation delay in the tree multiplier is equal to O (log3/2 (N)). For large multiplier word lengths, this WTM is faster than the carry-save structure. The WTM perform multiplication operation with minimum logical area and minimum delay that is suitable for high speed operation. Fig. 4 and 5 shows the architecture of WTM and adder utilized in the WTM respectively. The F block given in the WTM is specifies the adder used WTM. This adder provides two outputs such as sum out (S_0) and carry out (C_0).

3.3 Ladner-FISCHER adder

LFA [24] is generally a parallel prefix form of Carry Look-ahead Adder. The parallel prefix graph which contains carry operator nodes represents the LFA. The amount of time required by LFA for generating the carry signals in prefix adder is o(log n). This LFA is faster adder and it is common choice in industry to provide higher performance. The LFA achieves better performance due to the minimum logic depth. The Fig. 6 shows the architecture of 16 bit LFA used in the AAS-WTM-LFA architecture. The input A and B shown in Fig. 6 are the output from the processing element and feedback value respectively.

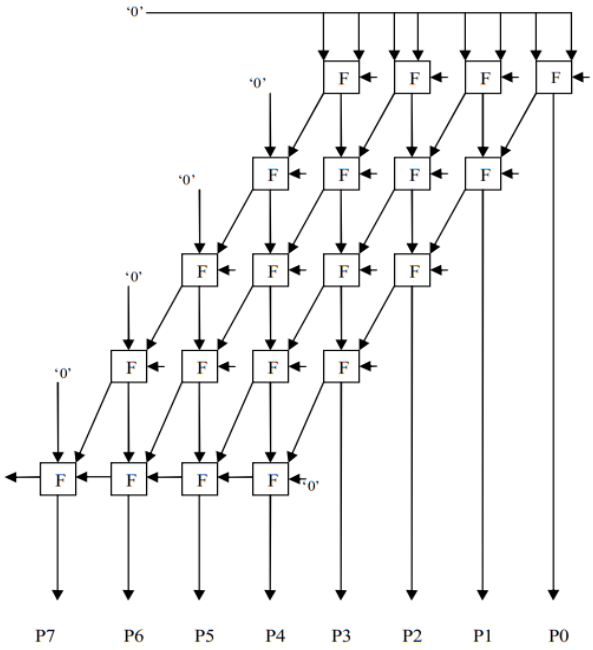

Figure. 4 Architecture of WTM

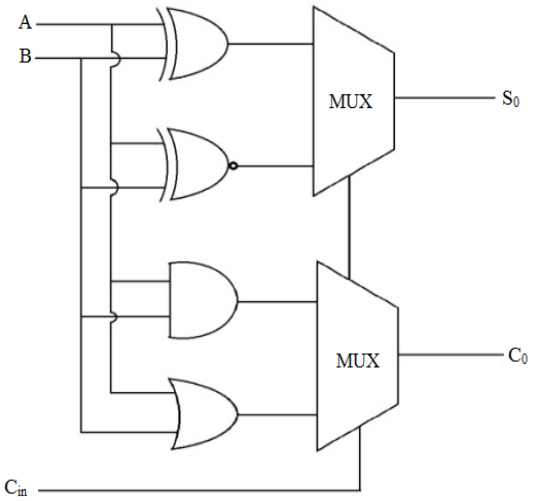

Figure. 5 Architecture of full adder used in the WTM

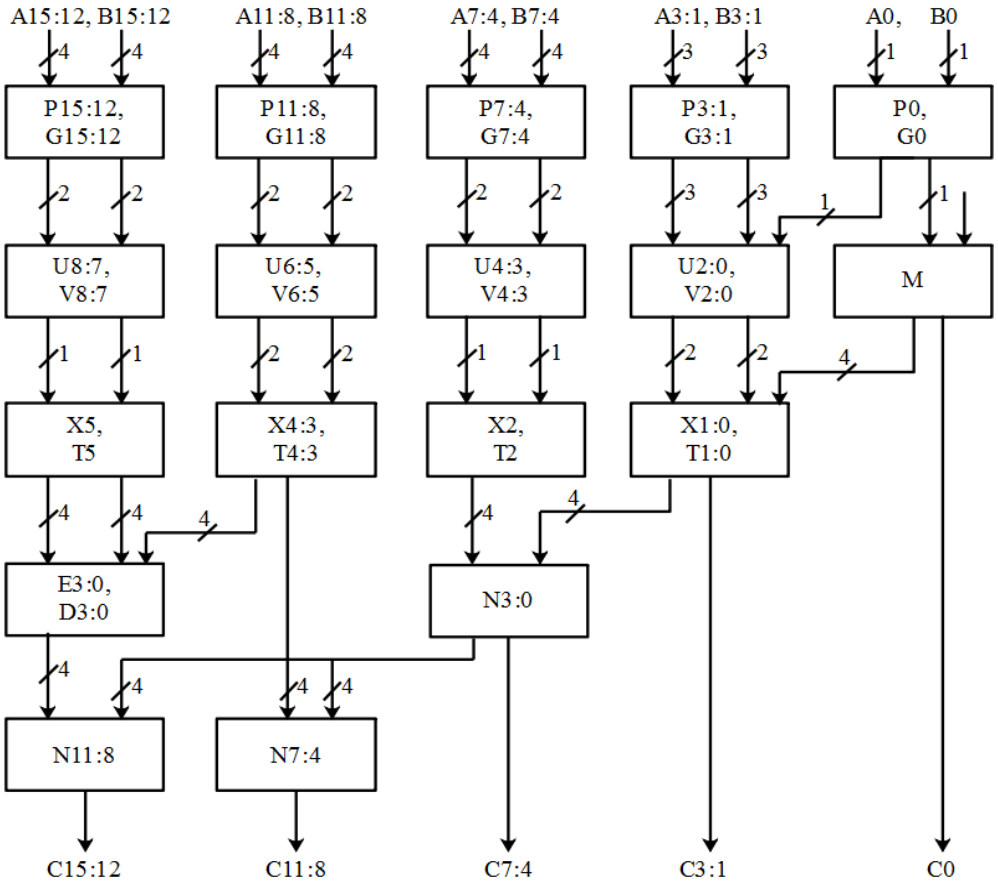

Figure. 6 Architecture of 16-bit LFA used in AAS-WTM-LFA

An efficient arrangement of LFA is look likes tree structure to perform higher arithmetic operations. This LFA is high speed adder that focuses in the gate level logic and it is designed with minimum amount of logic gates. This helps to reduce the memory and delay of the AAS-WTM-LFA architecture. In AAS-WTM-LFA architecture, the 16 bit addition is performed for decreasing the area and improving the speed of the spectrum sensing in CR. The inputs of the LFA are generated and propagated by using XOR and AND operations respectively.

The operation of generation and propagation are carried out in gray cell and black cell. Subsequently, it provides carry value. The sum value is obtained by taking the XOR between carry and next bit propagation value. The architecture of Efficient LFA provides the less delay and less memory for the 16-bit addition.

4. Results and discussion

The simulation results of the AAS-WTM-LFA architecture is described in this section. Additionally, the comparative analysis also provided to know the efficiency of the AAS-WTM-LFA based spectrum sensing in CR. The existing methods used for the comparison are ACS [18], AAS [18], AAS-CSLA [22], AAS-R8-CSA [22] and AAS-R8-CSLA [22]. The implementation of AAS-WTM-LFA architecture is carried out in the Xilinx tool for various virtex devices. Here, ACS [18], AAS [18], AAS-CSLA [22], AAS-R8-CSA [22] and AAS-R8-CSLA [22] are implemented by using Xilinx tool to evaluate the AAS-WTM-LFA architecture.

4.1 Simulation setup

The FPGA performance of the AAS-WTM-LFA architecture is analyzed in terms of LUT, flip-flop, slice, bonded Input and Output Block (IOB), frequency and power.

In this AAS-WTM-LFA architecture, the data created by the data generator is modulated by using different modulation schemes such as BPSK, QPSK, QAM modulator. Then the modulated data are transmitted through the AWGN channel. Then the final control block is considered as AAS-WTM-LFA based spectrum sensing technique.

Table 2. Comparative analysis of AAS-WTM-LFA for Spartan 6 device

Device	Architecture	Slices	Flip flops	LUT	Bonded IOB	Frequency (MHz)	Power (W)	Delay (ps)
Spartan 6	ACS [18]	527	720	882	340	72.622	0.916	3.13
	AAS [18]	519	715	878	337	78.152	0.897	2.56
	AAS-CSLA [22]	122	34	282	11	85.873	0.721	1.86
	AAS-R8-CSA [22]	119	34	280	11	82.652	0.701	1.78
	AAS-R8-CSLA [22]	118	34	278	11	89.241	0.678	1.54
	AAS-WTM-LFA	98	29	247	10	98.315	0.514	1.12

The output signal samples of AWGN are directly send to Xilinx RTL compiler through MATLAB. Here, the WTM and LFA based AAS is designed using Verilog code. The architecture of AAS-WTM-LFA is simulated in two different design cases Spartan device and AAS-WTM-LFA with Virtex device.

4.1.1. Performance analysis using Xilinx tool

The performances of AAS-WTM-LFA is compared with five different architectures in terms of FPGA parameters. The five different architectures used for the comparison are ACS [18], AAS [18], AAS-CSLA [22], AAS-R8-CSA [22] and AAS-R8-CSLA [22].

Table 2 shows the comparison of AAS-WTM-LFA with exiting architectures for Spartan 6 with XC6SLX16 device and CSG324 package. Generally, the Spartan 6 device is modern device that delivers the capacities of leading system integration with less system cost. Besides the less system cost is achieved in high volume applications than the Spartan 3 devices. In this research, AAS based spectrum sensing is mainly depending on the blocks of WTM and LFA. Table 2 shows that the performances of AAS-WTM-LFA in Spartan 6 device are better than the remaining architectures. The 16 bit LFA used in the AAS is effectively enhances the speed and reduces the area.

Additionally, the comparative analysis of AAS-WTM-LFA for different Virtex devices are shown in Table 3. The Table 3 shows that the AAS-WTM-LFA gives better performance than the remaining architectures in all Virtex devices. For example, the number of LUT for the AAS-WTM-LFA in Virtex 6 device is 7, it is less when compared to the existing architectures.

From the Table 3, knows that the AAS-WTM-LFA architecture achieves higher frequency for all Virtex devices. An achievement of higher frequency using AAS-WTM-LFA shows that the respective architecture also obtains less delay. Therefore, the input processing time through the FPGA based AAS-WTM-LFA implementation consumes less time. The simulation waveform obtained from the FPGA implementation is shown in the Fig. 7. The control signals used in the architecture of AAS-WTM-LFA are Clk, en, rst and done. The input and output of the signal processed through the AAS are Data_in and Data_out (i.e., sine wave generator output). Additionally, the address generated in this AAS-WTM-LFA is represented as Addr.

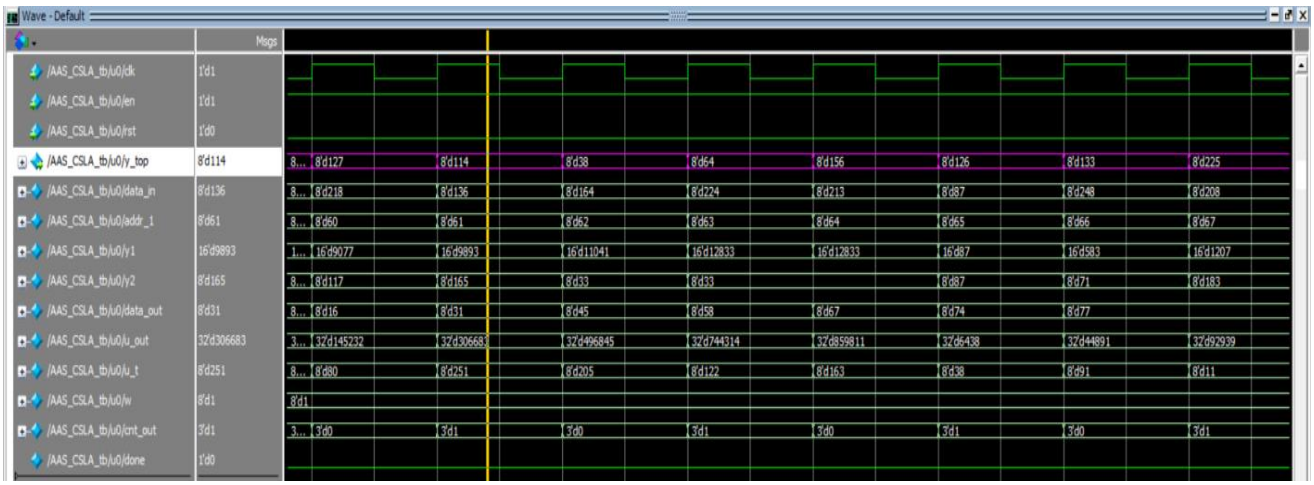

Figure. 7 Simulation waveform

Table 3. Comparative analysis of AAS-WTM-LFA for different Virtex devices

Device	Methodology	LUTs	Flip flops	slices	Bonded IOB	Frequency (MHz)	Power (W)	Delay (ps)
Virtex 4 Xc4vfx12	ACS [18]	779/10944	362/10944	552/5472	67/240	70.213	0.323	3.65
	AAS [18]	758/10944	348/10944	542/5472	53/240	74.134	0.235	2.31
	AAS-CSLA [22]	367/10944	117/10944	283/5472	11/240	76.304	0.191	1.79
	AAS-R8-CSA [22]	383/10944	117/10944	292/5472	11/240	72.586	0.191	1.35
	AAS-R8-CSLA [22]	354/10944	115/10944	260/5472	11/240	78.652	0.179	1.21
	AAS-WTM-LFA	314/10944	103/10944	243/5472	10/240	82.417	0.152	1.04
Virtex 5 Xc5vlx20t	ACS [18]	412/12480	18/12480	192/3120	18/172	69.113	0.415	3.17
	AAS [18]	391/12480	16/12480	183/3120	14/172	73.652	0.432	2.52
	AAS-CSLA [22]	376/12480	11/12480	169/3120	11/172	82.143	0.325	2.01
	AAS-R8-CSA [22]	399/12480	117/12480	164/3120	11/172	81.718	0.325	1.82
	AAS-R8-CSLA [22]	73/12480	25/12480	25/3120	11/172	85.603	0.322	1.47
	AAS-WTM-LFA	61/12480	19/12480	19/3120	10/172	79.174	0.265	1.08
Virtex 6 Xc6vcx75t	ACS [18]	18/46560	45/93120	13/11640	19/240	376.285	1.802	3.56
	AAS [18]	16/46560	31/93120	10/11640	14/240	383.321	1.592	2.83
	AAS-CSLA [22]	12/46560	25/93120	8/11640	11/240	418.25	1.293	2.37
	AAS-R8-CSA [22]	15/46560	25/93120	8/11640	11/240	417.162	1.293	1.98
	AAS-R8-CSLA [22]	11/46560	25/93120	7/11640	11/240	417.162	1.291	1.49
	AAS-WTM-LFA	10/46560	19/93120	6/11640	11/240	423.417	0.914	1.25
Virtex 6 LP Xc6vlx75tl	ACS [18]	24/46560	43/93120	17/11640	21/240	262.214	1.651	3.49
	AAS [18]	18/46560	31/93120	12/11640	18/240	285.563	1.347	2.68
	AAS-CSLA [22]	14/46560	25/93120	7/11640	11/240	319.214	1.065	2.31
	AAS-R8-CSA [22]	13/46560	25/93120	8/11640	11/240	318.269	1.065	1.92
	AAS-R8-CSLA [22]	12/46560	25/93120	6/11640	11/240	320.487	1.062	1.43
	AAS-WTM-LFA	10/46560	19/93120	5/11640	10/240	334.465	0.904	1.06
Virtex 7 Cx7vx330t	ACS [18]	16/204000	43/408000	19/51000	19/600	412.243	0.298	3.38
	AAS [18]	12/204000	31/408000	14/51000	15/600	433.421	0.213	2.56
	AAS-CSLA [22]	9/204000	25/408000	9/51000	11/600	478.629	0.143	2.07
	AAS-R8-CSA [22]	9/204000	25/408000	8/51000	11/600	478.629	0.143	1.85
	AAS-R8-CSLA [22]	8/204000	25/408000	9/51000	11/600	478.629	0.142	1.48
	AAS-WTM-LFA	7/204000	19/408000	8/51000	10/600	484.147	0.108	1.14

4.2 Performance analysis using MATLAB

In this section, the quality of the signal which is given in the AAS-WTM-LFA is analyzed in terms of BER and FAR. Since, the signal quality is analyzed by varying the SNR range from -10 to 10. The signal quality is compared with one exiting architecture namely AAS-R8-CSLA architecture. The BER and FAR are described as follows.

4.2.1. Bit Error Rate

Generally, the BER is defined as the amount of bit errors per unit time. BER is defined as the ratio between the total numbers of transmitted bits in a certain time. The BER is specified in the following Eq. (9).

$$BER = \frac{Affected\ bits}{Total\ transmitter\ bits} \quad (9)$$

4.2.2. False Alarm Rate

FAR is defined as the amount of false alarm per the total amount of warning in a specified situation. Table 4, Table 5 and Table 6 shows the comparative analysis of signal quality for AAS-WTM-LFA with AAS [18] and AAS-R8-CSLA [22]. The Table 4, Table 5 and Table 6 shows the comparison for the QPSK, BPSK and QAM respectively. The BER and FAR comparison is taken when the 100 bits given as the input to the AAS-WTM-LFA architecture.

From the Tables, it concludes that the QAM used in the AAS-WTM-LFA achieves better performance than the AAS-R8-CSLA architecture. For example, the BER of the AAS-WTM-LFA is 0.09 for -10dB SNR, it is less when compared to the QPSK and BPSK modulation.

Table 4. Comparative analysis of AAS-WTM-LFA for QPSK modulation

SNR	BER			FAR		
	AAS [18]	AAS-R8-CSLA [22]	AAS-WTM-LFA	AAS [18]	AAS-R8-CSLA [22]	AAS-WTM-LFA
-10	0.35	0.31	0.30	35	31	30
-8	0.30	0.28	0.26	30	28	27
-6	0.27	0.26	0.25	26	26	24
-4	0.20	0.17	0.16	19	17	15
-2	0.17	0.14	0.12	17	14	13
0	0.14	0.09	0.08	14	9	7
2	0.10	0.01	0.01	10	1	1
4	0.08	0.01	0	6	1	1
6	0.01	0	0	1	0	0
8	0.01	0	0	1	0	0
10	0	0	0	0	0	0

Table 5. Comparative analysis of AAS-WTM-LFA for BPSK modulation

SNR	BER			FAR		
	AAS [18]	AAS-R8-CSLA [22]	AAS-WTM-LFA	AAS [18]	AAS-R8-CSLA [22]	AAS-WTM-LFA
-10	0.31	0.29	0.28	31	29	28
-8	0.26	0.18	0.17	25	18	15
-6	0.19	0.16	0.15	19	16	14
-4	0.13	0.09	0.08	12	9	8
-2	0.08	0.07	0.06	8	7	6
0	0.05	0.01	0.01	5	1	1
2	0.03	0.01	0	3	1	0
4	0.01	0	0	1	0	0
6	0.01	0	0	1	0	0
8	0	0	0	0	0	0
10	0	0	0	0	0	0

Table 6. Comparative analysis of AAS-WTM-LFA for QAM modulation

SNR	BER			FAR		
	AAS [18]	AAS-R8-CSLA [22]	AAS-WTM-LFA	AAS [18]	AAS-R8-CSLA [22]	AAS-WTM-LFA
-10	0.15	0.10	0.09	15	10	9
-8	0.10	0.02	0.02	10	4	3
-6	0.07	0.01	0.01	7	2	1
-4	0.02	0	0	2	0	0
-2	0.01	0	0	1	0	0
0	0.01	0	0	1	0	0
2	0	0	0	0	0	0
4	0	0	0	0	0	0
6	0	0	0	0	0	0
8	0	0	0	0	0	0
10	0	0	0	0	0	0

The graphical illustration of BER and FAR for three different modulation methods are given in Fig. 8 and Fig. 9 respectively.

5. Conclusion

Nowadays, the challenges due to the next generation spectrum usage are overcome by using the CR. In this research, the WTM and LFA are integrated in the AAS-WTM-LFA architecture to improve the spectrum sensing performance. This helps to achieve an improved sensing function and radio sensitivity during the allocation of optimal bands to the users of CR. Here, the weak signals of PU are effectively identified by using the AAS architecture. Besides, the propagation delay required by the WTM is less as well as the delay and memory used in the FIR filter is reduced by using the LFA.

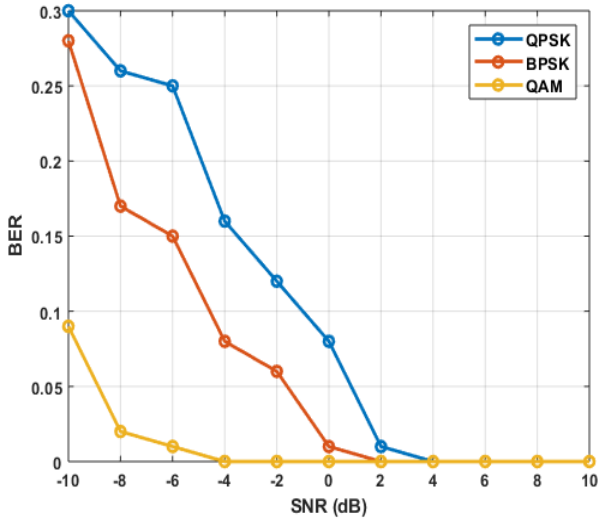

Figure.8 BER comparison of AAS-WTM-LFA for different modulation schemes

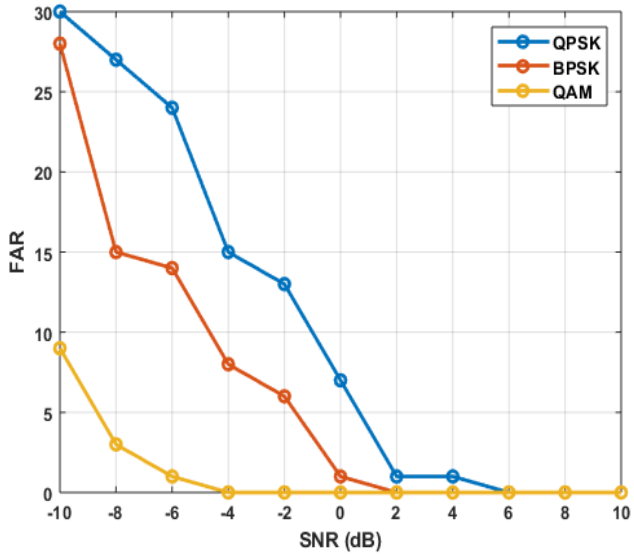

Figure.9 FAR comparison of AAS-WTM-LFA for different modulation schemes

The performance of the AAS-WTM-LFA architecture is better when compared to remaining five architectures such as ACS, AAS, AAS-CSLA, AAS-R8-CSA and AAS-R8-CSLA. For example, the frequency of the AAS-WTM-LFA is for Virtex 7 device, it is high when compared to other architectures. Additionally, the performance of AAS-WTM-LFA with QAM modulation is better, than the QPSK and BPSK modulation. The FAR of AAS-WTM-LFA with QAM is 3 for -8dB SNR, it is less when compared to the AAS-R8-CSLA and to other modulation scheme. In future, an effective modulation technique and optimization in FPGA modules can be developed to improve the CR performances.

Conflicts of Interest

The authors declare no conflict of interest.

Author Contributions

The paper conceptualization, methodology, software, validation, formal analysis, investigation, resources, data curation, writing-original draft preparation, writing-review and editing, visualization, have been done by 1st author. The supervision, and project administration, have been done by 2nd author.

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