OPTIMIZED SPACE-VECTOR-MODULATED QUASI Z-SOURCE NPC INVERTER FOR SOLAR PV APPLICATION

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Abstract*: An optimized space vector modulation technique for controlling a quasi Z-source NPC inverter for solar photovoltaic application is presented in this paper. The presented algorithm optimizes the number of switching transitions over a switching cycle by modifying the placement of the shoot-through states in some of the sub-triangles of the space vector diagram of a conventional neutral point clamped inverter. This approach leads to a reduction in the total losses of the quasi Z-source inverter by reducing the switching losses. The presented concepts are expected to be cheaper than existing methods because a reduction in losses will lead to the use of smaller and cheaper heat sinks in practical implementation. In this paper, the effectiveness of the proposed optimized space vector modulation technique has been demonstrated through simulations in SABER®.*

1. INTRODUCTION

Conventional power generation based on fossil fuel resources is considered to be unsustainable in the long term. This has been the main driver for an extensive deployment of renewable energy resources such as wind power, solar photovoltaic (PV), hydropower, biomass power, among others, into the power grid in the last several years [1, 2]. Among the major renewables, solar PV has continued to be expanded at a rapid rate over the years, and it already plays a substantial role in electricity generation in some countries [3].

Power electronic converters have been acknowledged to be an enabling technology for more renewable energy integration into the grid, including solar PV systems [4]. These converters are to provide stable output voltage in spite of unstable input variables at the highest efficiency, lowest cost and minimum size. This has led to the development of many new interface power electronic converters. Most of the converter topologies employed in PV systems are characterized as two-stage converters. Two-stage converters employ a cascade of dc-dc converter and voltage source inverter (VSI) for processing the dc power available from the PV panels into ac power suitable for grid integration [5]. To improve the spectral performance of the output voltage fed into the grid, multilevel inverters are usually employed. One of such topologies is the neutral-point-clamped (NPC) inverter. Some of the advantages of the NPC inverter over the two-level counterpart include lower voltage stress across semiconductor devices, lower switching losses and better harmonic performance [6, 7]. However, the ac output voltage of the NPC inverter is limited and cannot exceed the available input voltage. Also, dead time is needed to prevent shoot-through problem caused by electromagnetic interference, which causes waveform distortion.

At present, the Z-source concept improves the structure of traditional inverters by bringing onboard voltage buck-boost capability in a single-stage structure [8]. A single-stage structure is an attractive approach because of its compactness, low cost and reliability. The Z-source NPC (ZNPC) inverter combines the properties of Z-source network with those of NPC inverter [9, 10]. However, the ZNPC inverter draws discontinuous input current which is not suitable for PV application. To overcome this drawback, the quasi Z-source NPC (qZNPC) inverter was proposed [11]. The qZNPC inverter draws continuous current from the PV array and is capable of handling a wide input voltage range [12]. Other advantages of the qZNPC inverter include employment of lower rated components, reduction in switching ripples to the PV panels, and lower EMI problems.

Space vector modulation (SVM) technique for controlling ZNPC/qZNPC has been reported in the literature [13-15]. A study of the switching patterns adopted in [13-15] reveals that there are some regions where the number of switching transitions can be optimized. This paper seeks to bridge that research gap by optimizing the number of switching transitions in these regions in the implementation of SVM strategy for optimal performance of the qZNPC inverter in PV application. The rest of the paper is organized as follows. In section 2, the operating principles as well as steady state analysis of the qZNPC inverter is presented. Section 3 describes the optimized space vector modulation strategy for controlling the qZNPC inverter to perform voltage buck-boost functionality. Simulation results are presented in section 4 to verify the proposed optimized algorithm.

2. TOPOLOGY AND OPERATING PRINCIPLES

Figure 1 illustrates the topology of the qZNPC inverter. The PV string is coupled to the inverter by the quasi Z-source network. Four switches with antiparallel diodes and associated clamping diodes form a phase leg of the inverter. The switching states of the qZNPC inverter are categorized into non-shoot-through (NST) and shoot-through (ST) states. The NST states are P, O and N. The P state means two upper switches in a phase leg are switched on, O means two middle switches conduct and N signifies turning on of two bottom switches. The shoot-through states are classified as full-shoot-through (FST), lower-shoot-through (LST) and upper-shoot-through (UST) states. FST refers to the simultaneous turn on of all four switches in a phase leg, UST means the three upper swtches are turned on while LST signifies the turning on of three bottom switches in a phase leg. The behaviour of qZNPC inverter is usually represented by equivalent circuits showing NST, UST and LST states for the partial shoot-through operation mode as shown in *fig. 2*.

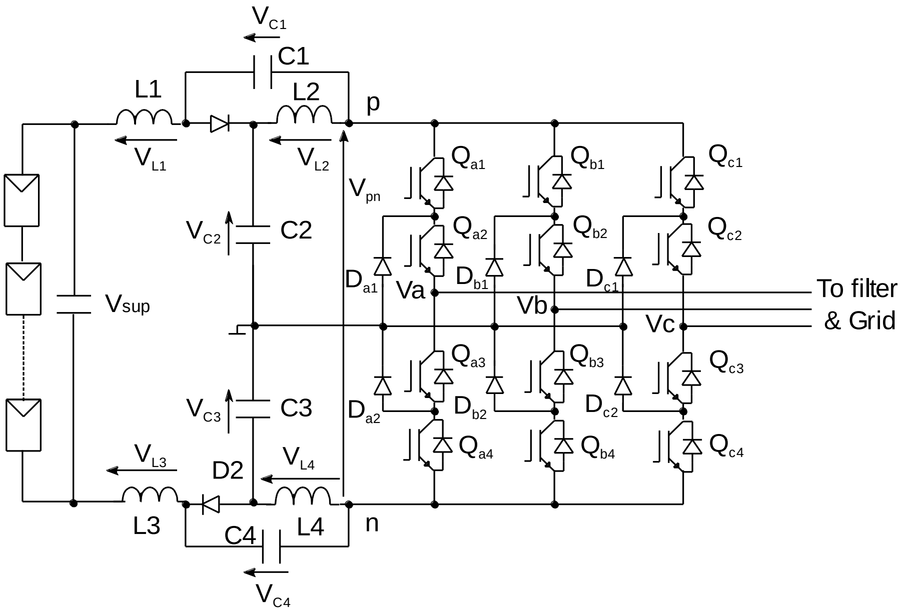

Fig. 1. Quasi Z-source NPC inverter

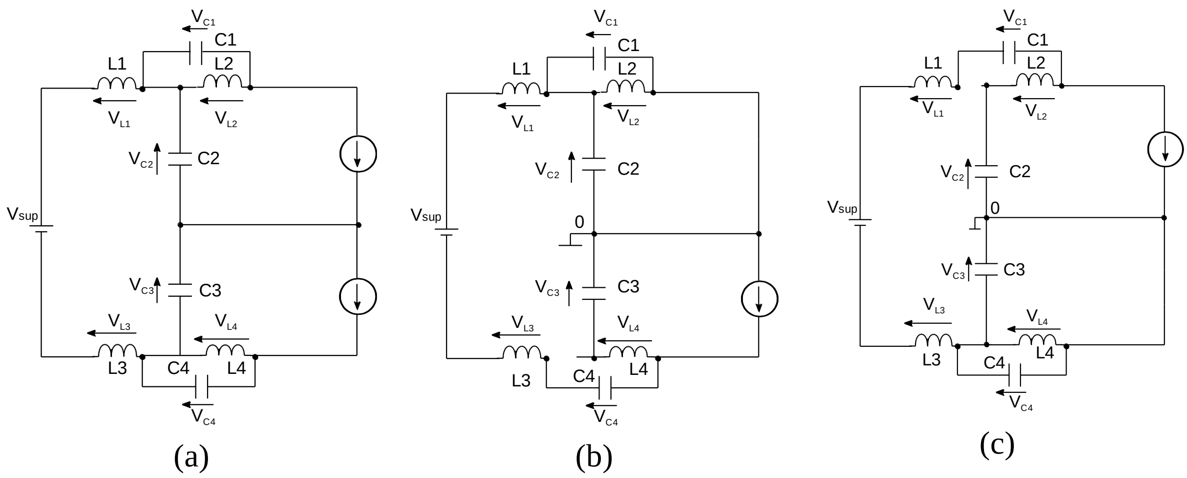

Fig.2. Simplified representation of qZNPC inverter in (a) NST, (b) UST, and (c) LST states.

Assuming symmetric quasi Z-source network and operation in the continuous conduction mode, the operation of the qZNPC inverter can be written as:

$$D_N + D_U + D_L = 1 \tag{1}$$

where D_N, D_U and D_L represent the duty cycles of the NST, UST and LST states, respectively. To ensure symmetric operation, D_U and D_L are set to be equal and represented by D_0. The peak of the dc-link voltage is given by the sum of the capacitor voltages, as

$$V_{C1} + V_{C2} + V_{C3} + V_{C4} = \widehat{V}_{pn}. \tag{2}$$

Performing inductor voltage balance over a switching period yields:

$$V_{C1} = V_{C4} = \frac{D_0 \cdot V_{\sup}}{2 - 4D_0}, \tag{3}$$

$$V_{C2} = V_{C3} = \frac{(1 - D_0) \cdot V_{\sup}}{2 - 4D_0}. \tag{4}$$

The peak dc-link voltage and the peak output line-to-line voltage are then found to be given by (5) and (6) respectively.

$$\widehat{V}_{pn} = \frac{V_{\sup}}{1 - 2D_0}. \tag{5}$$

$$\widehat{V}_{out} = M \cdot \left(\frac{1}{1 - 2D_0}\right) \cdot V_{\sup} = B_F \cdot \left(M \cdot V_{\sup}\right), \tag{6}$$

In (6), $D_0 < 0.5$ is the shoot-through ratio, B_F is the boost factor while M is the modulation index, respectively.

3. OPTIMISED SVM TECHNIQUE FOR QUASI Z-SOURCE NPC INVERTER

Space vector modulation uses the concept of space vectors to compute duty cycles of the switches. The operation of each phase leg of a traditional NPC inverter can be represented by switching states P, O, and N. *Figure 3* shows the space vector diagram (SVD) of a conventional NPC inverter.

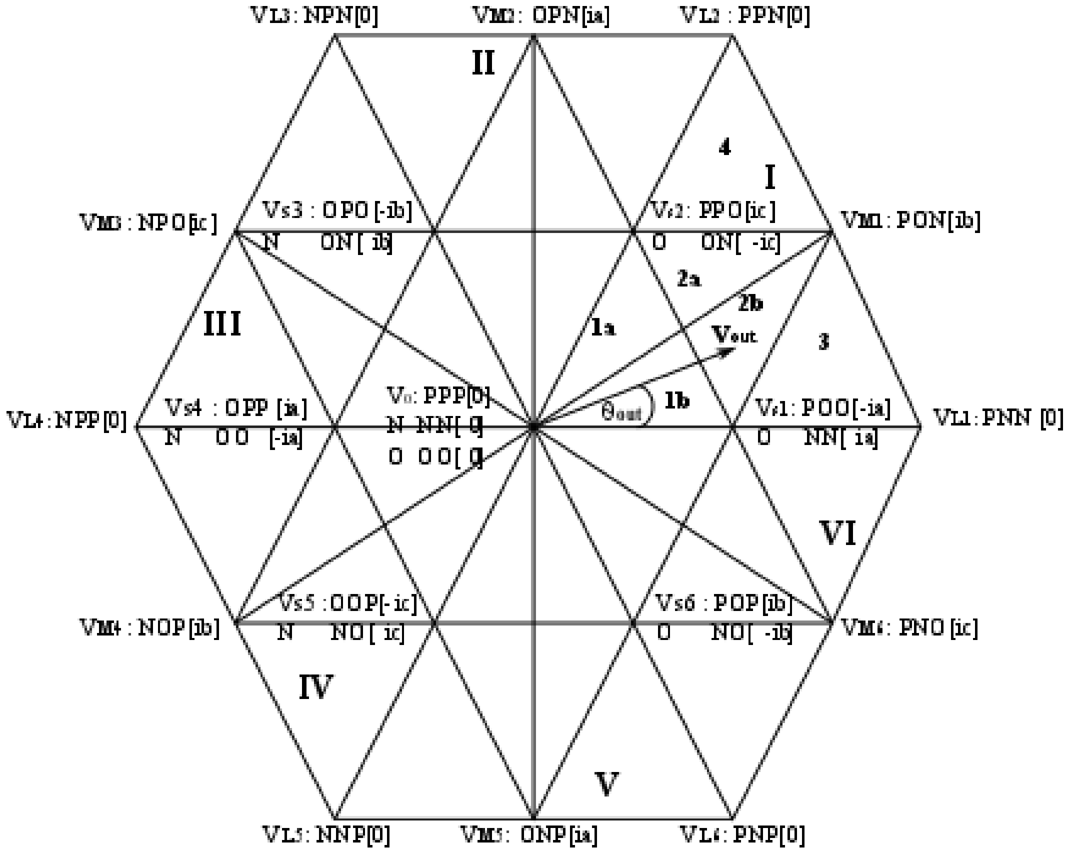

Fig. 3. Space vector diagram of conventional NPC inverter

The SVD is divided into six sectors (I to VI) and contain 27 switching states classified as zero (V_0), small (V_{S1} to V_{S6}), medium (V_{M1} to V_{M6}) and large (V_{L1} to V_{L6}) vectors. Each sector contains four smaller triangles labelled 1 (1a and 1b), 2 (2a and 2b), 3 and 4, respectively. The rotating reference vector V_{out} represents the desired three-phase output voltage which is synthesized with the nearest three vectors in each switching cycle. For three-level operation of the conventional NPC inverter, the modulation index *M* should be between 0.57 and 1. Under such conditions, the reference vector traverses triangles 2, 3 and 4 in each sector. If the reference vector is located in triangle 3 of sector I, for instance, then it has to be synthesized with the vectors V_{S1}, V_{M1} and V_{L1}.

The space vector modulation process is completed by applying the selected voltage vectors to the output according to a switching sequence. A sequence that results in minimum number of transitions is the preferred choice because that leads to high quality output voltage waveform and lower switching losses. To achieve minimum number of switching transitions, a 7-segment switching sequence is usually adopted. It is often convenient to perform “origin shifting” and subsequently perform a three-level modulation using two-level principles [16].

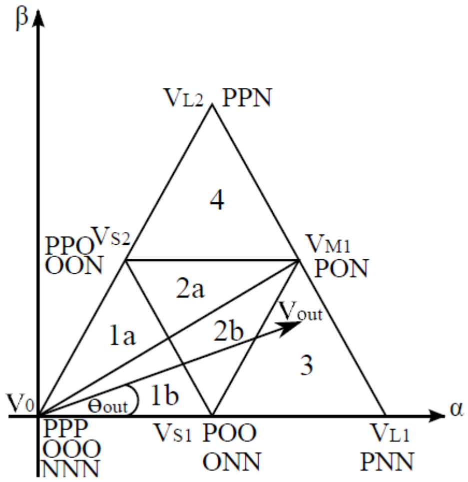

Fig. 4. Space vector diagram for sector I of the conventional NPC inverter

Consider *fig. 4* which depicts the vectors in sector I of the SVD shown in *fig.3*. If the origin is shifted from [PPO/OOO/NNN] to [POO/ONN], the the equivalent null (E-null) state is transferred to [POO/ONN] while the equivalent active (E-active) states are transferred to [PPP/OOO/NNN], [PPO/OON], PON and PNN, respectively. The sequence over time of the application of the selected converter switching states has to be decided for every switching cycle. For instance in triangle 3 the voltage vectors V_{S1} [PPO/ONN], V_{M1} [PON], and V_{L1} [PNN] are selected to synthesize the reference vector V_{out} so the switching sequence used is ONN → PNN → PON → POO → PON → PNN → ONN. The number of switching transitions here is twelve (12).

To enable boost capability, shoot through states have to be inserted in appropriate phase legs. In case of two-level quasi Z-source inverter, shoot-through states are applied using the duration of the null vectors only. The two null vectors in two-level SVM both produce zero line-to-line voltage. Both null vectors and shoot-through states produce zero line-to-line voltage so they can replace each other for voltage boosting. The shoot-through states in the two-level quasi Z-source inverter applies a full short circuit across the dc link.

For the case of qZNPC inverter, the small vectors serve the same purpose as the null vectors of the two-level quasi Z-source inverter. However, there is a difference in that none of the small vectors produces zero line-to-line volage. Thus, if nearest three vector switching is desired then full shoot through cannot be applied. This is the main reason behind the choice of alternate UST and LST in modulating qZNPC inverters. While doing this, we have to ensure that the number of switching transitions is minimized.

We now consider the insertion of shoot-through states when the reference voltage vector is located in triangles 2, 3 and 4. Triangle 1 is not considered because when the reference vector is located in that triangle, the output voltage degenerates into two levels which defeats the purpose of multilevel output voltage. Tables 1 to 4 show the switching sequences and number of switching transistions when the reference voltage vector is located in triangle 2a, 2b, 3 and 4, respectively.

Table 1. Switching transitions in triangle 2a with conventional SVM for qZNPC inverter

	STATES	**Qa 1,2,3,4**	**Qb 1,2,3,4**	**Qc 1,2,3,4**	**Switchings**
	PPO	1100	1100	0110	
LST	PPL	1100	1100	0111	1
	POO	1100	0110	0110	3
	PON	1100	0110	0011	2
UST	UON	1110	0110	0011	1
	OON	0110	0110	0011	1
UST	UON	1110	0110	0011	1
	PON	1100	0110	0011	1
	POO	1100	0110	0110	2
LST	PPL	1100	1100	0111	3
	PPO	1100	1100	0110	1
Total					16

Table 2. Switching transitions in triangle 2b with conventional SVM for qZNPC inverter

	STATES	**Qa 1,2,3,4**	**Qb 1,2,3,4**	**Qc 1,2,3,4**	**Switchings**
	ONN	0110	0011	0011	
UST	UNN	1110	0011	0011	1
	OON	0110	0110	0011	3
	PON	1100	0110	0011	2
LST	POL	1100	0110	0111	1
	POO	1100	0110	0110	1
LST	POL	1100	0110	0111	1
	PON	1100	0110	0011	1
	OON	0110	0110	0011	2
UST	UNN	1110	0011	0011	3
	ONN	0110	0011	0011	1
Total					16

Table 3. Switching transitions in triangle 3 with conventional SVM for qZNPC inverter

	STATES	**Qa 1,2,3,4**	**Qb 1,2,3,4**	**Qc 1,2,3,4**	**Switchings**
	POO	1100	0110	0110	
LST	POL	1100	0110	0111	1
	PON	1100	0110	0011	1
	PNN	1100	0011	0011	2
UST	UNN	1110	0011	0011	1
	ONN	0110	0011	0011	1

	STATES	Qa 1,2,3,4	Qb 1,2,3,4	Qc 1,2,3,4	Switchings
UST	UNN	1110	0011	0011	1
	PNN	1100	0011	0011	1
	PON	1100	0110	0011	2
LST	POL	1100	0110	0111	1
	POO	1100	0110	0110	1
Total					12

A critical study of the switching transitions in Tables 1 to 4 reveals that the switching transitions for triangles 3 and 4 are same as those encountered for the conventional NPC inverter. However, in triangle 2, the number of switching transitions is 16 per switching cycle instead of 12. For an ideal case the number of switching transitions per switching cycle should be 12. However, when shoot-through states are inserted into small vectors, there are regions on the SVD where 12 switching transitions per switching cycle is not possible in three-level SVM for Z-source converters. This is because as the reference vector traverses, there are two types of triangular regions (triangle 2 and triangles 3, 4) that come into the picture over a fundamental cycle. Triangles 3 and 4 offer 12 switching transitions while triangle 2 offers 16 switching transitions per switching cycle. This is the approach employed in [12-14].

Table 4. Switching transitions in triangle 4 with conventional SVM for qZNPC inverter

	STATES	Qa 1,2,3,4	Qb 1,2,3,4	Qc 1,2,3,4	Switchings
	OON	0110	0110	0011	
UST	UON	1110	0110	0011	1
	PON	1100	0110	0011	1
	PPN	1100	1100	0011	2
LST	PPL	1100	1100	0111	1
	PPO	1100	1100	0110	1
LST	PPL	1100	1100	0111	1
	PPN	1100	1100	0011	1
	PON	1100	0110	0011	2
UST	UON	1110	0110	0011	1
	OON	0110	0110	0011	1
Total					12

In triangle 2a, if the positions of PPL and PPO are interchanged the number of switching transitions can be reduced to 14. Similarly, in triangle 2b if the positions of UNN and ONN are interchanged, the number of switching transitions is reduced to 14. Since it is not possible to get 12 switching transitions in triangle 2 over a switching period, the minimum number of switching transitions after 12 is considered to be the optimal value. Therefore, 14 switching transitions in triangle 2 is considered as an optimal solution. The optimized switching patterns are shown in Tables 5 and 6 respectively.

The proposed optimized SVM approach leads to a reduction in the average switching frequency of the qZNPC inverter compared to the SVM methods found in previous works. This is the main contribution of this paper. With the number of switching transitions in a switching cycle optimized using the proposed approach, the position of UST/LST states in triangle 2 becomes different to those of triangles 3 and 4.

Table 5. Switching transitions in triangle 2a with proposed SVM for qZNPC inverter

	STATES	**Qa 1,2,3,4**	**Qb 1,2,3,4**	**Qc 1,2,3,4**	**Switchings**
LST	PPL	1100	1100	0111	
	PPO	1100	1100	0110	1
	POO	1100	0110	0110	2
	PON	1100	0110	0011	2
UST	UON	1110	0110	0011	1
	OON	0110	0110	0011	1
UST	UON	1110	0110	0011	1
	PON	1100	0110	0011	1
	POO	1100	0110	0110	2
	PPO	1100	1100	0110	2
LST	PPL	1100	1100	0111	1
Total					14

Table 6. Switching transitions in triangle 2b with proposed SVM for qZNPC inverter

	STATES	**Qa 1,2,3,4**	**Qb 1,2,3,4**	**Qc 1,2,3,4**	**Switchings**
UST	UNN	1110	0011	0011	
	ONN	0110	0011	0011	1
	OON	0110	0110	0011	2
	PON	1100	0110	0011	2
LST	POL	1100	0110	0111	1
	POO	1100	0110	0110	1
LST	POL	1100	0110	0111	1
	PON	1100	0110	0011	1
	OON	0110	0110	0011	2
	ONN	0110	0011	0011	2
UST	UNN	1110	0011	0011	1
Total					14

4. RESULTS AND DISCUSSION

A simulation exercise in SABER® was undertaken to verify the proposed optimized SVM technique for controlling the qZNPC inverter to perform voltage buck-boost function. The parameters presented in Table 7 were used for the simulation exercise.

Table 7. Parameters used for simulation studies

PV panel output voltage	500 – 600 V
Output voltage to grid	380 - 415 V, line-to-line rms
Grid frequency	50 Hz
Switching frequency	5 kHz
L_1, L_2, L_3, L_4	1 mH
C_1, C_2, C_3, C_4	470 μF

The main contribution of this paper is the optimization of the number of switching transitions during the control of qZNPC inverter to be as close as possible to that of a conventional NPC inverter. When a three-level nearest three vector SVM is implemented in a conventional NPC inverter, the number of switching transitions recorded when the reference vector traverses triangles 2, 3 and 4 is 36. When a similar exercise is done for a qZNPC inverter, the number of switching transitions recorded is 40. Applying the optimized SVM approach to the qZNPC inverter reduces the number of switching transistions from 40 to 38, which is the optimized number obtainable.

Simulation results for the case where the output of the PV array is assumed to be at a maximum of 600 V are shown in *fig. 5*. Under this condition, the qZNPC inverter works in the VSI mode. The required output voltage to the grid is synthesized with a modulation index of 0.915 with the shoot-through duty cycle set to 0. This operation results in a peak output line-to-line voltage of 547.2 V (387 V rms) as expected. This is clearly seen in *fig. 5a*. An output line-to-line voltage waveform with nearest three vector switching is shown in *fig. 5b; fig. 5c* – displays balanced output currents fed to the grid; *fig. 5d* – shows the current drawn from the PV array which is without ripples because shoot-through states have not been activated; *fig. 5e* – shows the capacitor voltages on C_1, C_4 and C_2, C_3 which are 0 V and 300 V, respectively.

To demonstrate the effectiveness of the optimized SVM algorithm described above for controlling the qZNPC inverter to perform voltage-boost operation, we assume the PV array's output voltage drops to the minimum of 500 V as a result of poor weather conditions. To synthesize the required grid voltages, the output of the PV array needs to be boosted. This is achieved by setting the modulation index and shoot-through ratio to 0.9 and 0.1, respectively. *Figure 6* depicts the main waveforms obtained when shoot-through states are used.

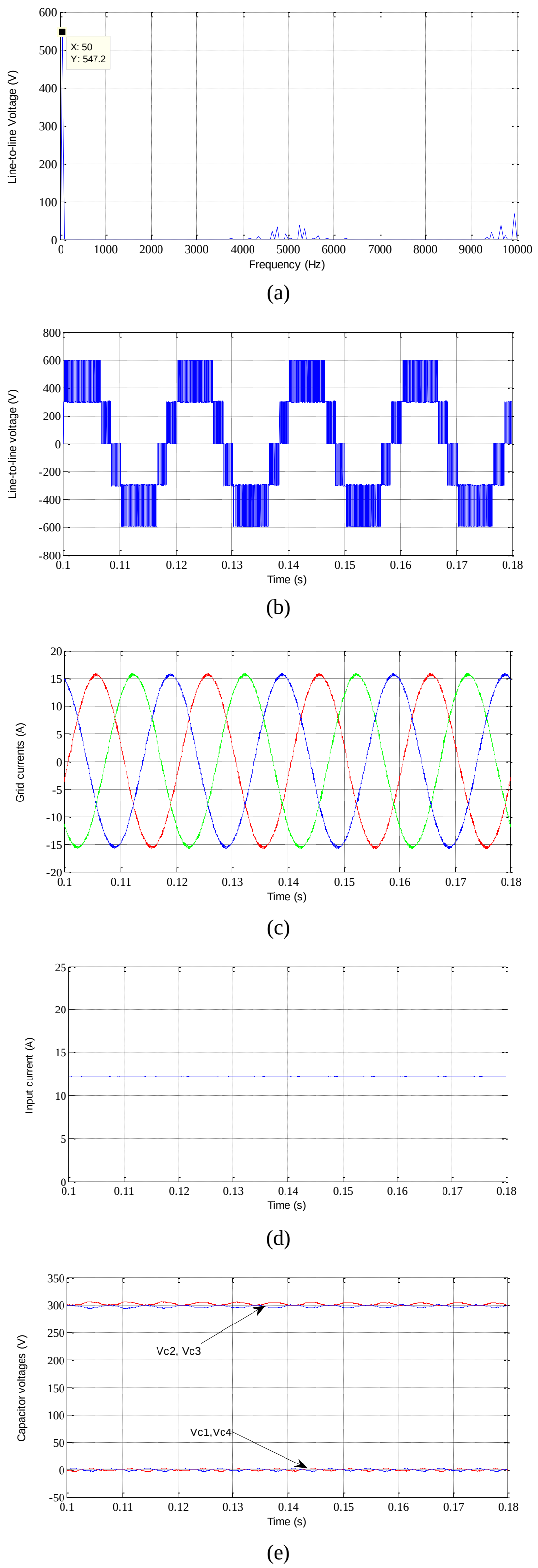

Fig.5 Buck-mode simulation results

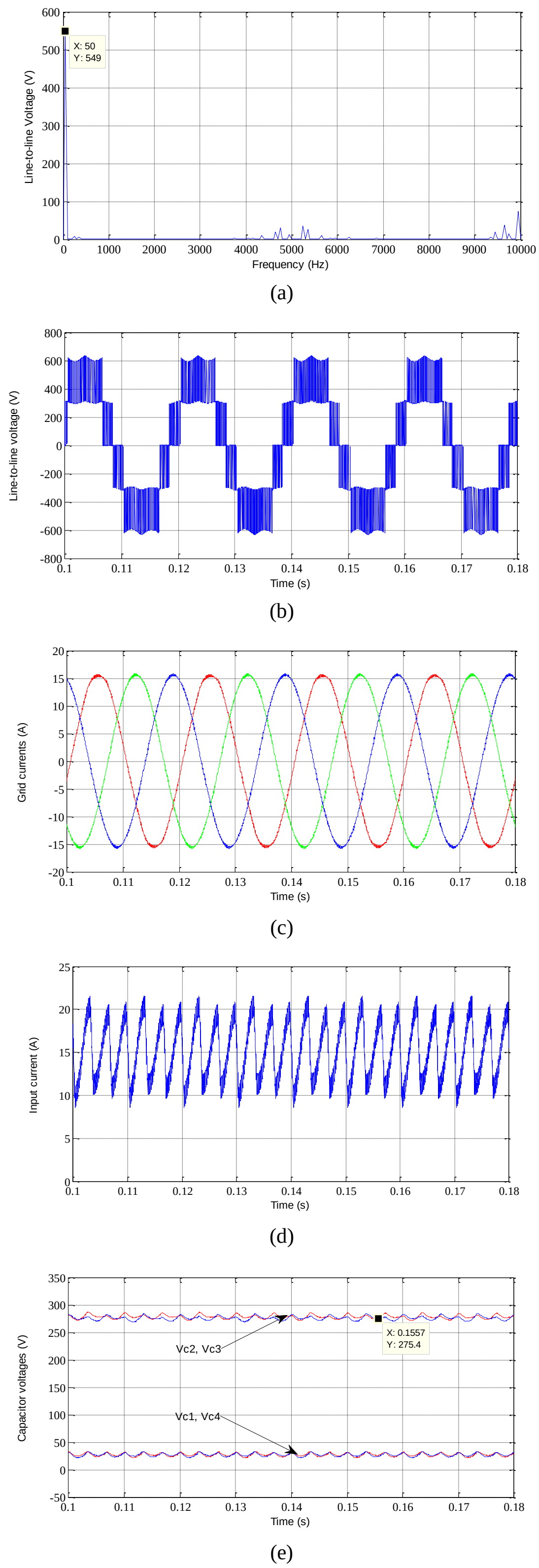

Fig. 6 Boost-mode simulation results

The spectrum of the output line-to-line voltage is shown in *fig. 6a*. This figure clearly shows a fundamental peak line-to-line voltage of 549 V as expected. The waveform for the output line-to-line voltage with nearest three vector switching is clearly shown in *fig. 6b*. *Figure 6c* shows the output currents of the qZNPV inverter which are still balanced and sinusoidal even when shoot-through states are inserted.

The current drawn from the PV array during this operating mode is shown in *fig. 6d*. This current is continuous with ripples resulting from the exchange of energy between the qZ-source inductors and capacitors during the insertion and removal of shoot-through states. The continuous input current drawn by the qZNPC inverter is very beneficial to the PV array. The voltages on the qZ-souce capacitors are also shown in *fig. 6e*.

The simulation results clearly agree well with the presented concepts thereby verifying the optimized SVM algorithm presented earlier. Compared with conventional SVM methods applied to the qZNPC inverter, the approach presented in this paper is cheaper since a reduction in the number of switching transitions will lead to decreased switching losses and therefore decreased total losses which will lead to the use of smaller (and cheaper) heat sinks in the practical implementation.

5. CONCLUSIONS

An optimized SVM technique for controlling a qZNPC inverter has been presented in this paper. Inserting UST and LST states into the conventional NPC inverter’s state sequence, voltage buck-boost functionality is achieved in a single-stage structure. The placement of the UST and LST states has been optimized in this paper leading to a reduction in the number of switching transitions per switching cycle compared to existing methods. Using the proposed optimized SVM algorithm leads to reduction in switching losses of the qZNPC inverter. The presented concepts have been verified using simulation results. It is expected that the presented solution will be cheaper than existing methods because of reduction in switching losses which will mostly result in lower overall losses and therefore smaller and cheaper heat sinks will be required in a practical implementation.

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