Impact Factor:	ISRA (India) = 3.117	SIS (USA) = 0.912	ICV (Poland) = 6.630
	ISI (Dubai, UAE) = 0.829	РИНЦ (Russia) = 0.156	PIF (India) = 1.940
		ESJI (KZ) = 8.716	IBI (India) = 4.260
	GIF (Australia) = 0.564	SJIF (Morocco) = 5.667	OAJI (USA) = 0.350
	JIF = 1.500		

SOI: 1.1/TAS DOI: 10.15863/TAS

International Scientific Journal

Theoretical & Applied Science

p-ISSN: 2308-4944 (print) **e-ISSN:** 2409-0085 (online)

Year: 2019 **Issue:** 04 **Volume:** 72

Published: 30.04.2019 **http://T-Science.org**

QR – Issue QR – Article

B.S. Yeralieva
TarSU them. M.H.Dulati
Master of Technical Sciences
b_eral@mail.ru

SECTION 4. Computer science, computer engineering and automation.

PROBLEM SOLVING OF DIGITAL PROCESSING SIGNALS ON COMPUTER INSTALLATION

Abstract: *One of the successful architectural solutions in the field of multiprocessor computing systems are reconfigurable computing systems (RVS), built on the base of programmable logic integrated circuits (FPGA).Rapid development of RVS is directly related to their ability to achieve high real performance for a wide class of labor-intensive tasks, since RVS allows you to program your computing architecture, adapting it under the structure of the current task being solved.*

Key words: *multiprocessor, digital, computing architecture.*

Language: *English*

Citation: Yeralieva, B. S. (2019). Problem solving of digital processing signals on computer installation. *ISJ Theoretical & Applied Science, 04 (72),* 592-594.

Soi: http://s-o-i.org/1.1/TAS-04-72-83 ***Doi***: crossref https://dx.doi.org/10.15863/TAS.2019.04.72.83

Introduction

Rapid development of effective computer installation caused common usage of digital signal processing technology (DSP). In turn delivery of the new intensive computational problem of the DSP is motivation for developments o more powerful computer installation (CI). One of the up-to-date classes of the intensive computational problem of the DSP is wide problem class of data-flowing computing of information, which means processing of big data store in real-time mode using the same mechanisms [1], which contains such problems as different hydro and radar data-flowing processing of pictures and the others.

Materials and Methods

For solving these classes of problems multiprocess computer installation is used (MCI), they make possible to reach high rate of productivity by means of development such direction as [1,2] – technical , which involves updating technologies of the creation element base, including by means of increasing the density of the valve-on-chip layout, leading to an increase of processor performance; - architectural - the building of optimal architectural Ci designed to solve specified classes of tasks; - algorithmic - the development of effective mathematical methods; - software - developing programs that maximize the capabilities of CI. Successes for each of the areas of development of the MAS give new qualitative opportunities in solving already existing complex tasks, and also open up prospects for solving new, even more labor-intensive tasks, the fulfillment of which until a certain moment was impossible due to insufficient performance of computing systems. One of the successful architectural solutions in the field of multiprocessor computing systems are reconfigurable computing systems (RVS) [1, 2], built on the base of programmable logic integrated circuits (FPGA). Rapid development of RVS is directly related to their ability to achieve high real performance for a wide class of labor-intensive tasks [5, 6], since RVS allows you to program your computing architecture, adapting it under the structure of the current task being solved. An important factor affecting the real performance of the RVS is the choice of the format representing numbers. Thus, the floating-point format is advisable to use for tasks that require high accuracy of calculations and are not so critical to speed of data processing and the FPGA hardware resource used. However, in most cases, the accuracies provided by the fixed-point format is enough to solve a wide range of tasks. Such format allows increase substantially the actual system performance compared to the use of the floating point format and significantly reduce the

number of FPGA hardware resources involved. This is due both to the properties of the format itself with a fixed comma, and to the possibility of using data of variable bit depth at different computational stages, which is typical of DSP tasks. Economy a hardware resource, in turn, may allow additional computational structures to be placed on the free hardware space of the FPGA, increasing the specific system performance. Specific performance in this work will be understood as the ratio of the real performance of the computing system to the expended hardware resource (the number of FPGA logic cells) required to solve the set task [9, 10]. In the tasks of stream processing, the algorithms of the fast Fourier transform (FFT) are widely used, therefore the specific and actual performance of the RVS when solving this class of problems depends on the efficiency of the implementation of the FFT algorithms. Structural implementation of FFT algorithms on RVS for data in a floating-point format does not constitute special problems due to the wide dynamic range and large bitness of the representation of numbers (usually 32 or 64 bits), but leads to low specific performance of computing systems, because of the properties format uses a large number of hardware FPGA resources. The use of the fixed-comma format with structural implementation of FFT algorithms makes it possible to achieve high specific and real performance of computing systems, but can lead to a high error of deductions and errors in the discharge grid overflow. This is due both to the narrow dynamic range of data representation in the fixed-commo format, and with changing capacity of the facts in the process of executing the algorithms. The amount of overflow errors may increase while enhancing the length of FFT and small capacity of program inputs. Elimination of overflow errors in progress arithmetic operations can be carried out in one of two ways: - applying a scaling operation (bit shift), which consists of discarding the least significant digits of the result of an arithmetic operation in order to present it with the required number of digits; - increase in digits for storing the result of an arithmetic operation. Existing methods of FFT implementation, eliminating overflow errors using the scaling operation, do not allow to increase the specific performance of the RVS without a serious loss of calculation accuracy. applying of the way of increasing digits for storing the results of arithmetic operations at the output of each iteration of the FFT avoids errors caused by scaling and, thus, preserves the accuracy of calculations, but leads to a significant growth in the involved FPGA for FFT large dimensions, what is also indesirable. Thus, an urgent task is the development of new methods for creating parallel-conveyor programs with scalable digits, implementing FFT algorithms on the RVS and allowing for high specific performance and acceptable computational accuracy when solving DSP tasks. By scaling a category, we mean a procedure of limited (targeted) increase in the bitness of the results of operations by one category or the coordinated use of a scaling operation (bit shift) for to guarantee computation without overflows and ensure the required accuracy.

Conclusion

RVS-on base FPGA have significant advantages compared in the MWS of traditional architectures, allowing you to customize the computational field of the system under the structure of the algorithm of the problem being solved and to provide higher real performance, close to the peak, in solving computationally labor-intensive and strongly related DSP problems in real time. Close to linear growth performance of the RVS, while increasing in the number of processors in the system, makes it possible to select the hardware for the computational tasks predictably and economically. The use of the fixed-commo data representation format for solving DSP tasks on the RVS significantly increases the specific and real system performance, but requires control on the accuracy of calculations and possible overflows of the discharge grid in conditions of limited and variable bitness of data representation at various computational stages. One of the most used algorithms for solving computationally laborious DSP problems is the FFT algorithm.

References:

1. Guzik, V. F., Kalyaev, I. A., & Levin, I. I. (2016). *Reconfigurable computing systems: a tutorial*. under total ed. I.A. Kalyaeva (Eds.). (p.472). Taganrog: SFU. ISBN 978-5-9275-1918-7.
2. Zotov, V. Y. (2006). *Designing embedded microprocessor systems based on FPGA company Xilinx* [Text]. (p.520). Moscow: Hotline – Telecom. ISBN 5-93517-165-1.

3. Kalyaev, I. A., & Levin, I. I. (2009). *Reconfigurable computing systems with high real performance [Electronic resource]*. Proceedings of the International Scientific Conference "Parallel Computational Technologies" (PaVT'2009). (pp.186-195). Chelyabinsk: SUSU.
4. Dordopulo, A. I., & Levin, I.I. (2008). *Software for solving computationally laborious tasks on reconfigurable computing systems* [Text]. Proceedings of the Second International Scientific Conference "Supercomputer Systems and Their Applications" (SSA'2008), October 27-29, 2008. (pp.50-54). Minsk: UIIP NAS of Belarus.
5. Lyons, R. (2006). *Digital Signal Processing* [Text] Per from English by ed. A.A. Britova. - 2 ed. (p.656). Moscow: Binom-Press. ISBN 5-9518-0149-4 (rus). 171
6. Sergienko, A. B. (2011). *Digital signal processing* [Text]: studies. Manual. - 3rd ed. (p.768). SPb.: BHV-Petersburg. ISBN 978-5-0606-9.
7. Artamonov, D. S., & Putrya, M. G. (n.d.). The method of optimization of the computational process on reconfigurable computing environments. *Information technologies and computing systems. Moscow: ISA RAS, №3*, p. 19-26.
8. Suvorova, E. A., & Sheinin, Y. E. (2003). *Designing digital systems on VHDL*. (p.576). SPb.: BHV-Petersburg. ISBN: 5-94157-189-5.
9. Tanenbaum, E., & Bos, H. (2015). *Modern operating systems.* (p.1120). SPb.: Peter. ISBN: 978-5-496-01395-6.
10. Martens-Atyushev, D. S. (n.d.). *Development of a configurable computing system for digital signal processing*. Technical Sciences - from theory to practice. Materials int. Scientific conference number 11 (47).