Received: July 2, 2019

INASS

International Journal of
Intelligent Engineering & Systems

http://www.inass.org/

A Practical Implementation of Memristor Emulator Circuit Based on Operational Transconductance Amplifiers

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Abstract: As described of electrical circuit have been considering that there are three fundamental passive two-terminal circuit elements; resistor, capacitor, and inductor respectively. In 1971, Prof. L. Chua proposed and described memristor which defines the relationship between magnetic flux and charge. This paper are purposed a memristor emulator circuit based on operational transconductance amplifiers (OTAs). The proposed circuits can be realized using commercially integrated circuits OTA, op amp as AD844, TL084, inductor, capacitor and resistors. The characteristic of memristor emulators can be examined in a practical experiment with the active and passive components. As described, the results could be demonstrated with the memristor circuit application. Furthermore, OTA is used to realize electronically tunable current conveyors emulator circuit. As a result of simulation, the decremental and incremental memristor emulator circuit is suitable for connecting in a series circuit. It was found that the frequency-dependent pinched hysteresis loop of proposed memristor emulator circuits can be updated by changing the value of capacitance and resistance, besides it increases the current gain of current conveyor. In addition to the expected results of memristor (R_M), Memcapacitor (C_M) and meminductor (L_M) are proposed to determine in time-domain characteristics of R-L-C mode circuits. The results of experimental are discussed of phenomena studies by the memory characteristics.

Keywords: Memristor, Emulator circuit, Operational transconductance amplifier (OTA).

1. Introduction

Recently, the memristors are purposed in form of memory-resistor and memristive devices that were presumed to exist when the link was made to voltage-polarity-dependent. The formulation of a memristor was first devised in 1971 by Chua [1] as a fourth circuit on passive elements such as R, L and C respectively. A number of memristor applications has been rapidly reported for digital logic circuits in [2-4] and neural networks in [5, 6].

The memristor emulator circuits based on CMOS differential difference current conveyors (DDCCs) have been proposed in [7] using memristor emulator circuit using two CFOAs, one OTA, three resistors and two capacitors. A multiple-output OTA (MO-OTA) has been used to realize either decremental or incremental memristor emulator circuits in [8].

Memristors offer a nonvolatile memory storage with simple device structure as detailed in [9, 10] including the artificial neural networks as synaptic weights with a pulse based memristor circuit [2], memristor XOR gate for resistive multiplier [3] and phase shift keying modulators based memristor [4].

Table 1. Comparison of the proposed circuit with those of some previous works

Circuits	No. of active components	No. of passive components	Decremental/Incremental
Proposed circuit Fig. 5	1-EDDCC (3-LM13600), 1-AD633	2-R, 1-C	Decremental
Fig. 6	1-EDDCC (3-LM13600), 1-AD633	2-R, 1-C	Incremental
Ref. [16] (2017)	1-CCTA	3-R, 1-C, 1-SW	Both
Ref. [17] (2017)	1-DVCCTA	3-R, 1-C, 1-SW	Both
Ref. [18] (2018)	7-MOS	1-C	Decremental
Ref. [19] (2015)	3-ECCII (6-LM13600), 1-AD633	1-R, 1-C	Decremental

Many types of mixed-mode circuits have been studied such as differential voltage current conveyors (DVCCs), second-generation current conveyors (CCIIs), current controlled current conveyors (CCCIIs), DDCCs and OTAs [11]. Based on the light-dependent resistor (LDR), a memcapacitor emulator has been presented using R_M-C_M converter and a method is used to satisfy a LDR memristor-based meminductor-equivalent circuit detailed in [12].

The modern active devices have been used to realize memristor emulator circuits such as current conveyor transconductance amplifier (CCTA) in [16], differential voltage current conveyor transconductance amplifier (DVCCTA) in [17]. The circuits in [17] provide decremental and incremental memristor emulators into one circuit by selecting the switch. The circuit in [16] is simulated using CMOS implementation of CCTA while the circuit in [17] is simulated using CMOS implementation of DVCCTA whereas experiment tests, these circuits have been built using commercially available ICs AD844 and CA3080. The circuit in [18] realizes memristor emulator circuit based on MOSFET-C.

The comparison of proposed circuits with those previous works are summarized in Table 1. Compared with [16-18], the proposed circuits can be pushed the operating of high frequency by capacitance, resistance and current gain of current conveyor, compared with [16, 18, 19], the proposed circuits in Figs. 5 and 6 provide decremental and incremental memristor emulators into single circuit and compared with [16, 17], the proposed circuits can be tested both simulation and experiment with the same active and passive components.

In this paper, we introduce a compact circuit model and physical hardware emulation for memristor using the electronically tunable differential different current conveyor (EDDCC). The hardware emulator will demonstrate experimentally memristor dynamics.

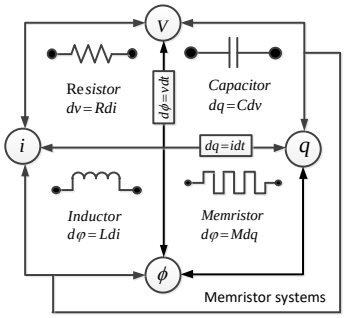

Figure.1 Four fundamental two-terminal circuit elements: resistor, capacitor, inductor and memristor [22]

This paper is organized as follows. The definitions and concept of memristor model is introduced in Section 2 and Section 3 is described about OTA-based ECCII. We present an OTA-based EDDCC memristor emulator that is similar to that of a memristor shown in Section 4. Experimental results and conclusion are given in Section 5 and 6, respectively.

2. Memristor model

Following [13], there are four fundamental circuit variables: electric current *i*, voltage *v*, charge *q* and magnetic flux φ described in Fig.1. The memristor, with memristance *M*-provides a functional relation between charge and flux, $d\varphi=Mdq$. Basic mathematical definition of a current-controlled memristor for circuit analysis is given by $v = R(w)i$ and $\frac{dw}{dt}$(i), where *w* is the state variable and *R* is a generalized resistance.

The concept of memristive systems is described as $v = R(w, i)$ and $\frac{dw}{dt}(i)$ where f is function of time.

A thin semiconductor film of thickness D sandwiched between two metal contacts is considered in Fig. 2. The total resistance is assigned with 2-variable resistors connected in series, where the resistances are given for the full length *D* of the

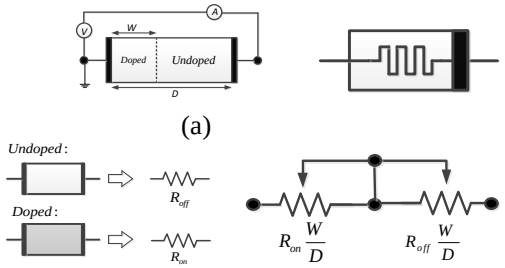

Figure.2 Coupled variable-resistor model for a memristor: (a) structure and symbol of the memristor and (b) diagram with a simplified equivalent circuit

device. However, the semiconductor film has a region with a high concentration of dopants having low resistance R_{on}. The remainder closes to essentially zero dopant concentration with higher resistance R_{off}. An external bias $v(t)$ across the device will move the boundary between the two regions causing the charged dopants to drift, we get

$$v(t) = \left\{R_{on}\frac{w(i)}{D} + R_{off}\left(1 - \frac{w(i)}{D}\right)\right\} i(t) \quad (1)$$

$$\frac{dw(t)}{dt} = \mu\frac{R_{on}}{D} i(t) \quad (2)$$

and $w(t)$ is given as

$$w(t) = \mu_v\frac{R_{on}}{D} q(t) \quad (3)$$

By substituting Eq. (3) into Eq. (1), the memristance for $R_{ON} = R_{OFF}$ can be expressed as

$$M(g) = R_{off}\left(1 - \frac{\mu_v R_{on}}{D^2}\right) q(t) \quad (4)$$

where the term of q-dependent is the crucial support to the memristance. It becomes larger with higher dopant mobilities μ_V and smaller semiconductor film thicknesses D, respectively.

3. OTA-based electronically tunable second-generation current conveyor (ECCII)

OTA is important active device that has been used to realize both voltage- and current-mode analog circuits. OTA-based circuits can be tested both simulation and breadboard experiment. Symbol of OTA is shown in Fig.3. The ideal OTA is described by $I_0 = g_m(V_1 - V_2)$, where is the output current, g_m is the transconductance gain, V_1 and V_2 denote respectively the non-inverting and inverting input voltages. The transconductance g_m of OTA can be controlled using external bias current.

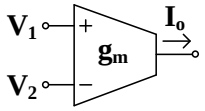

Figure. 3 Circuit symbol of OTA

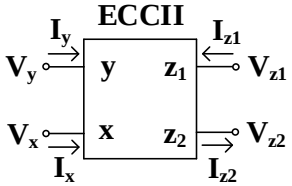

Figure.4 Symbol of ECCII

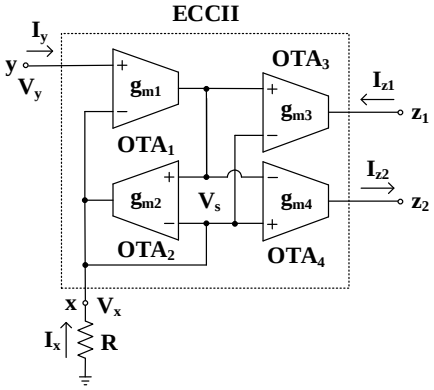

Figure. 5 OTA implementation for ECCII

The symbol of the ECCII is shown in Fig. 4 and its ideal characteristics can be described by

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \mp k & 0 \end{bmatrix} \begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} \quad (5)$$

ECCII has a unity voltage gain between terminals y and x and has current gain k between terminals z and z. OTA implementation for ECCII can be shown in Fig. 5. Using nodal analysis, the relation between V_x and V_y can be expressed as

$$V_x = \frac{g_{m1}g_{m2}\gamma_{in}R}{1+g_{m1}g_{m2}\gamma_{in}R} V_y \quad (6)$$

where g_{m1} and g_{m2} are respectively the transconductance gains of OTA_1 and OTA_2, R is the given resistor and rin is the small-signal input resistance of OTA_2.

4. OTA-based electronically tunable differential different current conveyor (EDDCC)

The part relationship of EDDCC is shown in Fig. 6 which is given as

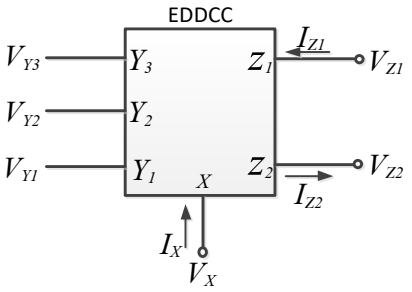

Figure.6 Circuit symbol of EDDCC

$$\begin{bmatrix} V_x \\ I_{y1} \\ I_{y2} \\ I_{y3} \\ I_{z1} \\ I_{z2} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & k_1 \\ 0 & 0 & 0 & -k_2 \end{bmatrix} \cdot \begin{bmatrix} V_{y1} \\ V_{y2} \\ V_{y3} \\ I_x \end{bmatrix} \quad (7)$$

where g_m is transconductance of EDDCC.

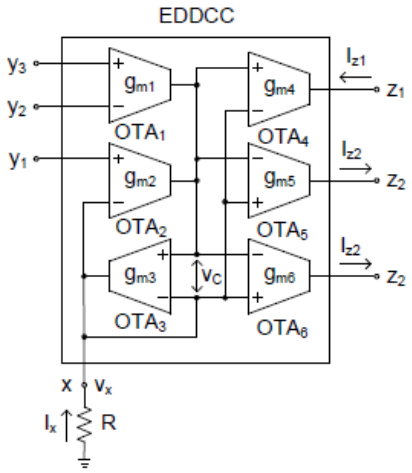

Figure. 7 Symbol of developed EDDCC

OTA implementation for EDDCC based on CMOS is depicted in Fig. 7. The OTA_1 to OTA_3 are used to provide a differential difference amplifier (DDA). By using nodal analysis, the relation of voltages V_x, V_{y1}, V_{y2} and V_{y3} can be expressed by

$$V_y = \frac{(g_{m2}g_{m3}\gamma_{in}R)V_{y1} - (g_{m1}g_{m3}\gamma_{in}R)V_{y2} + (g_{m1}g_{m3}\gamma_{in}R)V_{y3}}{1 + (g_{m3}R + g_{m2}R + g_{m3}\gamma_{in}R)} \quad (8)$$

where g_{mi} is the gain of transconductance of $OTA_{i,}$, R is the defined resistor and r_{in} is input resistor in case of small signal of OTA_3 which has highly resistance. Relationship between Vx, Y_1, Y_2, and Y_3 Ports for EDDCC is given as

$$V_x \approx V_{y1} - V_{y2} + V_{y3} \quad (9)$$

From Fig. 7, we assume the current I_x is equal to output current of OTA_3 which is given as

$$I_x = g_{m3}(V_C - V_x) \quad (10)$$

$$I_{Z1} = g_{m4}(V_C - V_x) \quad (11)$$

$$I_{Z2} = g_{m5}(V_x - V_C) \quad (12)$$

Substituting this equations

$$V_C - V_x = \frac{I_{Z1}}{g_{m4}} \quad (13)$$

$$V_C - V_x = \frac{I_{Z2}}{g_{m5}} \quad (14)$$

into this equation

$$V_C - V_x = \frac{I_x}{g_{m3}} \quad (15)$$

Then, we can rewrite I_{z1} and I_{z2} as

$$I_{Z1} = \left(\frac{g_{m4}}{g_{m3}}\right) I_x = k_1 I_x \quad (16)$$

$$I_{Z1} = \left(\frac{g_{m5}}{g_{m3}}\right) I_x = k_2 I_x \quad (17)$$

It is noted that k_1 and k_2 are the current gain of EDDCC controlled by g_{m4} and g_{m5}. Current gain of I_{z1} and I_{z2} is amplified by k_1 and k_2 that is different from the ordinary DDCC. Hence, the gain k_1 and k_2 are independently controlled.

The multi-output EDDCC can simply create by increasing plus-type of EDDCC, when the increased parallel input of OTA is connected to OTA_4. If minus-type EDDCC is increased, the parallel input of OTA will increase by connecting with OTA_5.

Relationship of voltage and current is given as

$$V(t) = \left\{\left(R_{on}\frac{w(t)}{D}\right) + R_{off}\left(1 - \frac{w(t)}{D}\right)\right\} i(t) \quad (18)$$

where D and W are the thick of sandwiched area and doped area in memristor. R_{on} and R_{off} are the resistance on the concentrated area of high and low doped. Memristor emulator circuits are proposed in Figs. 8 and 9 with 2-resistor, 1-capacitor and 1-analog multiplier which are used the concept followed in [17].

By using the nodal analysis, we get

$$V_m = i_m R_1 + V_x \quad (19)$$

$$V_C = \frac{k_2}{R_1 C_1}\int_0^1 v_m(\tau)d\tau \quad (20)$$

$$V_R = -k_1 R_2 + I_m \quad (21)$$

Following the characteristic of input/output of AD844, the voltage V_{mul} is given as

$$V_{mul} = -i_m \frac{k_1 k_2 R_2}{10 R_1 C_1}\int_0^t v_m(\tau)d\tau \quad (22)$$

Using the input properties of DDCC is given as

$$V_x = V_{y1} - V_{y2} + V_{Y3} \quad (23)$$

$$V_m = i_m R_1 - \left(i_m \frac{k_1 k_2 R_2}{10 R_1 C_1}\int_0^1 V_m(\tau)d\tau\right) + V_{sum} \quad (24)$$

From Eq.(22), we assume V_{sum} is equal to zero and flux $\phi_m(t)$ is defined by

$$\phi_m(t) = \int_0^1 V_m(t)dt \quad (25)$$

Then, Eq. (22) can rewrite as

$$\frac{V_m}{i_m} = R_1 - \left(\frac{k_1 k_2 R_2}{10 R_1 C_1}\phi_m(t)\right) = M(\phi(t)) \quad (26)$$

where $M(\phi(t))$ is the resistance of memristor that is used k_1 and k_2 to compensate the attenuation rate constant at 1/10 from multiplier circuit. Moreover, it can compensate the effect from frequency that affect to pinched hysteresis loop behavior of memristor.

From Figs. 8 and 9, the DC voltage V_{off1}, V_{off2}, V_{off3} are the bias current to improve the pinched hysteresis loop behavior, when the characteristic is distorted. Voltage V_{off1} and V_{off2} is applied to adjust the symmetry between the positive and negative of pinched hysteresis loop and then V_{off3} is defined to tune the zero-crossing of pinched hysteresis loop.

We assume that $v_{in}(t) = v_p \sin(\omega t)$ is the input of Fig. 8, where $\omega = 2\pi f$ and V_p is the amplitude of voltage signal. Then we define

$$\phi_m(t) = -\left(\frac{V_p}{\omega}\right)\cos(\omega t) = \left(\frac{V_p}{\omega}\right)\cos(\omega - t) \quad (27)$$

and substitute $\phi_m(t)$ in Eq.(30), the memristance is given as

$$M(\phi_m(t)) = R_1 - \left(\frac{k_1 k_2 R_2}{10 R_1 \omega C_2}\cos(\omega t - \pi)\right) \quad (28)$$

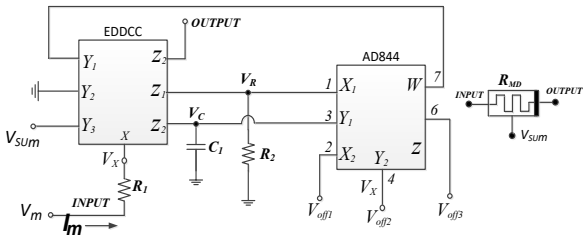

Figure. 8 Emulator circuit symbol of decremental EDDCC memristor and equivalent circuit

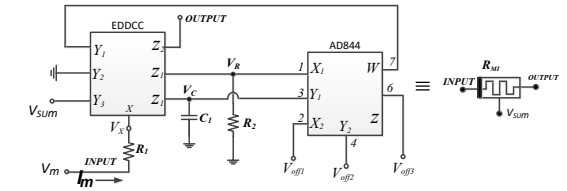

Figure.9 Emulator circuit symbol of incremental EDDCC memristor and equivalent circuit

From Eq.(28), the memristance consists of linear time-variant and linear time-invariant resistors. If the frequency increases, the linear time-invariant resistor will decrease. That mean the dependent frequency is pinched the hysteresis loop, when the frequency is increased. At the fix time, the linear time-variant resistor is updated by frequency that will update this circuit by adjusting k_1 and k_2, respectively.

5. Simulation results

In order to investigate the operation of the proposed memristor emulator circuits, the circuits of Figs. 7 to 9 were simulated using PSPICE simulations. ECCII in Fig. 3 and EDDCC in Fig. 5 were implemented using commercially available IC LM13600N [57]. A commercially available IC AD844J [56] was used for voltage multiplier.

Table 2. Summarized performances of ECCII and EDDCC

Parameters	Value
Supply voltage	±10 V
OTA	LM13600N
V_x/V_y and V_x/V_{y1} (no load)	-0.9 V to 0.9 V
V_x/V_{y2} and V_x/V_{y3} (no load)	-0.1 V to 0.1 V
-3dB bandwidth (V_x/V_{yi}); i = 1, 2, 3	7.3 MHz
-3dB bandwidth (I_z/I_x)	11 MHz
R_{yi}: C_{yi}; i = 1, 2, 3	185 kΩ: 8.4 pF
R_x: L_x	17 Ω: 24 μH
R_z: C_z	22 kΩ: 6.12 pF

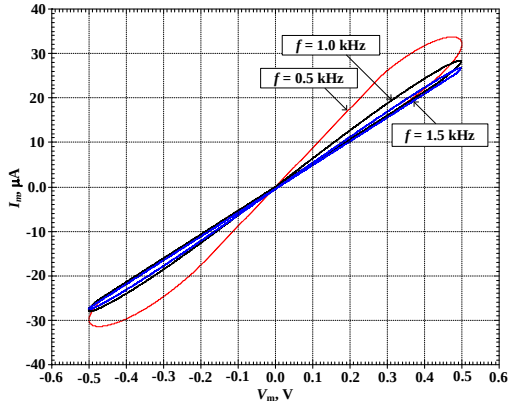

Figure.10 Simulated frequency dependent pinched hysteresis loop of memristor emulator at current gain k_1 = k_2 = 1 and different frequencies

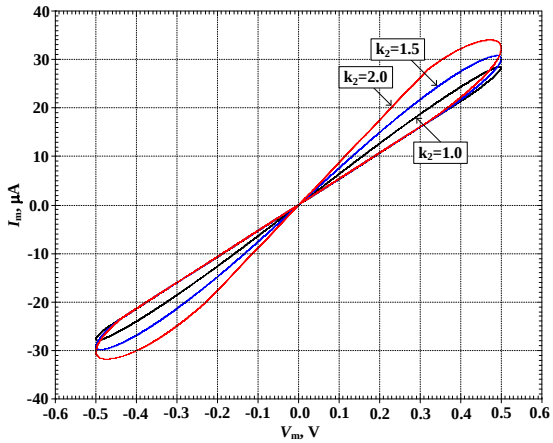

Figure.11 Simulated frequency dependent pinched hysteresis loop of memristor emulator at f = 1 kHz and k_1 = 1 with different current gains k_2

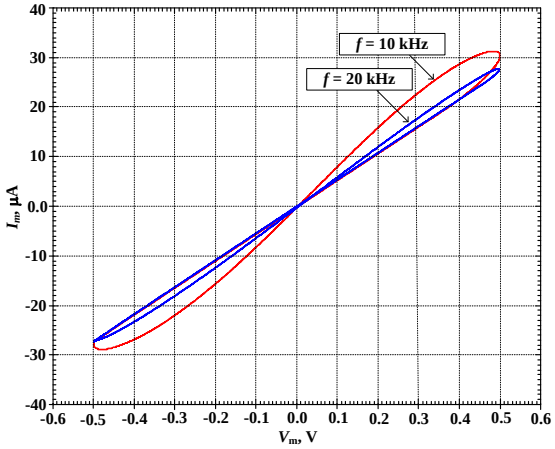

Figure.12 Simulated frequency dependent pinched hysteresis loop of memristor emulator at k_1 = 1 and k_2 = 20 with frequency of 10 and 20 kHz

The commercially available IC LM13600N was supplied by the DC supply voltages of ±10 V while OTA_1, OTA_2 for ECCII in Fig. 3 and OTA_1, OTA_2, OTA_3 for EDDCC in Fig. 5 were biased by the DC current sources of 50 μA. The simulated performances of the ECCII and EDDCC were shown in Table 2.

The proposed decremental memristor emulator circuits in Figs. 8 and 9 were simulated. The values of resistances and capacitance were given as R_1=15 kΩ, R_2=5 kΩ and C_1=1 nF. In case to simulate the proposed incremental memristor emulator circuits in Fig.8, the low resistance value such as R_1=5 kΩ should be used. The DC voltages V_{off1}, V_{off2}, and V_{off3} in Fig.9 were given as 26 mV, 0 V and –50 mV, respectively, and current gain k_1 was fixed as 1 (k_1 = 1).

Fig. 10 shows the simulated frequency-dependent pinched hysteresis loop in voltage-current relationship corresponding to $v_m(t)$ versus $i_m(t)$ plane for the frequencies of 0.5, 1.0 and 1.5 kHz with amplitude of applied signal 0.5 V (peak) constant and the current gain k_2 was 1. This result was confirmed that when amplitude of applied signal and capacitance-value constants, the proposed memristir emulator circuit depends on the frequency of the exciting source.

Fig. 11 shows the simulated frequency-dependent pinched hysteresis loop in voltage-current relationship corresponding to $v_m(t)$ versus $i_m(t)$ plane for the current gains k_2 of 1.0, 1.5 and 2.0 while the frequency of 1 kHz with amplitude of applied signal 0.5 V (peak) constants. This result was confirmed that the frequency-dependent pinched hysteresis loop in voltage-current relationship of the proposed circuits can also be controlled by adjusting current gains of current conveyor.

To confirm Eq. (17) that by increasing the current gain of current conveyor, the pinched hysteresis loop behavior of proposed memristor emulator circuit can be pushed for operating at higher frequency. Fig. 12 shows the simulated frequency-dependent pinched hysteresis loop in voltage-current relationship corresponding to $v_m(t)$ versus $i_m(t)$ plane for the current gain k_2 = 20. In this case, the frequencies of the exciting source of 10 kHz and 20 kHz at amplitude of 0.5 V (peak) were applied and value of capacitance C_1 is constant. In this result, the voltages V_{off1} = 48 mV and V_{off3} = –40 mV were used to obtain perfect the pinched hysteresis loop behavior.

The proposed decremental memristor emulator circuit in Fig. 8 was and simulated. The values of resistances and capacitance were similar to the simulation in Fig. 8 The circuit was design as k_1 = k_2 = 1. Fig. 13 shows simulated frequency-dependent

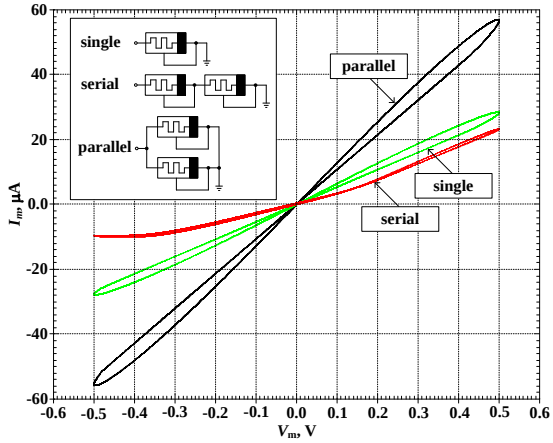

Figure.13 Simulated pinched hysteresis loop of memristor at 1 kHz frequency with series and parallel connection

pinched hysteresis loop in voltage-current relationship corresponding to $v_m(t)$ versus $i_m(t)$ plane for the frequency of 1 kHz with amplitude of applied signal 0.5 V (peak) constant. This result was confirmed that proposed circuit in Fig. 9 can be applied to connection in serial and in parallel.

6. Circuit implementation of R_M-C_M and R_M-L_M convertor

Following [14], the memcapacitor and meminductor emulators are constructed using AD844 shown in R_M-C_M convertor in Fig. 14. Relationship of v_{CM} and v_{RM} is give as $v_{RM} = v_{CM}$. Then, OTA formed by AD844 to produce the current i_{RM} is given as

$$iR_M = \left(\frac{1}{RC}\right)\int iC_M dt \tag{29}$$

Memcapacitance from R_M-C_M is defined as

$$C_M = \frac{d\sigma C_M}{d\phi C_M} = \frac{RC}{R_M} \tag{30}$$

Fig. 15 depicts the R_M-L_M convertor, when v_X=x_Y, v_Z=v_{output}, i_Z = i_X that is used for R_M-L_M convertor. The current through the equivalent meminductor i_{LM} is defined as

$$i_{LM} = \frac{(0-V_x)}{R_1}, \quad i_{RM} = \frac{(0-V_y)}{R_3} \tag{31}$$

Then, the relationship of v_{LM} and v_{RM} as

$$v_{LM} = v_Z = v_{y'} = v_{x'} \tag{32}$$

$$v_{RM} = \frac{1}{R_2C_2}\int v_{LM} dt \tag{33}$$

Therefore, the meminductance is obtained from R_M-L_M converter as

$$L_M = \frac{d\sigma C_M}{dqL_M} = \frac{R_1R_2R_3}{R_1R_M} \tag{34}$$

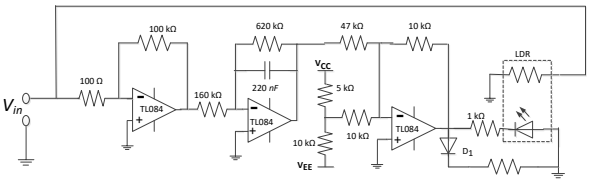

Figure.14 Schematic of proposed R_M-C_M circuit

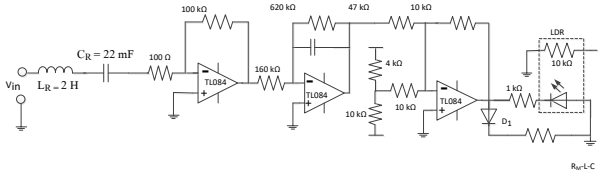

Figure.15 Schematic of proposed R_M-L-C circuit

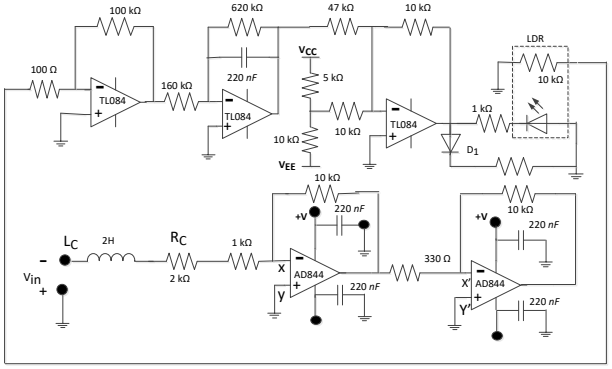

Figure.16 Schematic of proposed R-L-C_M circuit

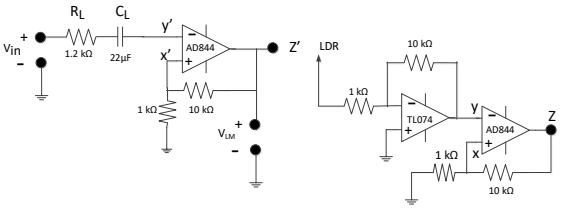

Figure. 17 Schematic of proposed R-L_M-C circuit

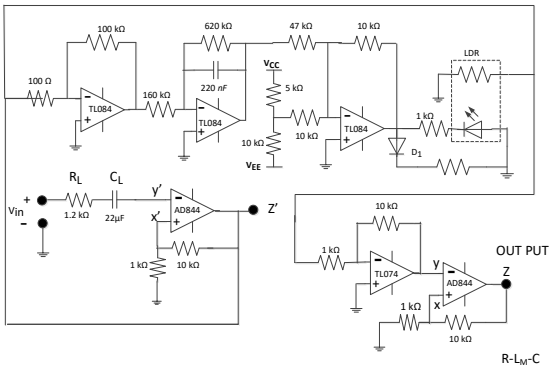

Figure.18 Schematic of proposed R-L_M-C circuit

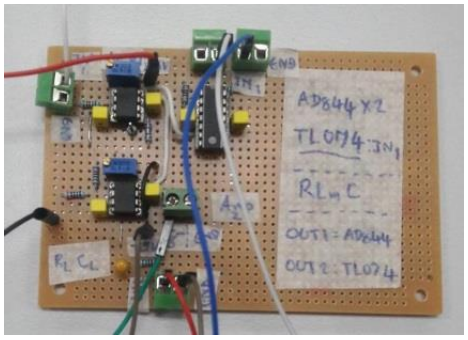

Figure.19 Physical implementation of R-L_M-C circuit from schematic shown in Fig. 18

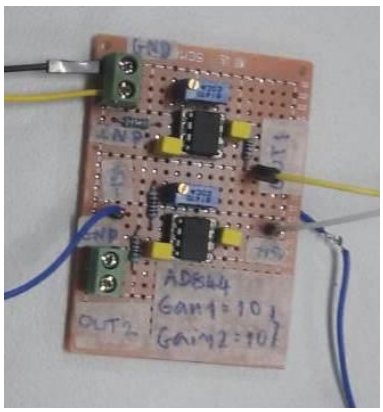

Figure.20 Physical implementation of R-L-C_M circuit is used schematic of proposed R_M-C_M circuit in Fig.14

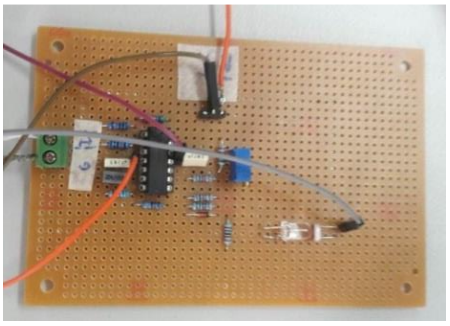

Figure.21 Experimental setup of LDR circuit is used schematic of proposed R-L-C_M circuit in Fig. 16

7. Experimental results for characteristics of R_M-L-C and R-L_M-C circuits

We consider the design of equivalent circuit for RLC-mode circuit in the R_M-L-C and R-L_M-C circuits shown in Figs. 17-18, respectively. Experimental setup for LDR circuit used is depicted in Fig. 21.

6.1 Experiment of R_M-L-C circuit

Design of R_M-L-C circuit using LDR-based memristor-equivalent circuit shown in Fig. 15.

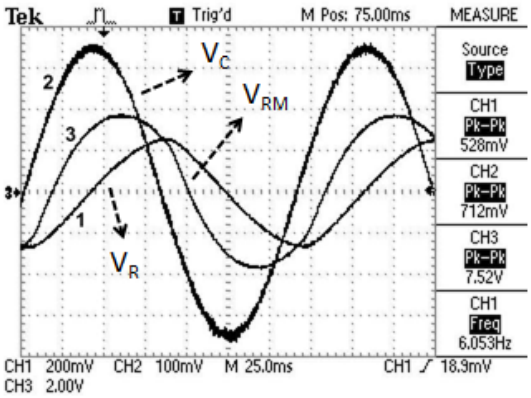

Figure.22 Experimental result v_{RM}, v_{CR}, v_{LR} of R_M-L-C circuit at f = 6 Hz, v_{in} = 2 V

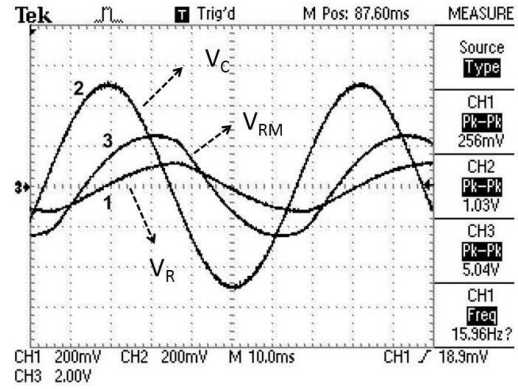

Figure.23 Experimental result v_{RM}, v_{CR}, v_{LR} of R_M-L-C_M circuit at f = 16 Hz, v_{in} = 2 V

From the experiment setup of R_M-L-C_M circuit are performed at 6 Hz and 16 Hz for v_{in} 2 V sinusoidal signal of input voltage shown in Figs. 22 and 23. The voltage v_{CR} across the capacitor C_R, voltage v_{LR} across the capacitor L_R, and voltage v_{RM} across the memristor for the given frequencies can be seen that v_{RM} is ahead of v_{CR} and v_{RM} lags behind v_{LR}. These results demonstrate that LDR-memristor equivalent circuit can be occupied both the memristor circuit and memory-less resistor characteristics.

6.2 Experiment of R-L_M-C circuit

Design of R-L_M-C circuit using LDR-based memristor-equivalent circuit is shown in Fig. 17.

The experiment setup of R-L_M-C circuit are performed at 16 Hz and 30 Hz for 2 V sinusoidal signal of input voltage shown in Figs. 24 and 25. The voltage v_{CR}, voltage v_{LR} , and voltage v_{RM} for the given frequencies can be realized that v_{RM} is ahead of v_{CR} and v_{RM} lags behind v_{LR}

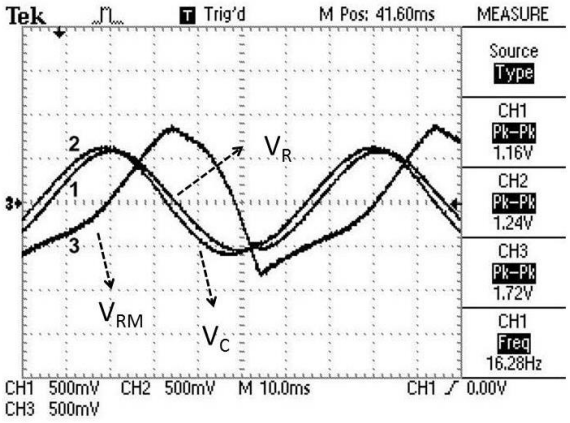

Figure.24 Experimental result v_{RM}, v_{CR}, v_{LR} of *R-L*$_M$*-C* circuit at f = 16 Hz, v_{in} = 2 V

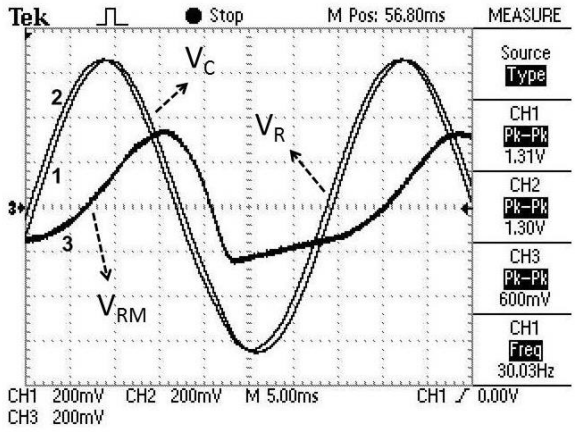

Figure.25 Experimental result v_{RM}, v_{CR}, v_{LR} of *R-L*$_M$*-C* circuit at f = 30 Hz, v_{in} = 2 V

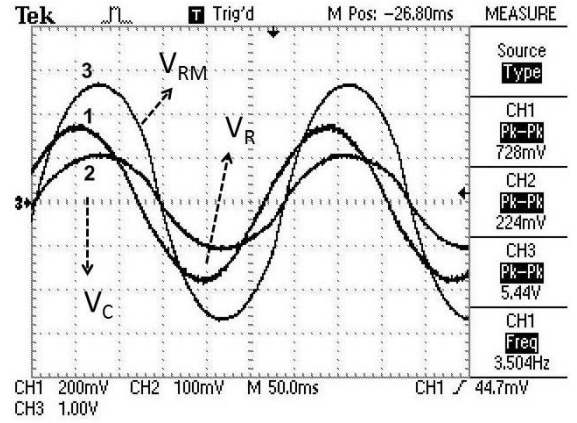

Figure. 26 Experimental result v_{RM} v_{CR}, v_{LR} of *R-L*$_M$*-C* circuit at f = 3.5 Hz, v_{in} = 2 V

6.3 Experiment of *R-L-C*$_M$ circuit

Design of *R-L-C*$_M$ circuit using LDR-based memristor-equivalent circuit is shown in Fig. 18.

The memory characteristics of the memristor V_{RM} are not normal sinusodial waveform shown in Figs. 26 and 27. This mechanism are mainly of non-

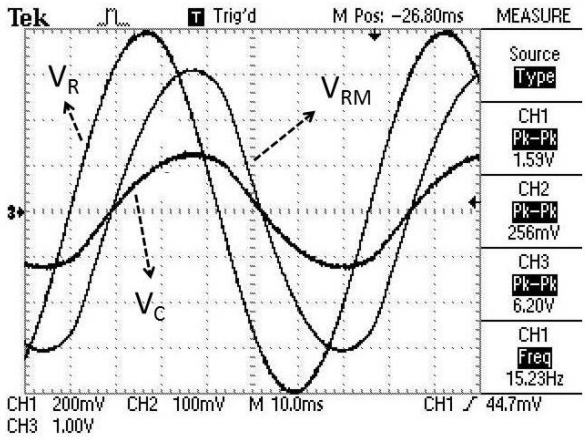

Figure. 27 Experimental result v_{RM}, v_{CR}, v_{LR} of *R-L*$_M$*-C* circuit at f = 15 Hz, v_{in} = 2 V

linear characteristics of memristor. Futhermore, the measurement phase relation is obtained at low frequency of sinusoidal, which is applied to a memristor device. After that the frequency are increases, then the phase shift is very narrow until it becomes as a line.

8. Conclusion

We have proposed the memristor emulator circuits based on commercially available ICs as AD844, TL074, TL084, resistors, inductors and capacitors. OTA has been used to realize ECCII and EDDCC, which are the important active element. Proposed emulator circuits with memresitive-element-equivalent circuits have been simulated by PSPICE simulator and circuit board is used for experiment tests. RLC-mode circuits are studied including with memristor, memcapacitor and meminductor. In the practical experiments, the proposed memcapacitor and meminductor circuits based on the LDR memristor-equivalent circuit can be verified that the experimental results are agreed with the proposed theory.

Acknowledgments

This work was supported by Rajamangala University of Technology Phra Nakhon.

References

[1] L. O. Chua, "Memristor-The Missing Circuit element", *IEEE Transactions Circuit Theory*, Vol. CT-18, pp. 507-511, 1971.

[2] H. Kim, M. P. Sah, C. Yang, T. Roska, and L. O. Chua, "Neural Synaptic Weighting with a Pulse-based Memristor Circuit", *IEEE Transactions on Circuits and System-I: Regular Papers*, Vol. 59, pp. 148-158, 2012.

[3] S. Shin, K. Kim, and S.M. Kang, "Memistor XOR for Resistive Multiplier", *Electronics Letters*, Vol. 48, pp. 78-80, 2012.
[4] I. C. Goknar, F. Oncul, and E. Minayi, "New Memristor Applications: AM, ASK, FSK, and BPSK Modulators", *IEEE Antennas and Propagation Magazine*, Vol. 55, pp. 304-313, 2013.
[5] X. Y. Wang, A. L. Fitch, H. H. C. Lu, and W. G. Qi, "Design of a Memcapacitor Emulator based on a Memristor", *Physics Letters A*, Vol. 376, pp. 394-399, 2012.
[6] D. Yu, H. H. C Iu, A. L. Fitch, and L. Yan, "A Floating Memristor Emulator based Relaxation Oscillator", *IEEE Transactions on Circuits and Systems- I: Regular Papers*, pp. 2888–2896, 2014.
[7] T. Abuelma'atti and Z. I. Khalifa, "A Continuous-Level Memristor Emulator and Its Application in a Multivibrator Circuit", *International Journal of Electronics and Communications*, Vol. 69, pp. 771-775, 2015.
[8] Y. Babacan, A. Yesil, and F. Kacar, "Memristor Emulator with Tunable Characteristic and Its Experimental Results", *International Journal of Electronics and Communications*, Vol. 81, pp. 99–104, 2017.
[9] S. Shin, K. Kim, and S. M. Kang, "Memristor Applications for Programmable Analog ICs", *IEEE Transactions on Nanotechnology*, Vol. 10, pp. 266-274, 2011.
[10] W. D. Jemison, "Variable Gain Amplifier Circuit using Titanium Dioxide Memristors", *IET Circuit Devices and System*, pp. 59-65, 2011.
[11] C. N. Lee, "Multiple-mode OTA-C Universal Biquad Filters", *Circuits System Signal Processing*, Vol. 29, pp. 263–274, 2010.
[12] X. Y. Wang, A. L. Fitch, H. H. C. Iu, V. Sreeram, and W. G. Qi, "Design of a Memcapacitor Emulator based on Memristor", *Physic Letter A*, Vol. 396, pp. 394–399, 2012.
[13] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The Missing Memristor Found", *Nature*, Vol. 453, pp. 80-83, 2008.
[14] H. Kim, M. P. Sah, Y. Changju, S. Cho, and L. O Chua, "Memristor Emulator for Memristor Circuit Applications", *IEEE Transactions on Circuits and Systems I: Regular Papers*, pp. 2422-2431, 2012.
[15] Y. Liang, H. Chen, and D. S. Yu, "A Practical Implementation of a Floating Memristor-less Meminductor Emulator", *IEEE Transactions on Circuits and System-II: Express Briefs*, Vol. 61, pp. 299-303, 2014.
[16] R. K. Ranjan, N. Rani, R.Pal, S. K. Paul, and G. Kanyal, "Single CCTA based High Frequency Floating and Grounded Type of Incremental/Decremental Memristor Emulator and Its Application", *Microelectronics Journal*, Vol. 60, pp. 119-128, 2017.
[17] R. K. Ranjan, N. Raj, N. Bhuwal, and F. Khateb, "Single DVCCTA based High Frequency Incremental/Decremental Memristor Emulator and Its Application", *International Journal of Electronics and Communications*, Vol. 82, pp. 177-190, 2017.
[18] A. Yesil, "A New Grounded Memristor Emulator based on MOSFET-C", *International Journal of Electronics and Communications*, Vol. 91, pp. 143-149, 2018.
[19] M. Kumngern, "A Floating Memristor Emulator Circuit using Operational Transconductance Amplifiers", In: *Proc. of IEEE Conference on Electron Devices and Solid-State Circuits*, 2015.