Received: May 31, 2019

INASS

International Journal of
Intelligent Engineering & Systems

http://www.inass.org/

Automatic Resonance-Frequency Tuning and Tracking Technique for a 1MHz Ultrasonic-Piezoelectric-Transducer Driving Circuit in Medical Therapeutic Applications Using dsPIC Microcontroller and PLL Techniques

Suttipong Boontaklang[1] **Chow Chompoo-Inwai**[1]*

[1] *Electrical Engineering Department, Faculty of Engineering,*
King Mongkut's Institute of Technology Ladkrabang, Bangkok, Thailand, 10520
* Corresponding author's Email: chow.ch@kmitl.ac.th

Abstract: Driving ultrasonic piezoelectric transducer (UPZT) at maximum performance in real-time operations is a very challenging task due to the deterioration problem of ultrasound output causing by human-skin impedance fluctuations. This paper proposed ideas and solutions on how to maximize the UPZT driving circuit performance in or deter to solve the deterioration problem. A newly-designed feedback control block with a phase-locked-loop (PLL) technique controlled by microcontroller has been added to the conventional UPZT driving circuit to ensure the automatic resonance frequency tuning and tracking capabilities. After intensive experiments, it is clear that the proposed technique works flawlessly and much more efficient compared to the conventional one. The experimental results also confirm that the percentage of error in tuning to the desired frequency is less than ±0.2% and the speed of tuning convergence time is between 9-12 milliseconds on average.

Keywords: Ultrasonic piezoelectric transducer, Resonance frequency, Automatic-tuning resonance frequency, Class-F power amplifier, Phase-locked-loop technique, PLL, Tracking capability.

1. Introduction

Ultrasound or ultrasonic wave has long been used in many industrial businesses [1-7] including the medical applications [8-10]. The key device to generate the ultrasound wave is called ultrasonic piezoelectric transducer (UPZT). Hypothetically, the UPZT converts electrical real power into mechanical motion or ultrasound wave/power; however, some energy could easily be dissipated or deteriorated due to the reactive elements of the UPZT itself. Therefore, for a high-efficiency system, the UPZT must be driven in the correct resonant mode to minimized its reactive power and realize maximum power transfer (MPT) [9, 11]. In practice, it is often found that the resonance frequency of each UPZT will be different. It is common to see from a manufacturing specifications that the recommended resonance frequency for each UPZT would come with tolerances e.g., 1 MHz±5.0% or 1 MHz±10%. A little deviation in driving frequencies from recommended specifications definitely results in some deterioration of ultrasound power outputs.

The first and main challenge is to generate the ultrasound power from any UPZT in the desired resonant mode with high electrical efficiency. There currently are various methods to drive the UPZT in resonant mode. As of today, the most popular UPZT driving circuits/techniques could be categorized into either power factor correction (PFC) based [2, 8] or the phase-locked loop (PLL) based solutions [1, 3-4, 12]. It is PFC-based driving circuits that usually require additional reactive components with some kinds of complicated compensation to minimize the reactive part of the UPZT impedance and thus put the UPZT into resonance. On the other hand, the PLL-based driving circuit usually feed current into UPZT of interest through a closed-loop system. However, most of the PLL-based driving circuits shared the similar drawback i.e. a limited locked-in range and also this type of circuits still requires a complex compensation to ensure the stability and

reliability of the UPZT driving systems under variations on large loading conditions [12].

The second challenge is that any UPZT has multiple resonant modes, which could be shifted anytime when the connected load varies. For this matter, a good driving circuit should be able to always tune-in or track the desired UPZT resonant mode and not fall into other undesired resonant frequencies. Therefore, having any kind of complex frequency or phase discriminator for driving circuits is crucial [13].

The third challenge is to precisely control the amplitude of the UPZT displacement and ensure proper mechanical or ultrasound output functions. The electrical power directly delivered to the UPZT must be precisely regulated and controlled. Various solutions for this challenge have been proposed with different ideas, for example, a burst-mode control [14], a zero-voltage-switching [15], a dual current-mode control [10] and also a sepic-based converter with pulse width modulation (PWM) technique [8].

This research proposes a novel technique to cover up all of the three aforementioned challenges. This work utilizes a PLL-based solution with a newly-designed feedback control system in order that the limited locked-in range problem could easily be expanded on any changing load conditions for the first challenge. The phase comparators, a high-speed microcontroller and other components of this proposed feedback control system have been integrated and implemented to ensure the reliability and stability in the second challenge performance enhancing. For the third challenge, an already-proven sepic-based PWM converter with class-F amplifier driving circuit from authors' previous work mentioned in [8] has been utilized here. Both sepic-converter and class-F amplifier control signals will be precisely gathered and recomputed by the newly-proposed feedback control technique. The experimental results and discussions from this paper clearly confirm the improvements in overall UPZT driving system performances and efficiencies.

The organizations of this paper are as follows: the first section is an introduction explaining the background problems and significance of this work, the second section presents the related theories i.e., UPZT equivalent circuits, equations and a brief of UPZT frequency response in different situations, the third section illustrates the ideas, conceptual design and a system overview of the proposed UPZT driving circuit with automatic-tuning resonance frequency technique, the fourth section thoroughly explains the in-depth details on how to design and implement each of the key components in the proposed feedback control system and also how each of them works, the fifth section presents the experimental results to validate many aspects of the newly-designed technique and discussions, and in the last section, the conclusion will be made.

2. Related theories

The equivalent circuit of any UPZT at resonance frequencies is illustrated in Fig. 1. It consists of an electrical arm and a mechanical arm [1-2, 8, 9]. The electrical arm has only two components: a static capacitance C_0 and a static dielectric loss R_0. The mechanical arm is a series of RLC circuit that composes by a dynamic capacitance C_1, a dynamic inductance L_1 and a dynamic resistance R_1. In general, both arms are connected in parallel and R_0 has bigger value than other parallel components; therefore, it is assumed to be neglected [5-6, 16].

From the equivalent circuit shown in Fig. 1, the admittance Y of any UPZT can be written as in Eq. (1) and Eq. (2), [5-6, 8, 16], where ω is the angular frequency (rad/sec)

$$Y = G + Bj \tag{1}$$

$$Y = \left[\frac{R_1\omega^2C_1^2}{(1-\omega^2L_1C_1)^2 + R_1^2\omega^2C_1^2}\right] + \left[C_0\omega + \frac{(1-\omega^2L_1C_1)\omega C_1}{(1-\omega^2L_1C_1)^2 + R_1^2\omega^2C_1^2}\right]j \tag{2}$$

The conductance G and the susceptance B can be written as in Eqs. (3) and (4), respectively.

$$G = \frac{R_1\omega^2C_1^2}{(1-\omega^2L_1C_1)^2 + R_1^2\omega^2C_1^2} \tag{3}$$

$$B = C_0\omega + \frac{(1-\omega^2L_1C_1)\omega C_1}{(1-\omega^2L_1C_1)^2 + R_1^2\omega^2C_1^2} \tag{4}$$

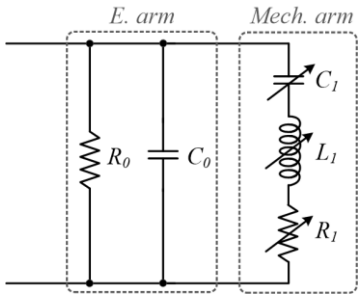


Figure.1 UPZT equivalent circuit

$$\left(G-\frac{1}{2R_1}\right)^2+(B-\omega C_0)^2=\left(\frac{1}{2R_1}\right)^2 \quad (5)$$

The result computed from Eq. (3) and Eq. (4) is given by Eq. (5). From Eq. (5), the locus of the UPZT admittance near resonance frequency can be plotted as shown in Fig. 2. Where f_s is the series resonance frequency, which corresponds to the maximum conductance, f_p is the parallel resonance frequency, f_r is the resonance frequency corresponding to the larger conductance when the susceptance is zero, f_a is the anti-resonance frequency corresponding to the smaller conductance when the susceptance is zero, f_m is the frequency of maximum admittance (minimum impedance) and f_n is the minimum admittance frequency.

$$f_s=\frac{1}{2\pi\sqrt{L_1C_1}} \quad (6)$$

From the UPZT equivalent circuit in Fig. 1, the impedance phase (θ) can be calculated as in Eq. (7).

$$\theta=\tan^{-1}\left[\frac{(2L_1C_0+L_1C_1-C_1C_0R_1^2)\omega}{C_1R_1}-\frac{L_1^2C_0\omega^3}{R_1}-\frac{C_0+C_1}{C_1^2R_1\omega}\right] \quad (7)$$

When the impedance phase of UPZT is zero, the following Eq. (8) is computed.

$$L_1^2C_1^2C_0\omega^4-\omega^2C_1(2L_1C_0+L_1C_1-C_0C_1R_1^2)+C_0+C_1=0 \quad (8)$$

$$f_r=\frac{1}{2\pi}\sqrt{\frac{(2L_1C_0+L_1C_1-C_0C_1R_1^2)-\sqrt{C_1^2(L_1-C_0R_1^2)^2-4L_1C_1C_0^2R_1^2}}{2L_1^2C_0C_1}} \quad (9)$$

$$f_a=\frac{1}{2\pi}\sqrt{\frac{(2L_1C_0+L_1C_1-C_0C_1R_1^2)+\sqrt{C_1^2(L_1-C_0R_1^2)^2-4L_1C_1C_0^2R_1^2}}{2L_1^2C_0C_1}} \quad (10)$$

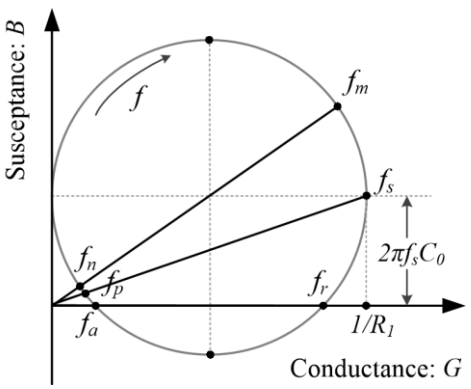


Figure.2 The UPZT admittance circle

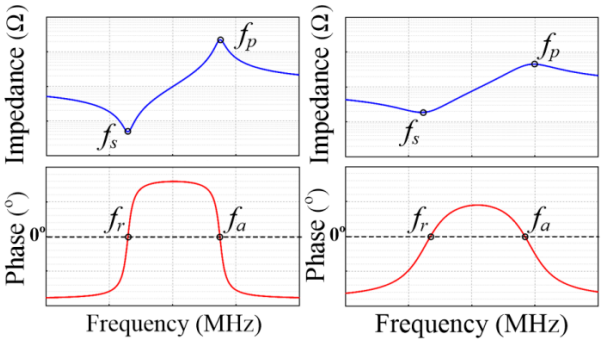


Figure.3 The frequency response of UPZT: (a) No load and (b) With load

By solving Eq. (8) the resonance frequency f_r and the anti-resonance frequency f_a can be written as in Eq. (9) and Eq. (10), respectively.

The comparison of the frequency responses of UPZT between (a) no load and (b) with load are shown in Fig. 3 [8-9]. There are two characteristic frequencies that are classified by a zero impedance phase f_r and f_a. The anti-resonance frequency f_a has higher impedance than the resonance frequency f_r and it is not at the optimum operating point of the UPZT [5, 16].

When the UPZT is excited by the resonance frequencies f_s, f_m or f_r, the electrical power fed to the UPZT is maximized. In this research, the f_r of the UPZT is used for designing instead of the f_s for the proposed automatic-tuning technique because of measuring the phase is relatively easier.

3. Proposed UPZT driving circuit design

The proposed automatic-tuning frequency UPZT driving circuit diagram is shown here in Fig. 4. It is similar to the conventional driving circuit without tuning capability from [8]. The proposed driving circuits utilize the same class-F power amplifier (PA) to supply the electrical power to the UPZT. This class-F PA is a switched-mode type with high efficiency of up to 95% according to [8]. The output power of this PA is controlled by a SEPIC converter in order that the ultrasound output power ($Watt_U$ or W_U) from the UPZT can be adjusted. The conventional driving circuit has a drawback that the driving frequency must be manually set from datasheet and cannot be changed during operating period. In real operations, the phase differences between voltage and current of the driving signal could be fluctuated all the time due to impedance changing of UPZT caused by the different pressure and touching surface with human skin. It is, of course, reflecting in deterioration in system efficiency and performance.

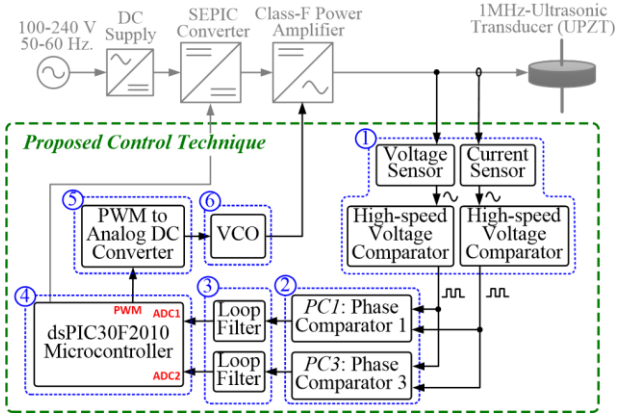


Figure.4 System diagram of the proposed UPZT driving circuit with automatic-tuning frequency capability

The main idea to resolve the aforementioned problem of the conventional driving technique is trying to real-time track the UPZT impedance and phase during operation, then recomputed the PA controlling signals using a newly-proposed high-speed dsPIC microcontroller. The main goal is to instantaneously tune the UPZT driving frequency to be as close to the changing resonance frequency (*fr*) as possible and also keep the phase difference to be near zero.

In order to do that, a newly-designed feedback control circuit consisting of six sub blocks as shown in Fig. 4 has been added to the conventional driving circuit to make it capable of tuning to any desire frequency and also tracking the UPZT changing impedance and phase all the time during operations.

Fig. 4 mainly indicates the key components and system overview of the newly-proposed automatic-tuning frequency driving circuit. Six sub feedback-control units have been added from the conventional driving circuit as follows: (1) *voltage and current sensing unit*, (2) *phase comparator*, (3) *loop filter*, (4) *dsPIC microcontroller*, (5) *PWM to analog DC converter* and (6) *voltage control oscillator (VCO)*. Fig. 5 mainly presents how each of six units works in sequences.

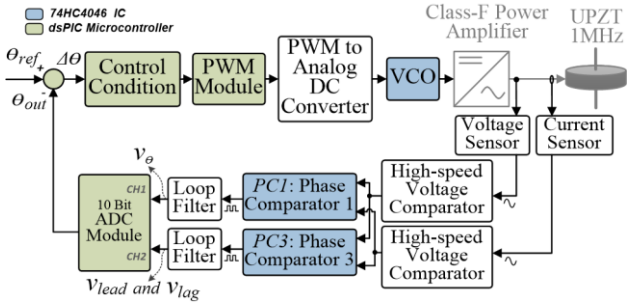


Figure.5 Another view of the newly-design feedback-control block of the proposed UPZT driving circuit

4. Proposed feedback control design

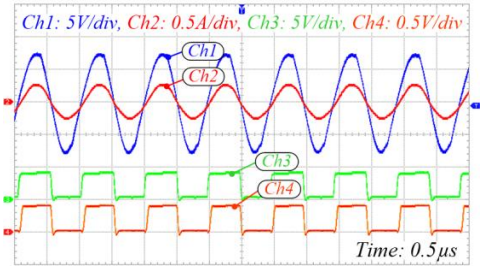
The operational flow of the newly proposed feedback control starts from sensing the voltage and current signals and passes them through the high-speed voltage comparator to transform into voltage and current pulse trains. Those pulse trains will then be fed through phase comparator units. Comparing results will be passed through the internal ADC module of the dsPIC30F2010 via loop filters. The computational process will then be done by dsPIC microcontroller before sending the desirable control signals to VCO units via the PWM to analog DC converters. The VCO units will then send out the controlling signals to tune the final frequency of the class-F power amplifier. The target when applying this technique with any UPZT in real-time operation is that the steady-state error from ideal resonance frequency *fr* must be lower than ±1.0% at any time and the phase difference between UPZT driving voltage and current must be lower than ±10^{o}.

4.1 Getting voltage and current pulse trains

This first step of the newly-proposed feedback control unit is shown by block number 1 in Fig. 4. This unit generates voltage and current pulse trains to be inputs of each phase comparator unit using a data-discrimination high-speed voltage comparators. An in-house-design voltage divider and a high-precision current sensor were used to gather voltage and current signals in real time. Fig. 6 illustrates the example of measuring input and pulse-train output signals for this procedure. Fig. 6 also confirms that this unit is working properly and accurately.

4.2 Phase comparator design

This research applies the phase comparator 1 (PC1) and the phase comparator 3 (PC3) from the 74HC4046 integrated circuit to be functioned as main phase comparator units. In this design, the higher resolution PC1 will be used as a phase-difference detector (0-180 degree) and the lower



Ch1: UPZT voltage, Ch3: Voltage pulse trains to phase comparator, Ch2: UPZT current, Ch4: Current pulse trains to phase comparator

Figure.6 Examples of voltage and current pulse trains

resolution PC3 will be used as a lead-lag detector (plus/minus sign).

Fig. 7 and Fig. 8 represent typical waveforms and how both PC1 and PC3 work. Two identical sets of voltage and current pulse-train signals from 4.1 will be fed into both PC1 and PC3 as SIG_{IN} and $COMP_{IN}$. The phase differences between the two can now be compared in terms of new pulse-train signals, namely $PC1_{OUT}$ and $PC3_{OUT}$, respectively.

At PC1, the rising edge and falling edge of both input signals SIG_{IN} and $COMP_{IN}$ will be compared. The comparison results will then be computed and translated into a phase difference value in the range of 0-180 degree with 2 MHz resolutions, $PC1_{OUT}$. In this design, the relationship between the average phase difference output voltage and phase difference in degrees is set as a linear relationship shown in the right-hand side of Fig. 7 The proposed design sets the operating supply voltage V_{CC} at 5V; therefore, the average output voltage between 0V to 5V is corresponding to phase difference between 0 to 180 degrees. In other words, the linear ratio of average output voltage to phase difference in this case equals 28 mV/1°.

At PC3, only rising edges of both input signals SIG_{IN} and $COMP_{IN}$ will be compared with the same strategies as in PC1, but, the average output voltage between 0V to 5V in this PC3 is corresponding to phase difference between 0 to 360 degrees instead. The translation here is a bit different from PC1. The current signal status will be read in the forms of either lagging (- sign) or leading (+ sign) with the voltage signal. The current status is *lagging* when the average comparison output is in the range of 0-2.5V and the current status is *leading* when the average comparison output is in the range of 2.5-5.0 V. This procedure is illustrated in Fig. 8.

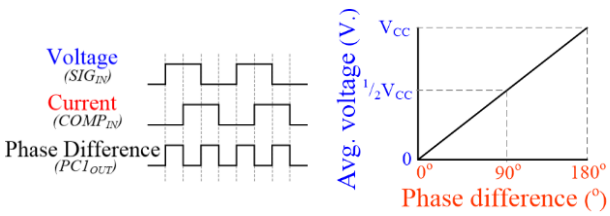


Figure.7 Phase comparator 1 (PC1) design

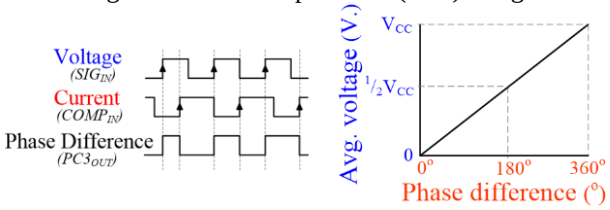


Figure.8 Phase comparator 3 (PC3) design

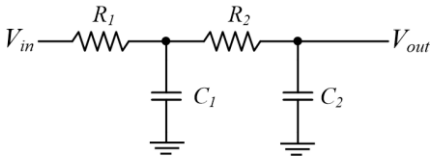


Figure.9 A simple equivalent circuit for a loop filter

The phase difference results from $PC1_{OUT}$ and $PC3_{OUT}$ will be fed into a 10-bit ADC module of the dsPIC30F2010 microcontroller via loop filters. The uncertainty and tolerances for processing the phase difference in this procedure is set to be at ±1°.

4.3 Loop filter configurations

In this work, a passive-type second-order RC low-pass filter [17] will be used as a loop filter due to its simplicity. The main task for loop-filter units in this work is to receive the PWM-like pulse trains from the phase comparator units which carry the voltage and current phase-differences information. The loop filters then convert such signals into analog direct current (DC) signal and send to the ADC module of the dsPIC microcontroller for further processing. A simple equivalent circuit with two resistors and two capacitors for a loop-filter design in this research is shown in Fig. 9.

A loop-filter design starts from knowing the maximum V_{RIPPLE} and V_{PWM} allowed from the phase comparator in 4.2. The attenuation factor in dB (A_{dB}) can now be computed using Eq. (11).

$$A_{dB} = 20 \times \log\left(\frac{V_{RIPPLE}}{V_{PWM}}\right) \tag{11}$$

Once the attenuation factor is known, we can apply the knowledge that the slope of a second order low-pass filter equals -40 dB/decade to determine a required 3-dB cut-off frequency (f_{3dB}) for a loop filter using either Eq. (12) or Eq. (13).

$$A_{dB} = Slope \times \log\left(\frac{f_{PWM}}{f_{3dB}}\right) \tag{12}$$

$$f_{3dB} = f_{PWM} \times 10^{-\frac{A_{dB}}{Slope}} \tag{13}$$

Another interesting view is to set Eq. (11) equals to Eq. (12) and solve for V_{RIPPLE}. This will result in Eq. (14) that expresses voltage ripple as a function of f_{3dB}. While this equation looks more complicated than Eq. (11), Eq. (12) and Eq. (13), it has very simple mathematics, especially, if we want to graphically plot ripple voltage versus f_{3dB} for determining slope, V_{PWM} and f_{PWM}.

$$V_{RIPPLE} = V_{PWM} \times 10^{\frac{Slope \times \log\left(\frac{f_{PWM}}{f_{3dB}}\right)}{20}} \quad (14)$$

Based on the circuit previously shown in Fig. 9, the components in the circuit can be calculated by

$$f_{3dB} = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \quad (15)$$

Given $R = R_1 = R_2$ and $C = C_1 = C_2$, Eq. (15) then becomes Eq. (16)

$$f_{3dB} = \frac{1}{2\pi RC} \quad (16)$$

From Eq. (16), by choosing the proper capacitor C values, the resistor R values for this loop filter can be computed. Therefore, from Eq. (11), the computed A_{dB} equals -66.375 dB and the f_{3dB} equals 43.818 kHz. We then get the desire values of capacitors $C_1 = C_2 = 15$ nF and the resistors $R_1 = R_2 = 242$ Ω for this design.

4.4 dsPIC Microcontroller

For the proposed control technique shown in Fig. 4, the output frequency of VCO is controlled by the pulse width modulation (PWM) module of the dsPIC30F2010 microcontroller. The frequency of a PWM signal here will be constant and the duty cycle can be adjusted depending on the signals from the phase comparators via loop filters. In this work, the dsPIC30F2010 is running at 29.4912 MHz (f_{cy}) to compute the PWM signal frequency for VCO unit at 10 kHz. The PWM bits resolution can be determined using Eq. (17) and equals to 11.526 bits which results in 2,949 steps of PWM pulse adjustability.

$$\text{PWM Bits Resolution} = \frac{\log\left(\frac{f_{cy}}{f_{PWM}}\right)}{\log(2)} \quad bits \quad (17)$$

Since we know that PWM amplitude is ranging from 0-5V, the PWM voltage resolution can now be computed and equals to 1.6954 mV/step. This PWM voltage resolution will then be used by dsPIC microcontroller to calculate the final desirable PWM duty cycle.

4.5 PWM to analog DC converter

The PWM signal from the dsPIC30F2010 will be converted into direct current (DC) signal by another second-order RC low-pass filter. This technique is similar to the converter mentioned in [17, 18]. It is called *PWM to analog DC converter* in this paper and is shown in Fig. 10. The DC signals getting from this process will be fed as inputs of the VCO unit in the next step.

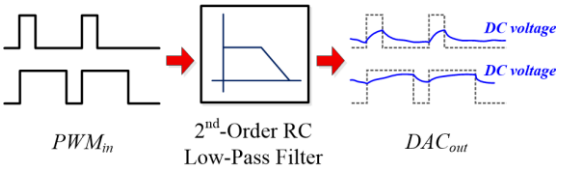


Figure.10 The PWM to analog DC converter in this work

In order to maximize the performance of this *PWM to analog DC converter*, the allowed ripple voltage must be set to less than the PWM voltage resolution computed from 4.4. In this research, the ripple voltage of DC signal from this converter must be less than 1.6954 mV. We then again apply Eqs. (11) and (13) to determine A_{dB} and f_{3dB}, respectively. The final value in computing f_{3dB} for this converter equals to 184.14 Hz. Again, by using Eqs. (15) and (16), the design values for capacitors will then be $C_1 = C_2 = 0.33$ uF and the design values for resistors will then be $R_1 = R_2 = 2.7$ kΩ in this certain step.

4.6 VCO configurations

We choose to use the voltage control oscillator (VCO) module from the PLL IC (74HC4046) in this research. This 74HC4046 IC has an internal and high-linearity VCO module. The center frequency of this module can be set upto 17 MHz at the operating supply voltage ($V_{CC} = 5$V).

The frequency range of VCO is set by the selecting value of R_1, R_2 and C_1 shown in Fig. 11. The value of R_1, R_2 and C_1 are selected to be 65 kΩ, 10 kΩ and 1 nF, respectively. In this research, the 74HC4046 IC is operated at 5.0 Volt. Therefore, the center frequency of VCO (f_0) equals 1.03 MHz and the VCO_{IN} range becomes 0.9-4.1V that yields the VCO_{OUT} frequency [f_{min} to f_{max}] of 0.98-1.08 MHz. The VCO_{IN} / VCO_{OUT} ratio (between input voltage and output frequency) is now equal to 32 mV/kHz. All VCO configurations are set as shown in Table 1.

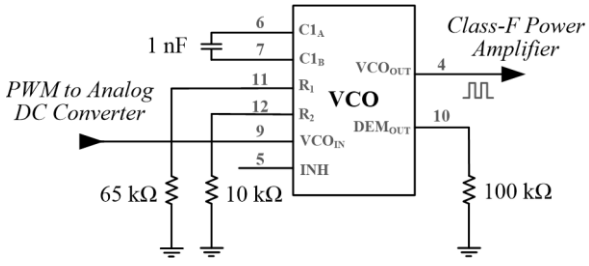


Figure.11 The VCO module used in this work

Table 1. VCO configurations

Descriptions	Setting values
Supply voltage: V_{CC}	*5.0 V*
Voltage range of VCO_{IN}	*0.9 - 4.1 V*
VCO_{OUT} center frequency: f_0	*1.03 MHz*
VCO_{OUT} maximum frequency: f_{max}	*1.08 MHz*
VCO_{OUT} minimum frequency: f_{min}	*0.98 MHz*
VCO_{IN} / VCO_{OUT} Ratio	*32 mV/kHz*

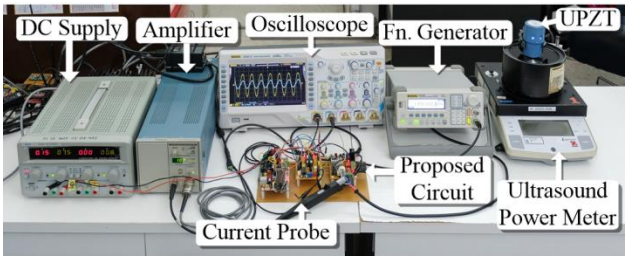


Figure.12 The experimental setup in this work

5. Experimental results and discussions

5.1 Test setup and experimental configurations

The experimental system configuration has been identically setup to the block diagram previously shown in Fig. 4 to verify accuracies and overall performances of the proposed auto-tuning technique. By using pure water as a UPZT load simulating the actual human skin to make it possible to measure and analyze the driving circuit manners and UPZTs characteristics. The calibrated ultrasound power meter model: UPM-DT-1 (±2mW resolution) is also connected at the end of UPZT under the test to record the ultrasound power output ($Watt_U$ or W_U) from each test. The actual experimental setup can be seen in Fig. 12. We then separated the test into five main parts from 5.2 to 5.6. Each section has its own purposes or targets as will be described here.

5.2 UPZTs frequency and impedance analysis

5.2.1. UPZTs frequency and impedance analysis

The main purpose of this test is to determine impedances and resonance frequencies (*fr* and *fa*) of five UPZT samples to be references. The experiment was done using a high-speed data acquisition device. The frequency response can be analyzed in the range of 1 Hz to 150 MHz, the swept-frequency resolution is at 1 Hz, the dynamic performance is 95 dB, the accuracy of a measuring gain is ±0.20 dB and the accuracy of a measuring phase is ±0.05°.

Table 2. The resonance frequencies and impedances analysis of five UPZT samples

UPZT Samples	Measuring resonance frequency: f_r (MHz)	Measuring anti-resonance frequency: f_a (MHz)	Measuring impedances: $\|Zr\|$ (Ω)
# 1	*1.0300*	*1.0750*	*30.5*
# 2	*1.0290*	*1.0770*	*32.3*
# 3	*1.0340*	*1.0710*	*27.4*
# 4	*1.0220*	*1.0670*	*24.6*
# 5	*1.0150*	*1.0660*	*29.5*

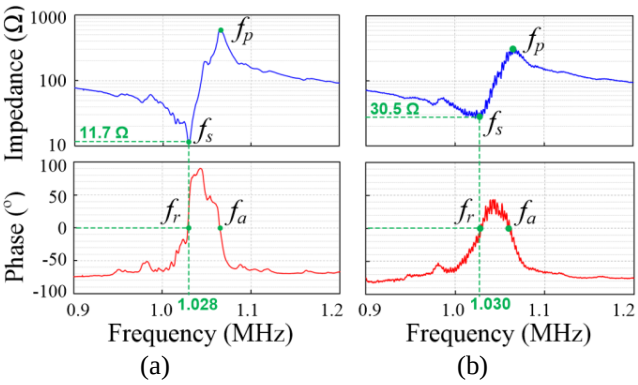


Figure.13 Impedance analysis with and without load: (a) no load and (b) with load

Table 2 presents the impedance test results of five samples. The experimental results show that the resonance frequencies of all UPZTs are in between 1.015-1.034 MHz, while the UPZT impedances at resonance frequencies are in between 24.6-32.3 Ω.

5.2.2. Impedance analysis with and without load

Fig. 13 plots the impedance analysis results of a UPZT sample in two cases: no load and with load. The test results in both cases were analyzed in the frequency range of 0.9-1.2 MHz. The increment of frequency-swept step is 0.05% or 2,000 steps along the test range.

From the experimental results in case of no load shown in Fig. 13(a), the resonance frequency (*fr*) is measured at 1.028 MHz and the impedance at resonance frequency equals 11.7 Ω. From the results in case of having load shown in Fig. 13(b), both of the resonance frequency (*fr*) and the impedance at resonance frequency are a bit larger than the no-load case. The resonance frequency (*fr*) is then measured at 1.030 MHz and the impedance at resonance equals 30.5 Ω.

5.3 Automatic frequency (*fr*) tuning capability

The purpose of this test is to verify the tuning capability of the proposed technique to see how

accurate it is and to compute the percentage of steady-state errors.

The same five UPZT samples from 5.2 were selected to be used in this experiment. Each of them was tested three times to settle around the desirable resonnace frequency (*fr*) mentioned in Table 2. The steady-state errors and final tuning frequencies from every single test were recorded. The test results are presented in Table 3. It is clear from this experiment that the newly-proposed and auto-tuning technique works efficiently. The steady-state errors comparing to the desired frequencies are less than ±1.0%.

5.4 Automatic frequency (*fr*) tuning performance

The main goal for this test is to see how good the proposed technique in automatically tuning UPZT driving circuit to the desirable resonance frequencies around 1 MHz by two indicators: (1) final phase differences (should be minimal and less than ±10 degree) and (2) the tuning time (the shorter the better). Table 4 presents in-depth details for the tuning performance tests.

Fig. 14 illustrates the performance test result for the UPZT sample #1 in Table 2 using the proposed automatic-tuning technique by setting the initial frequency of the driving circuit at 0.95 MHz, regardless of the initial phase differences. It can be clearly seen from the plot that it took around 10 ms (10.8 ms to be exact in this case) for the proposed technique in order to tune to the desirable resonance frequency (*fr*) at 1.030 MHz and also to the minimal phase difference at -1.04 degree. The roots mean squared error (RMSE) of a phase difference from zero in this case is equal to 1.046°.

Table 3. Automatic-tuning capability test results

UPZT samples	Desired resonance frequency: f_r (MHz)	Proposed auto-tuning method		
		Test No.	Auto-tuning frequency (MHz)	Steady-state error (%)
# 1	**1.0300**	**1**	*1.0295*	*-0.05*
		2	*1.0279*	*-0.20*
		3	*1.0301*	*0.01*
# 2	**1.0290**	**1**	*1.0281*	*-0.09*
		2	*1.0311*	*0.20*
		3	*1.0296*	*0.06*
# 3	**1.0340**	**1**	*1.0336*	*-0.04*
		2	*1.0341*	*0.01*
		3	*1.0348*	*0.07*
# 4	**1.0220**	**1**	*1.0217*	*-0.03*
		2	*1.0225*	*0.05*
		3	*1.0199*	*-0.20*
# 5	**1.0150**	**1**	*1.0162*	*0.12*
		2	*1.0153*	*0.03*
		3	*1.0148*	*-0.02*

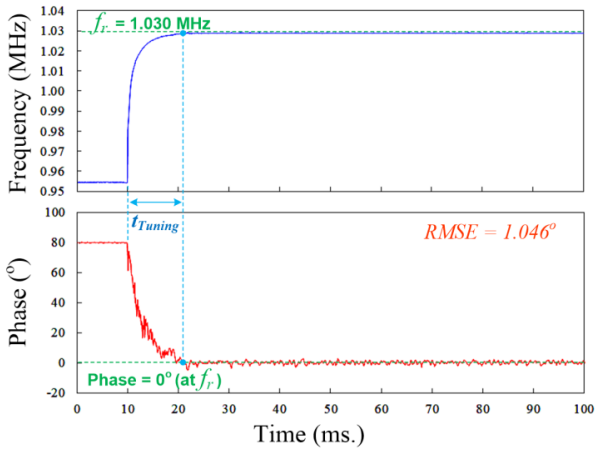


Figure.14 Example of performance test results

Table 4. Automatic tuning performance test results

UPZT samples	Desired resonance frequency: f_r (MHz)	The proposed tuning method		
		Tuned frequency (MHz)	Final phase difference (Degree °)	Tuning time t_{Tuning} (ms)
# 1	**1.0300**	*1.0295*	*-1.04*	*10.8*
# 2	**1.0290**	*1.0281*	*-1.93*	*11.1*
# 3	**1.0340**	*1.0336*	*-2.46*	*11.9*
# 4	**1.0220**	*1.0217*	*-3.87*	*10.5*
# 5	**1.0150**	*1.0162*	*-1.22*	*9.2*

5.5 Efficiency comparisons (conventional from [8] vs proposed techniques)

The efficiency comparisons have been done between two different methods: (1) the conventional fixed-frequency-and-non-tuned technique mentioned in [8] versus (2) the proposed auto-tuning technique.

The main input power is equally fed into each driving circuit and the measurements were done at the PA driving-circuit outputs and at the UPZT ultrasound output. The efficiencies were computed and analyzed. It is confirmed from the experimental results in Table 5 that the proposed technique results in higher efficiencies in every ways.

Fig. 15 illustrates the examples of measuring voltage and current signals from UPZT driving circuits. Fig. 15(a) illustrates driving voltage and current signals from the conventional technique (set fixed resonance frequency (*fr*) at 1.000 MHz). The phase differences between voltage and current signals could be varied from 10°-80° depending on the UPZT itself or the load characteristics resulting in deterioration of power transfer and inefficiency.

Table 5. Efficiency comparisons test results (conventional non-tuned vs proposed techniques)

Input Power (W)	**Conventional technique** *(driving UPZT at fixed frequency around 1 MHz in [8])*				**The proposed technique** *(driving UPZT with Auto-tuning frequency capability)*			
	PA Output (W)	PA Eff. (%)	UPZT Output (W_U)	UPZT Eff. (%)	PA Output (W)	PA Eff. (%)	UPZT Output (W_U)	UPZT Eff. (%)
1.0	**0.830**	**83.0**	**0.372**	**44.8**	*0.930*	*93.0*	*0.590*	*63.4*
2.0	**1.839**	**92.0**	**0.746**	**40.6**	*1.876*	*93.8*	*1.186*	*63.2*
3.0	**2.773**	**92.4**	**1.106**	**39.9**	*2.821*	*94.0*	*1.784*	*63.2*
4.0	**3.364**	**84.1**	**1.354**	**40.2**	*3.714*	*92.9*	*2.328*	*62.7*
5.0	**4.023**	**80.5**	**1.642**	**40.8**	*4.516*	*90.3*	*2.840*	*62.9*
Avg.	***86.4%***		***41.3%***		***92.8%***		***63.1%***	

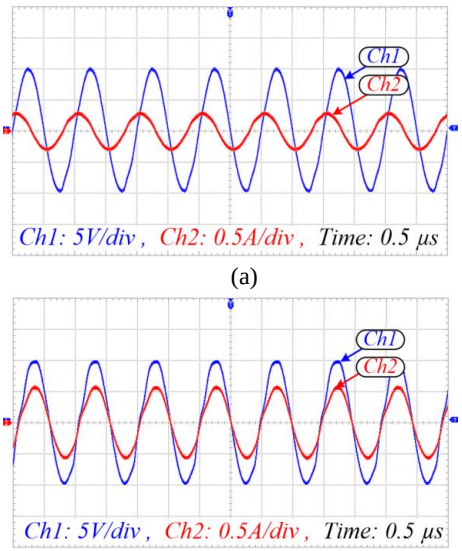


Figure.15 Voltage and current signals at UPZTs: (a) Conventional non-tuned voltage and current signals [8] and (b) Proposed automatic tuning voltage and current signals

Fig. 15(b), on the other hand, illustrates the UPZT driving signals from the proposed driving circuit with automatic-tuning technique. The phase differences between the voltage and current signals has significantly drop-down close to zero which results in more efficient power transfer.

5.6 Tracking capability when load is changing

Not only we want to see the proposed technique has efficient tuning capability but also the properly tracking capability when the load is changing. The need for tracking capability is mandatory when the physiotherapist uses the ultrasound device with real patients in the actual operations. The impedance of any UPZT will be changed all the time due to the human-skin touching area. The last experiment is setup to simulated such circumstance and to verify the tracking capability of the proposed technique when the load is changing from "No load - Load - No load" conditions.

Fig. 16 presents the plots of operating frequency (fixed at *fr*) and the phase difference between voltage and current when using the conventional driving circuit mentioned in [8]. It is clear that the driving circuit frequency is solid as constant all the time. Unfortunately, during the loaded condition (the 3rd to 7th second), the phase difference will be changing so much resulting in deterioration of ultrasound power output. The phase difference here could be varied from 10° to 80° depending on load characteristics which could lead to 5 to 40 percents of ultrasound power dropped.

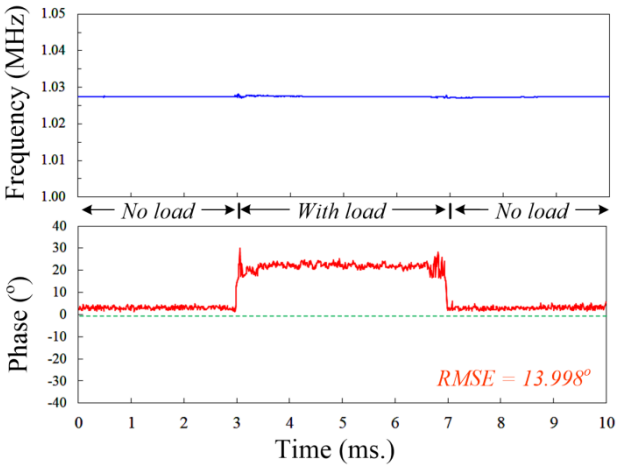


Figure.16 Conventional fixed-frequency tracking capability when load is changing [8]

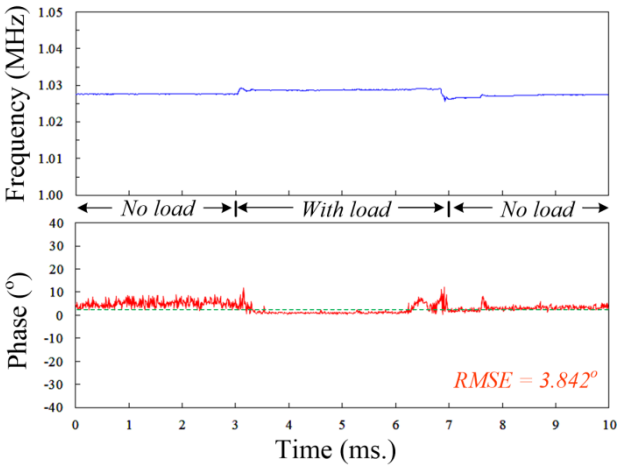


Figure.17 The proposed automatic tracking capability when load is changing

Fig. 17 shows the plots of operating frequency and phase difference when using the proposed automatic tuning technique. It is confirmed that the proposed technique is able to properly track the frequency when the load is changing and also maintain the phase difference to be minimal (less than $\pm 10^{o}$) over the test period.

6. Conclusions

This research proposed the novel methodology of using the PLL technique incorporates with dsPIC microcontroller (dsPIC30F2010) for enhancing and maximizing the performance of a 1 MHz UPZT driving circuit class-F type from the conventional research. This research applied the newly-proposed phase angle comparator circuit to track the phase differences between the voltage and current in the feedback control part of the UPZT driving circuit. The acquired phase differences will then be passed to analyze in a dsPIC microprocessor and then recalculate the optimum parameters in main control circuit to assure the minimal phase angle differences (closet to zero and must be less than $\pm 10^{o}$).

It is clear to be seen from the experimental results that all UPZTs under the test have different impedances and resonance frequencies. The results also confirm that the newly proposed technique is capable of automatically tuning to the optimum resonance frequency regardless of any preset value for maximizing the overall ultrasonic performance, accurately and reliably. The average percentage of automatic tuning frequency errors is less than ±0.2%. The speed of convergence is around 9-12 millisecond. The stability and reliability of the proposed method has been insured. In addition to that, the proposed methodology also shows the promising results of tracking the desired resonance frequency even in the case of a real-time load changing.

Acknowledgments

This research was partially sponsored by the King Mongkut's Institute of Technology Ladkrabang (KMITL) Foundation, under the Graduate School Scholarship, 2016. The authors would also like to thank my colleagues from the Energy System and Illumination Research Center (ESIRC, KMITL) who provided great helps in this research and for comments that greatly improved this valuable manuscript.

References

[1] Y. Mizutani, T. Suzuki, H. Ikeda, and H. Yoshida, "Power maximizing of ultrasonic transducer driven by MOSFET inverter operating at 1 MHz", In: *Proc. of International Conf. On Industrial Electronics, Control and Instrumentation (IECON)*, pp. 983-986, 1996.

[2] T. Yuan, X. Dong, H. Shekhani, C. Li, Y. Maida, T. Tou, and K. Uchino, "Driving an inductive piezoelectric transducer with class E inverter", *International Journal of Sensors and Actuators A: Physical*, Vol.261, pp. 219-227, 2017.

[3] Y. Mizutani, T. Suzuki, J. Ishikawa, H. Ikeda, and H. Yoshida, "Operating frequency control for maximizing output power of MOS-FET power inverter to drive megasonic transducer at 3 MHz", In: *Proc. of International Conf. On Industrial Electronics, Control and Instrumentation (IECON)*, pp. 877-881, 1997.

[4] Q. Li, L. Zhu, and F. Wang, "Design of Ultrasonic Generator Based on DDS and PLL Technology", In: *Proc. of International Symposium on High Density packaging and Microsystem Integration (HDP '07)*, pp.1-4, 2007.

[5] H. Zhang, F. Wang, D. Zhang, L. Wang, Y. Hou, and T. Xi, "A new automatic resonance frequency tracking method for piezoelectric ultrasonic transducers used in thermosonic wire bonding", *International Journal of Sensors and Actuators A: Physical*, Vol.235, pp.140-150, 2015.

[6] H. Zhang, F. Wang, Y. Tian, X. Zhao, D. Zhang, and L. Han, "Electrical matching of low power piezoelectric ultrasonic transducers for microelectronic bonding", *International Journal of Sensors and Actuators*, Vol.199, pp.241-249, 2013.

[7] X. Wei, Y. Yang, W. Yao, and L. Zhang, "An automatic optimal excitation frequency tracking method based on digital tracking filters for sandwiched piezoelectric transducers used in broken rail detection", *International Journal of Measurement*, Vol.135, pp. 294-305, 2019.

[8] S. Boontaklang, C. Chompoo-inwai, J. Mungkorn, and M. Leelajindakrairerk, "Novel Design of Class-F Power Amplifier for a Therapeutic-Ultrasonic-Piezoelectric-Transducer (UPZT) Driving Circuit Using the Multi-Microprocessor-Controlled Techniques", In: *Proc. of International Conf. on Electrical Engineering (ICEE 2014)*, pp.1450-1455, 2014.

[9] X. Liu, A. I. Colli-Menchi, J. Gilbert, D. A. Friedrichs, K. Malang and E. Sánchez-Sinencio, "An Automatic Resonance Tracking Scheme With Maximum Power Transfer for Piezoelectric Transducers", *IEEE Transactions on Industrial Electronics*, Vol.62, No.11, pp.7136-7145, 2015.

[10] D. A. Friedrichs, R. W. Erickson and J. Gilbert, "A New Dual Current-Mode Controller Improves Power Regulation in Electrosurgical Generators", *IEEE Transactions on Biomedical Circuits and Systems*, Vol.6, No.1, pp.39-44, 2012.

[11] M. A. Ahmad, A. M. Elshurafa, K. N. Salama and H. N. Alshareef, "Determination of maximum power transfer conditions of bimorph piezoelectric energy harvesters", *Journal of Applied Physics*, Vol.111, No.10, 2012.

[12] C. Lin, Y. Lu, H. Chiu and C. Ou, "Eliminating the Temperature Effect of Piezoelectric Transformer in Backlight Electronic Ballast by Applying the Digital Phase-Locked-Loop Technique", *IEEE Transactions on Industrial Electronics*, Vol.54, No.2, pp. 1024-1031, 2007.

[13] L. Cheng, Y. Kang and C. Chen, "A Resonance-Frequency-Tracing Method for a Current-Fed Piezoelectric Transducer", *IEEE Transactions on Industrial Electronics*, Vol.61, No.11, pp.6031-6040, 2014.

[14] J. M. Alonso, C. Ordiz and M. A. Dalla Costa, "A Novel Control Method for Piezoelectric-Transformer Based Power Supplies Assuring Zero-Voltage-Switching Operation", *IEEE Transactions on Industrial Electronics*, Vol.55, No.3, pp.1085-1089, 2008.

[15] D. Vasic, Y. Liu, F. Costa, and D. Schwander, "Piezoelectric transformer-based DC/DC converter with improved burst-mode control", In: *Proc. of IEEE Energy Conversion Congress and Exposition*, pp.140-146, 2013.

[16] Y. Kuang, Y. Jin, S. Cochran, and Z. Huang, "Resonance tracking and vibration stablilization for high power ultrasonic transducers", *International Journal of Ultrasonics*, Vol.54, pp.187-194, 2014.

[17] R. Metivier, *Method for Converting a PWM Output to an Analog Output When Using Hall Effect Sensor ICs (Application information AN296094)*, Allegro Micro Systems LLC, Massachusetts, 2013.

[18] B. Nisarga, *PWM DAC using MSP430 high-resolution timer (Application report SLAA497)*, Texas instrument, Dallas Texas, 2011.