



## A Novel Back Lobe Reduction Technique for Microstrip Antenna Array Using Partial Ground and DGS

Vantaku Nagendra Lakshmana Kumar<sup>1\*</sup>

Moturi Satyanarayana<sup>1</sup>

Sohan Pal Singh<sup>2</sup>

<sup>1</sup>*Department of Electronics and Communication Engineering,  
MVGR College of Engineering (Autonomous), Vizianagaram, Andhra Pradesh, India*

<sup>2</sup>*Department of Electronics and Communication Engineering,  
Mahatma Gandhi Institute of Technology, Hyderabad, Telangana, India*

\*Corresponding Author Email: [vlakshmana1127@gmail.com](mailto:vlakshmana1127@gmail.com)

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**Abstract:** In this communication, back lobe reduction in microstrip antenna array using partial ground and defected ground structure (DGS) is presented. An eight element rectangular microstrip patch antenna array is designed for X-band frequency of 9.1GHz, with a peak gain of 12.04dBi and back lobe level of -13.75dB. Using partial ground plane technique; the back lobe level is reduced to -18.28dB. Then, by placing defected ground structure (DGS) slots on the ground plane, the  $S_{11}$  is further reduced by 7.65dB and back lobe level is reduced to -18.82dB. This microstrip antenna array with partial ground plane and DGS technique has a peak gain of 12.41dBi. By using this novel technique, the front to back ratio has improved from 19dB to 24.23dB. The Simulations are carried using High frequency structured simulator (HFSS) software and compared with measured results. A difference of 0.96dB is observed between simulated and measured back lobe level.

**Keywords:** Back lobe level, Defected ground structure, Front to back ratio, Microstrip patch antenna, Sidelobe level.

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### 1. Introduction

Microstrip antennas are low profile, simple and inexpensive antennas. These are conformable to planar structures, can be compatible to Monolithic microwave integrated circuit (MMIC) designs and mechanically robust [1]. Due to these advantages they find applications in satellites, missiles, aircrafts, spacecraft and communication systems. The peak sidelobe level and back lobe level are very important parameters in the design of microstrip array antennas. Due to side lobes and back lobes, the power will get wasted in unwanted directions and also creates electromagnetic interference to other on-board neighboring antennas. Lot of work has been done in the past to reduce sidelobe level in antenna arrays, but only limited work is done to reduce back lobe level. Pozar, in his base work has proposed that the diffraction effects can influence the minor lobes in microstrip antennas [2]. It is

very much essential that the front to back ratio has to be greater than 20dB for array antennas in communication systems [3].

In literature, some solutions have been proposed to reduce the back lobe level or to increase the FBR (front to back ratio) in microstrip antenna arrays. Using electromagnetic band gap structures or EBG structures, the back lobe level can be reduced by suppressing the surface waves [4]. In [5], the concepts of mode-superposition and Electromagnetic bandgap structures are used to improve the FBR in microstrip patch antenna. But it requires a large reflector to be used. In paper [6], improvement of FBR is explained using planar soft surfaces. But it involves metal vias to be placed, which is little complex in fabrication. Reduction of back radiation for single circular patch antenna is presented in [7] using planar soft structures. The design becomes more complex for implementing array due to metal vias. Back lobe reduction for

textile microstrip antennas is proposed in [8] using soft surface around the circular microstrip patch antenna. This occupies more area than patch itself. The ground plane edge modification with soft surface is presented in [9] for single microstrip patch antenna at 2.4GHz. But the design of unit cell itself is complex and broadside gain decreases by 1dBi. The concept of ground plane edge shaping is used to increase front to back ratio [10]. But there the peak gain decreases by 2dBi with improvement in FBR. In [11], the concept of quarter wave length choke is explained to achieve high front to back ratio. Using micro-machining technology, where the substrate below the radiating patch is removed to realize low dielectric substrate, the FBR can be improved [12]. But it involves high fabrication cost. The concept of metamaterial superstrate is explained in [13] to reduce surface and space wave effects. It has eliminated the drawback of poor FBR encountered in previous decoupling circuits. It presents an FBR of 20dB for 2 element array in S-band frequency. Using Substrate-Integrated waveguide (SIW) technique, the suppression of back lobe is presented for slot array antennas [14, 15]. In [16], bow-tie slots on SIW cavity are used for triple band applications. Although it gives FBR greater than 17dB, it demands complex feeding mechanism. In [17], substrate integrated technology is used for radio altimeter applications where in two cavity resonators are nested. It promises FBR greater than 19dB. But it requires three feeding points for single antenna. The concept of backed reflector can also be used to reduce back lobe radiation [18]. It is explained for C-band applications. Most of the existing techniques are demonstrated with single antennas at lower band of frequencies and more or less complex from fabrication point of view. In this paper a simple technique of partial ground plane and defected ground structure (DGS) is presented for back lobe reduction of 8-element microstrip patch antenna array at X-band frequency. First the ground plane optimization is done to reduce the back lobe and then rectangular DGS slots are applied adjacent to T junctions of the feed network to improve the return loss further by 7.65dB. Further, the FBR also improves because of DGS. This proposed technique preserves the peak gain unlike other DGS techniques where the peak gain is seriously get effected. The fabrication is very simple etching process unlike existing techniques, where separate metal strips and vias have to be incorporated. Most of the existing techniques explain achievement of high

FBR taking single antenna only. They don't guarantee high FBR with array. In this paper an FBR of 24.23dB is presented for 8-element array antenna. Section 2 presents the design of eight element rectangular microstrip antenna array. In Section 3, the concepts of partial ground plane and DGS are discussed. In Section 4, the results and discussions are presented. Section 5 gives the Conclusion.

## 2. Design of 8- element rectangular microstrip antenna array

At first, single rectangular microstrip patch antenna is designed with edge feed technique for X-band frequency of 9.1GHz. FR4 substrate with dielectric constant  $\epsilon_r = 4.4$ , height  $h=1.6\text{mm}$ , loss tangent  $\delta = 0.02$  is taken. The resonant frequency is  $f_0 = 9.1\text{GHz}$ . The dimensions of width and length are calculated using the following equations [1, 19]. The width of the patch antenna is given by

$$W = \frac{c}{2f_0 \sqrt{\frac{(\epsilon_r+1)}{2}}} \quad (1)$$

Where “ $c$ ” is the speed of light. The effective length of patch antenna depends on the resonant frequency ( $f_0$ ) and is given by

$$L_{eff} = \frac{c}{2f_0 \sqrt{\epsilon_{reff}}} \quad (2)$$

Where

$$\epsilon_{reff} = \frac{\epsilon_r+1}{2} + \frac{\epsilon_r-1}{2} \left[ 1 + \frac{12h}{w} \right]^{-\frac{1}{2}} \quad (3)$$

The E-fields at the edges of the patch undergo fringing effects. Because of these effects, effective length of the patch antenna appears to be greater than its actual length. So, actual length and effective length of a patch antenna can be related as

$$L = L_{eff} - 2\Delta L \quad (4)$$

Where  $L$  is the actual length,  $\Delta L$  is a function of effective dielectric constant  $\epsilon_{reff}$  and the width to height ratio ( $w/h$ ).

$$\frac{\Delta L}{h} = 0.412 \frac{(\epsilon_{reff}+0.3) \left( \frac{w}{h} + 0.264 \right)}{(\epsilon_{reff}-0.258) \left( \frac{w}{h} + 0.8 \right)} \quad (5)$$

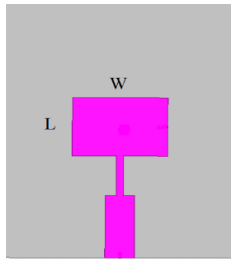


Figure. 1 Edge fed rectangular patch antenna

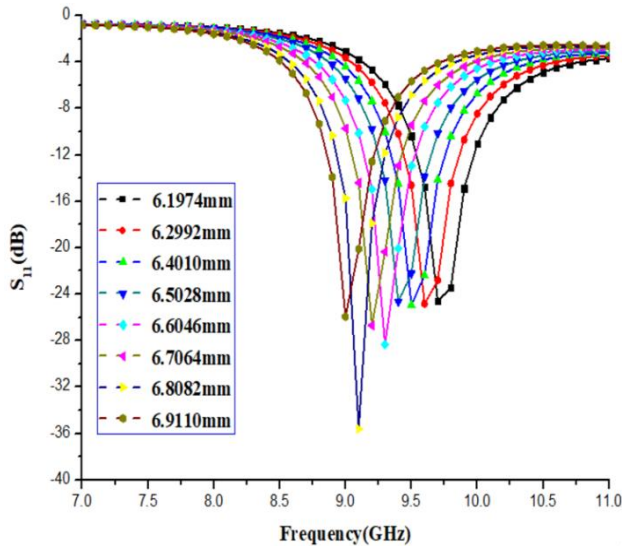


Figure. 2  $S_{11}$  plot for single patch with  $L$  variation

The designed values of patch antenna are  $W=10.03\text{mm}$ ,  $L=7.17\text{mm}$ . The patch model is shown in Fig.1. The patch antenna is in turn optimized for best return loss by varying  $L$  value. At  $L = 6.8082\text{mm}$   $S_{11}$  of  $-35.6\text{dB}$  was achieved using HFSS software. It is shown in Fig. 2.

The optimized dimensions of rectangular patch antenna are  $W=10.03\text{mm}$  and  $L=6.8082\text{mm}$ . These optimized dimensions are considered in the design of 8-element rectangular microstrip array antenna. The array is designed using corporate feed technique as shown in Fig. 3. Each patch in the array are placed with a separation of  $\lambda/2$  distance. Here, the corporate feed network is 3 stage network consisting of  $50\Omega$  line at the first stage. The power fed at the  $50\Omega$  line is distributed equally using  $100\Omega$  lines on either side.  $70.7\Omega$  quarter wave transformer is used for impedance matching between  $100\Omega$  line and  $50\Omega$  junction point. Again, in the second stage same procedure is repeated. In the final stage,  $100\Omega$  line and each patch are impedance matched with  $158.7\Omega$  quarter wave transformer. The dimensions of strip lines, which are used in the feed network are shown in Table 1.

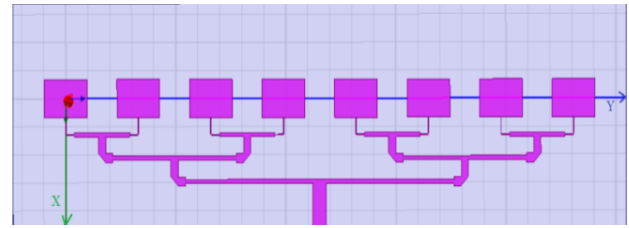


Figure. 3 Eight element microstrip array antenna with corporate feed technique

Table 1. Strip line dimensions of corporate feed network

S.No	Impedance in $\Omega$	Width in mm	Length in mm
1	50.0	3.058	7.527
2	70.7	1.621	4.625
3	100.0	0.709	Variable
4	158.7	0.141	4.886

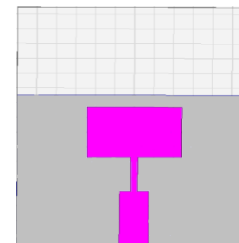


Figure. 4 Single patch with partial ground plane

Table 2. Back lobe level comparison with ground plane variation in case of single patch

S.No	% Ground plane	Sidelobe level in (dB)	Back lobe level in (dB)
1	100	--	-18.094
2	75	-15.745	-18.263
3	70	-15.746	-20.117
4	65	-17.342	-22.547
5	64	-17.533	-23.409
6	63	-17.629	-24.504
7	62	-16.368	-22.904

### 3. Concept of partial ground plane and DGS

The partial ground plane effect is first studied on single patch antenna. Ground plane is reduced from 100% to lower values and both back lobe as well as sidelobe level is observed. The ground plane is removed from opposite side of feed line as shown in Fig. 4.

For 63% of ground plane, both sidelobe as well as back lobe are reduced to great extent. The back lobe level is  $-24.50\text{dB}$  for 63% ground plane. By further reducing the ground plane, poor performance is observed in both back lobe as well as side lobe level. These are shown in Table 2. Here 63% ground

plane is equivalent to the patch ground plane extended up to  $h=1.6\text{mm}$  from the patch edge. The ground plane has to be minimally maintained up to fringing field extension  $\Delta L$ , for the patch action to be proper. The ground plane is preserved up to  $h=1.6\text{mm}$  distance from the patch edge, in 8-element microstrip antenna array as shown in Fig. 5 and back lobe level is observed. Surface waves and space waves are the major concern in microstrip antennas.

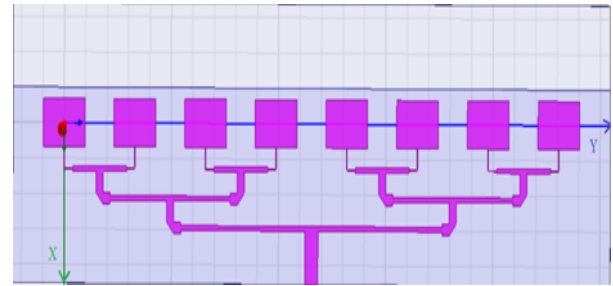


Figure. 5 Eight element antenna array with partial ground plane

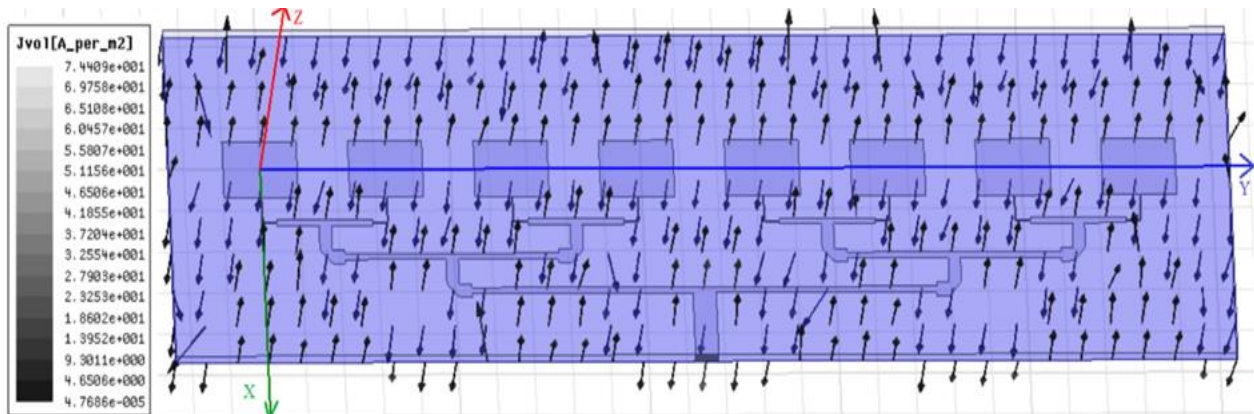


Figure. 6 Vector current density distribution in array with full ground plane

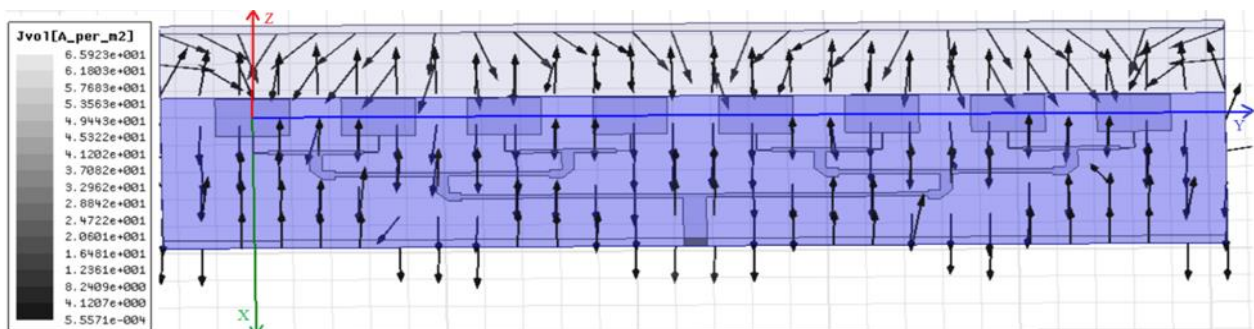


Figure. 7 Vector current density distribution in array with partial ground plane

When patch array antenna is fabricated on substrate, back radiation occurs due to the surface waves. The ground plane or substrate can diffract the surface waves and space waves and leads to more back radiation. Especially when the substrate with more thickness and dielectric constant are taken, the surface wave power will be more scattered in back ward direction and lead to more back lobe level. The E-plane edge diffraction effects are more dominant than the H-plane edge diffraction effects [20] and its influence will decrease if the length of the ground plane is reduced in the direction of feed as shown in Fig.5.

From Fig.6 and Fig.7, it is very clear that back ward (towards bottom side) diffraction is more prominent at the edges in case of array with full ground plane compared to array with partial ground plane.

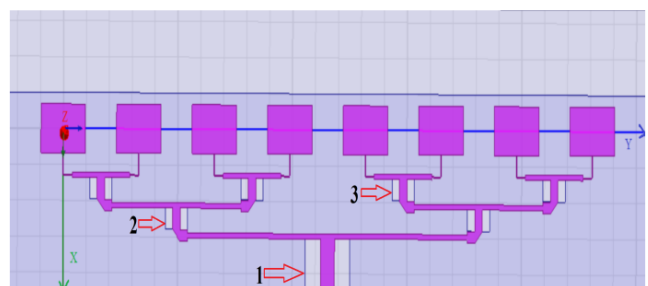


Figure. 8 Eight element microstrip antenna array with partial ground plane and DGS slots

The array with partial ground plane has a limitation of poor return loss when compared to full ground plane as depicted in Fig.12. In order to improve return loss as well as to inhibit feed line radiation to some extent, DGS slots are kept on either sides of feed lines at 3 stages of corporate feed network as shown in Fig. 8.

Defected ground structure (DGS) is a novel concept introduced to improve the performance of antenna. It is a defect that is intentionally placed in the ground plane of printed antennas. The defect is placed by etching out the ground plane with appropriate size and shape. DGS can be applied for different patch structures like triangular, rectangular, circular etc. [21, 22]. DGS can be used to increase impedance bandwidth, gain and to achieve low sidelobe level. It can be used for reducing Cross-pol radiation and mutual coupling effect, by choosing optimized dimensions of DGS [23-25]. It can also be used in the multiband antenna design, for size reduction of antenna etc. DGS can be modelled by three different equivalent circuits depending up on the geometry and size of DGS [26, 27]. They are LC and RLC equivalent circuits,  $\Pi$  shaped equivalent circuit and Quasi-static equivalent circuit. Most of the DGS is represented as parallel RLC resonant circuit connected to transmission lines at its both sides as shown in Fig.9. Here  $Z_0$  is the characteristic impedance of the transmission line. Depending on the shape of DGS, it can exhibit filtering action.

In this paper, rectangular DGS slots are kept adjacent to the T-junctions of feed line network as shown in Fig. 8, to decrease  $S_{11}$  further and to enhance the front to back ratio. The dimensions of type-1 DGS slot are 3.058mmX7.28mm and type-2&3 DGS slot is 1.62mmX2.99mm. The widths of these DGS slots are optimized widths. The lengths are taken same as the lengths of feed lines at the corresponding stage of the feed line network.

#### 4. Results and discussions

Single patch antenna with optimized dimensions is taken and ground plane is reduced to 63% as discussed in section 3, to reduce back lobe level. Fig. 10 shows the  $S_{11}$  comparison of single patch with full and partial grounds respectively. With full ground, the  $S_{11}$  is -35.6dB and with partial ground (63%) it is -18.29dB at 9.1GHz. Fig. 11 shows the normalized gain plot with full and partial grounds respectively. As discussed in section 3, the back lobe level has reduced from -18.09dB to -24.5dB with partial ground plane. The peak gain obtained with full ground plane is 5.54dB at 9.1GHz. whereas it is 6.15dB with partial ground plane.

Fig. 12 shows the comparison of  $S_{11}$  for 8 element array in three different cases of ground plane. The  $S_{11}$  is -15.6dB at 9.1GHz with full ground plane. Whereas, -14.9dB with partial ground plane

(as discussed in section 3). In order to improve  $S_{11}$ , the DGS slots are kept along with partial ground plane. As a result, the  $S_{11}$  has decreased drastically to -22.6dB at 9.1GHz. Fig. 13 shows the normalized gain comparison of 8 element array with full ground and partial ground cum DGS. The back lobe has reduced from -13.7dB to -18.8dB because of partial ground and DGS. The side lobes are also decreased to some degree.

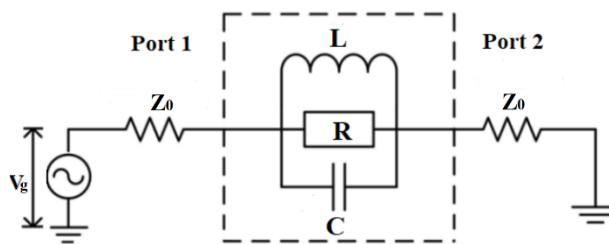


Figure. 9 RLC equivalent circuit for unit DGS

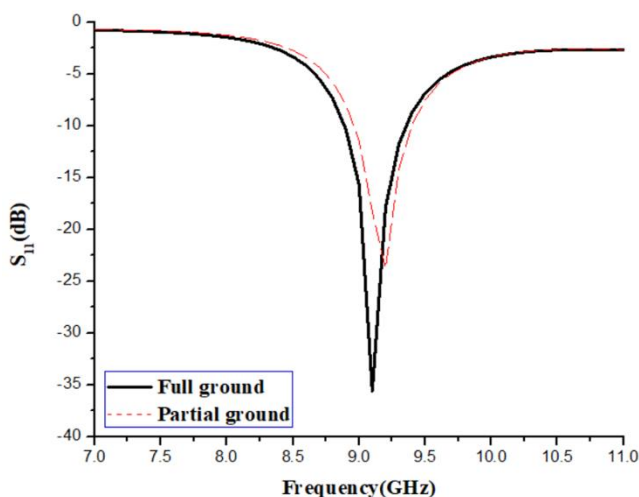


Figure. 10  $S_{11}$  plot for single patch antenna in two cases

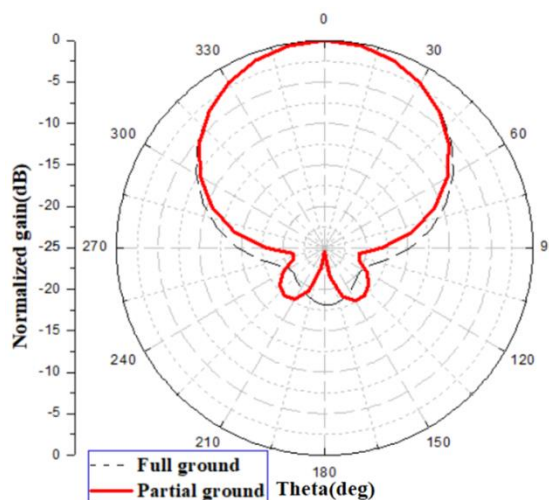


Figure. 11 H-plane pattern for single patch antenna in two cases

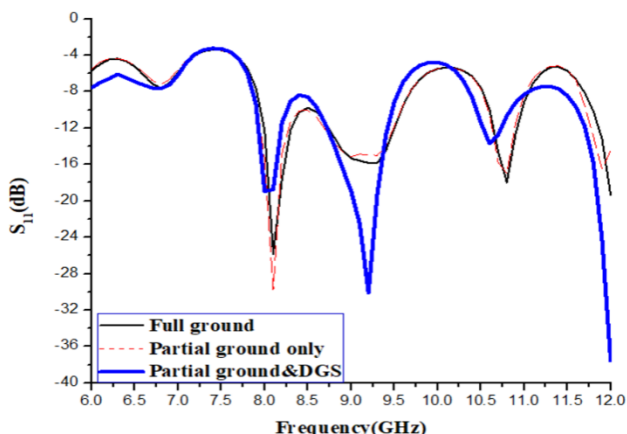


Figure. 12  $S_{11}$  plot for 8 element array in three different cases of ground plane

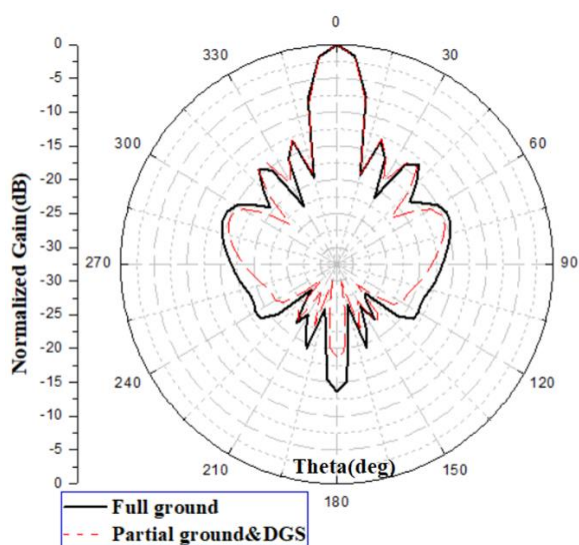


Figure. 13 H-plane pattern for 8 element array in two cases

Table 3. Performance comparison of 8 element array with different ground planes at 9.1GHz

S.No.	Parameters	Full ground plane	Partial ground plane	Partial ground & DGS
1	$S_{11}$ (dB)	-15.59	-14.92	-22.59
2	Peak Sidelobe level(dB)	-13.26	-13.16	-13.67
3	Back lobe level(dB)	-13.72	-18.27	-18.82
4	Peak Gain(dBi)	12.04	12.32	12.41
5	Radiation efficiency%	60.70	59.97	59.66
6	FBR (dB)	19	22.46	24.23
7	FNBW(deg)	30	30	30

The front to back ratio with full ground plane is 19dB and it has increased to 24.23dB because of partial ground cum DGS. Table 3 gives the comparison of different parameters in three cases

at 9.1GHz. Fig. 14 shows the peak gain versus frequency for 8 element array with full ground and partial cum DGS ground.

Fig. 15 shows the Front to back ratio (FBR) at different frequencies in three cases of ground plane. Highest FBR is observed at 9.1GHz, with partial ground and DGS. FBR with partial ground and DGS is more compared to FBR with full ground plane over 8.7GHz to 10.4GHz.

Fig. 16 shows  $S_{11}$  plot for 8 element array with partial ground and DGS. The simulation value of  $S_{11}$  is -22.59dB at 9.1GHz. Whereas, the measured value is -19.95dB at 9.1GHz. A difference of 2.64dB is observed between simulated and measured values. Fig. 17 (a)-(b) shows the simulation and measured values of H-plane Co-pol and Cross-pol patterns of 8 element array with partial ground and DGS. Cross-pol levels below -40dBi are observed in H-plane pattern.

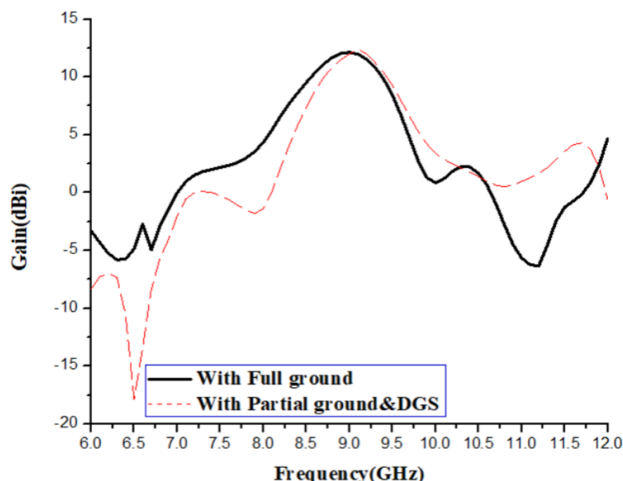


Figure. 14 Peak gain versus frequency plot for 8 element array

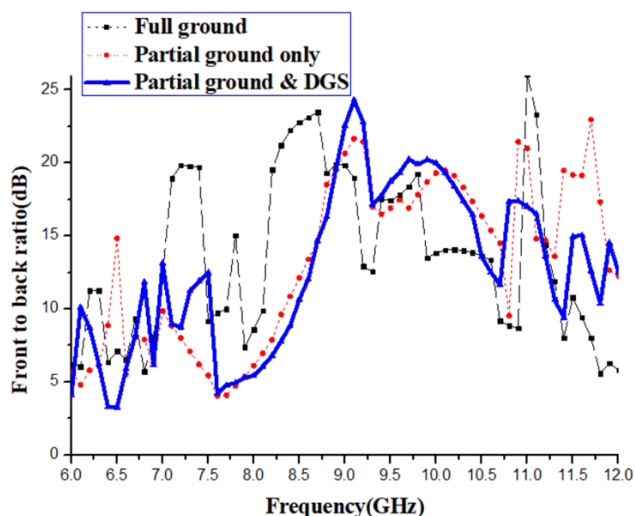


Figure. 15 Front to back ratio versus frequency plot for 8 element array

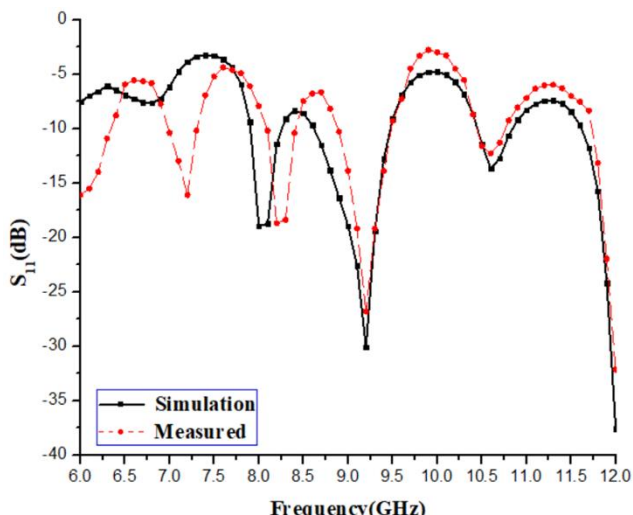


Figure. 16  $S_{11}$  plot for 8 element array with partial ground & DGS

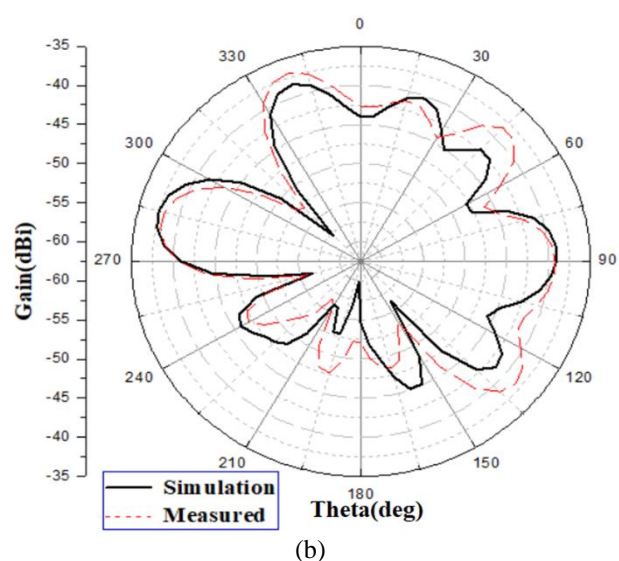
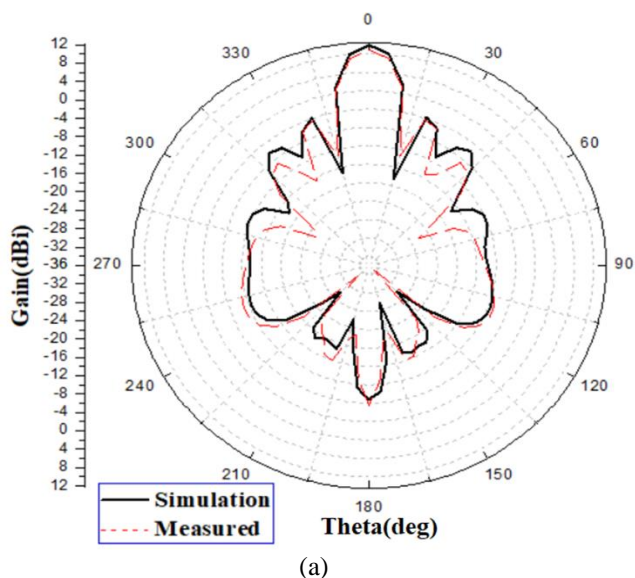


Figure. 17 Simulation and measured values: (a) H-plane co-pol pattern and (b) H-plane Cross-pol pattern

Fig. 18 (a) and (b) shows the top surface and ground plane of single microstrip patch antenna (with partial ground plane) respectively. Fig. 19 shows the 8 element microstrip array with full ground plane. Fig. 20 (a) and (b) shows the top surface and ground plane of the array (with partial ground & DGS) respectively. Fig. 21 (a) and (b) shows the orientation of 8 element array with partial ground plane & DGS, for Co-pol and Cross-pol measurements respectively.

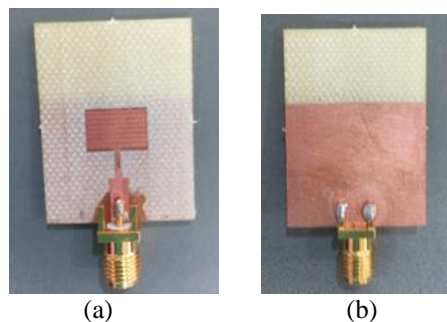


Figure. 18 Single microstrip patch antenna: (a) front view of patch and (b) ground plane of patch



Figure. 19 Eight element microstrip array with full ground plane

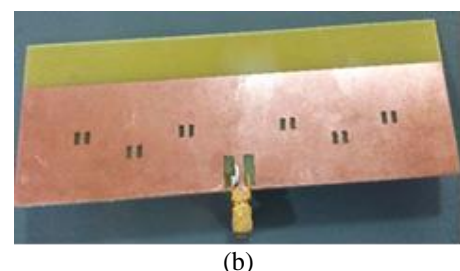
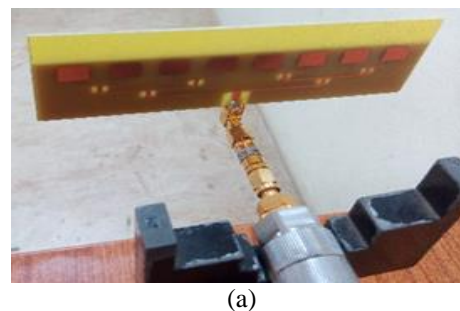
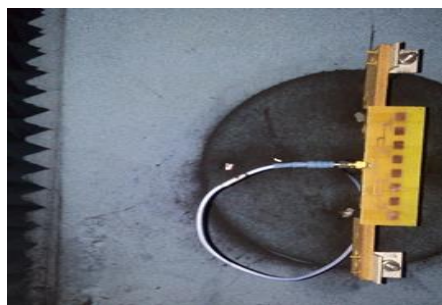


Figure. 20 Top surface and ground plane: (a) eight element array with partial ground plane & DGS and (b) ground plane of array with partial ground & DGS



(a)



(b)

Figure. 21 Orientation of 8 element array: (a) orientation of array (with partial ground & DGS) for Co-pol measurement and (b) orientation of array (with partial ground & DGS) for Cross-pol measurement

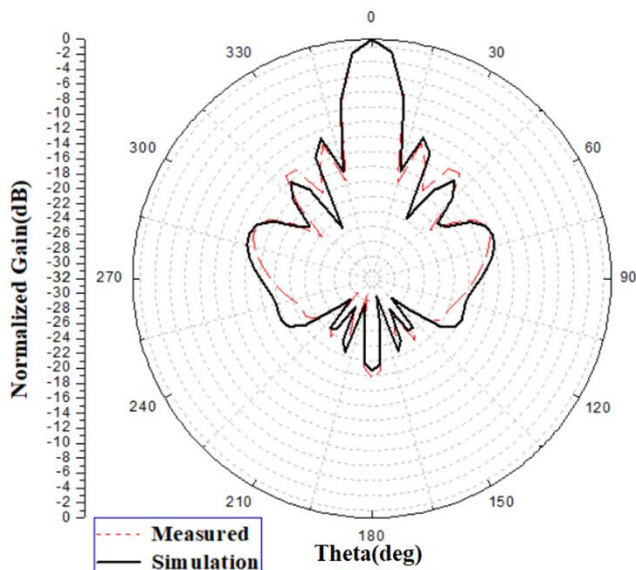


Figure. 22 Normalized gain plot of array with partial ground & DGS

Table 4. Comparison of proposed technique with references

Ref.	Technique used	Freq. (GHz)	No. of elements	Gain (dBi)	FBR(dB)
E. S. Silveira et al. [3]	Asymmetric positioning of antenna with respect to ground	2.5	1x8	Not available	>20
E Guo et al. [5]	EBG structure as a reflector	4.90-5.42	Single Yagi array with 6x4 reflector	8.5-9.5	>15
Z. Qamar, et al. [13]	metamaterial superstrate	3.6	1x2	4.37	20
K. Kumar and S. Dwari [16]	Slot on SIW cavity	9.44	1	7.2	>17.3
D. Chaturvedi et al. [17]	SIW cavity resonator	5.8	1	5.85	>19
Present paper	Partial ground & DGS technique	9.1	1x8	12.41	24.23

Fig. 22 shows the normalized gain plot of the array with partial ground and DGS. A difference of 0.96dB is observed between the simulated and measured back lobe level. Also a difference of 0.82dB is observed between the simulated and measured peak sidelobe level. Table 4 shows the comparison of current technique with some of the existing techniques. Size reduction of 28.86% is achieved with this technique as shown in Table 5. The simulations are done using ANSYS HFSS version-18 and practical measurements are done using VNA E5071C and anechoic chamber.

Table 5. Calculations for Size reduction of Antenna array

Full ground area(FGA)	$139 \times 39 = 5421\text{mm}^2$
Antenna top surface area(ATA)	$717\text{mm}^2$
Partial ground area(PGA)	$139 \times 27 = 3753\text{mm}^2$
Total DGS slots area(DA)	$104\text{mm}^2$
Antenna area without partial ground and DGS	$\text{FGA} + \text{ATA} = 6138\text{mm}^2$
Antenna area with partial ground and DGS	$\text{PGA} - \text{DA} + \text{ATA} = 4366\text{mm}^2$
% Size Reduction of antenna	$[(6138 - 4366) / 6138] \times 100 = 28.86\%$



## 5. Conclusion

A novel technique for back lobe reduction in microstrip antennas is proposed. Effect of partial ground and DGS in microstrip antennas is studied. When the ground plane is preserved up to  $h$  (substrate height) distance from patch edge, the back lobe level has reduced by 5.1dB. When DGS slots are kept on either sides of feed line sections in feed network, the  $S_{11}$  has decreased from -14.92dB to -22.59dB along with improvement in front to back ratio. The FBR has increased from 19dB to 24.23dB, by using this combined technique of partial ground and DGS. The peak gain has also improved from 12.04dBi to 12.41dBi, without much change in radiation efficiency. This technique can be applied in the design of satellite, missile and aircraft antennas to minimize EMI between on-board antennas. By choosing low dielectric substrates like Rogers RT/duroid 5880 and so on, still back lobe level can be reduced.

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