A MODIFIED VIRTUAL SPACE VECTOR MODULATION TECHNIQUE FOR Z-SOURCE NPC INVERTERS

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Abstract*: A modified virtual space vector modulation approach for the control of a Z-source neutral point clamped inverter is presented in this paper. This approach works perfectly for the traditional neutral point clamped inverter. In this paper, the effectiveness of the virtual space vector modulation technique in balancing the input capacitor voltages of the Z-source NPC inverter with no low-frequency oscillations superimposed in addition to voltage buck-boost capability is demonstrated through simulations in SABER®. A prototype converter is used to capture experimental results for validation.*

1. INTRODUCTION

Neutral-point-clamped (NPC) inverters are used in both medium-voltage high-power and low-power systems. Their popularity is attributed to merits like better harmonic performance, reduced switching losses, low dv/dt, smaller filter volume, and better electromagnetic compatibility [1]. Unfortunately, the ac peak output voltage that it can synthesize is always less than the input dc source. Thus in many applications a dc-dc boost converter is required at the input stage to meet the required output value. The resulting system becomes more complicated and its control can be difficult [2]. The Z-source NPC (ZNPC) inverter overcomes these limitations. The ZNPC inverter topology has received a lot of attention in the research community and is expected to find application in photovoltaic (PV) power systems [3]. It has also been explored for motor drive applications

such as hybrid electric vehicles [4]. The ZNPC inverter adjustable speed drive (ASD) system has several unique advantages that are very desirable for many ASD applications, such as ride-through capability during sags, reduced line harmonics, improved power factor and reliability, and extending the output voltage range. However, this converter inherits one particular problem of the conventional NPC inverter: unbalanced input capacitor voltages [5, 6].

In many applications, well balanced capacitor voltages are required otherwise increased harmonics and damage of switching devices may result. As a result, there have been much efforts to solve the capacitor voltage balancing problem [7-9]. The capacitor voltage balancing control methods are grouped based on the pulse width modulation (PWM) methods. These include carrier-based sinusoidal PWM (CBSPWM) [10-12], space vector PWM (SVPWM) [8, 13-15], and selective harmonic elimination PWM (SHEPWM) [16]. SVPWM method offers low noise, small ripple, better dc utilization as well as easy implementation in a microcontroller [17] and therefore has attracted more attention.

For the conventional three-level SVPWM, the capacitor voltages can be balanced through adjustment of the redundant small vectors' duration [5, 6, 9, 13, 18]. In [15], an SVPWM-based capacitor voltage controller that uses the direction of load currents was proposed. In this method, redundant voltage vectors were distributed to ensure small current flows through the neutral point (NP) so as to achieve capacitor voltage balance. The idea behind most SVPWM schemes is to select three nearest vectors to form the reference vector. However, these methods are not capable of balancing the capacitor voltages for high modulation index and low power factor [17]. Virtual space vector modulation (VSVM) was proposed to overcome this problem [19].

Several variants of the VSVM technique have been reported in the literature to balance the capacitor voltage of the conventional NPC inverter and some of its derived topologies [17, 19, 20]. Nevertheless, none of these techniques has been verified with the ZNPC inverter in the literature. This creates a research gap since the ZNPC inverter is expected to replace the NPC inverter in most applications where the dc source may not be constant but the output ac voltage needs to be controlled to obtain a favourable value for the load. In this paper the VSVM technique proposed in [19] for controlling the conventional NPC inverter is modified and applied to the ZNPC inverter to verify its effectiveness in modulating this converter. Applying this modified VSVM technique to the ZNPC inverter enables the inverter to perform voltage buck-boost function in addition to balancing input capacitor voltages with all low-frequency oscillations completely eliminated.

The main advantage of the VSVM technique over the conventional SVPWM technique is its ability to eliminate completely low-frequency oscillations of the capacitor voltages. Capacitor voltage oscillation increases the voltage stress on power devices which may lead to premature failure of the converter. However, this benefit in capacitor voltage balance is achieved at the expense of an increased number of commutations compared to the

conventional SVPWM strategy. The increase in commutations is due to the fact that the VSVM technique always employs five different switching states per switching cycle while the conventional SVPWM uses only four for high modulation index and majority of switching cycles. The additional commutations may lead to an increase in switching losses.

In section 2, a brief review of the ZNPC inverter circuit is presented. The modified VSVM technique for controlling this converter is explained in section 3. Simulation as well as experimental results are presented in section 4 to verify the effectiveness of the VSVM technique in modulating the ZNPC inverter.

2. REVIEW OF Z-SOURCE NPC INVERTER

Figure 1 shows the circuit configuration of the ZNPC inverter. The reference is taken as the neutral point, "o". Each output phase leg has three values: $V_i/2$, 0, $-V_i/2$. With operation as a traditional NPC inverter, V_i equals $2V_{DC}$ which is also the maximum output line-to-line voltage obtainable.
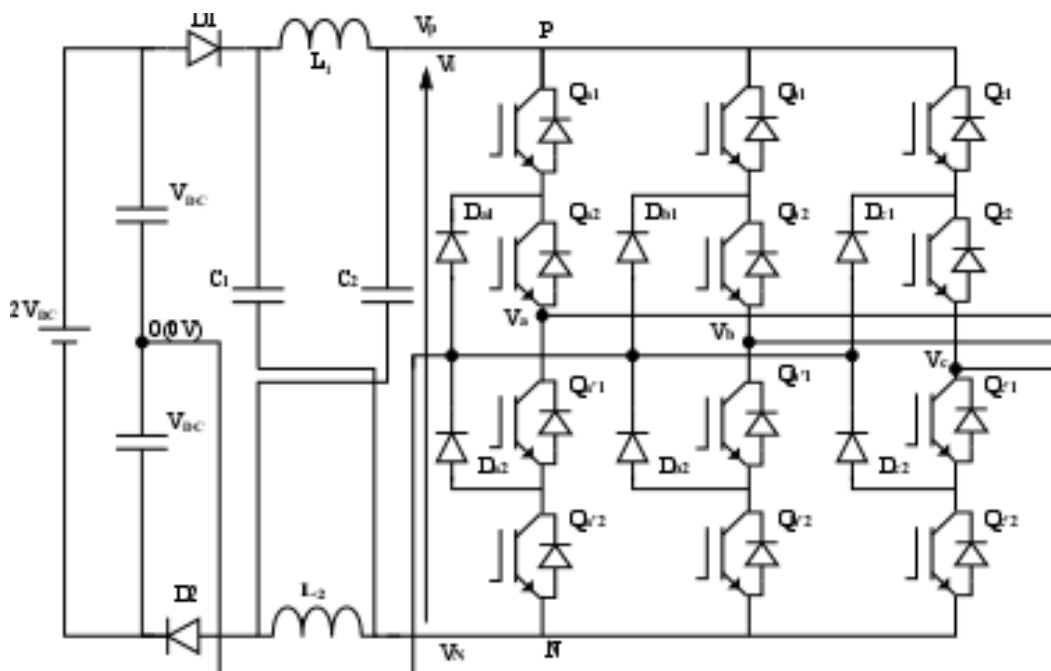

Fig. 1. Z-source NPC inverter

If shoot-through states are introduced into phase legs, an output line-to-line voltage greater than the available dc voltage can be obtained. Thus, ZNPC inverter can step down and step up the output voltage with a single stage structure.

The ZNPC inverter can be operated either with full-shoot-through states or partial-shoot-through states. In this work, partial-shoot-through method is selected since it produces output waveforms with better harmonic content [21].
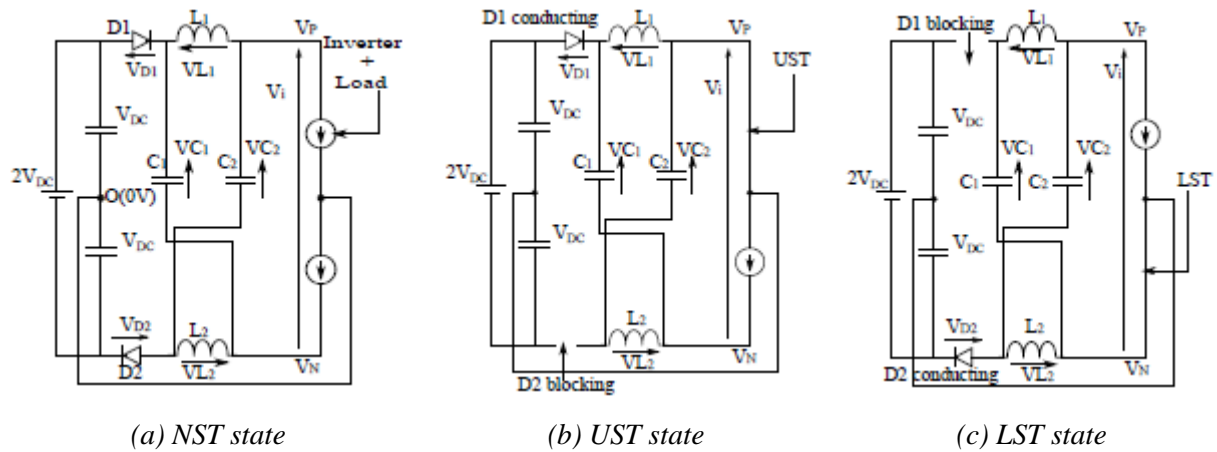
(a) NST state   *(b) UST state*   *(c) LST state*

Fig. 2. Simplified representation of ZNPC inverter during (a) NST, (b) UST and (c) LST states

Figure 2 shows the simplified equivalent circuits of ZNPC inverter in different states. It is assumed the impedance network is symmetrical. Voltage equations for non-shoot-through (NST) states are given as:

$$V_{L1} = 2V_{DC} - V_{C2} \tag{1}$$

$$V_{L2} = 2V_{DC} - V_{C1} \tag{2}$$

$$V_P = +V_i/2 \tag{3}$$

$$V_N = -V_i/2 \tag{4}$$

$$V_i = V_{C1} + V_{C2} - 2V_{DC} \tag{5}$$

In a similar manner, voltage equations during upper-shoot-through (UST) states are given by:

$$V_{L1} = V_{DC} \tag{6}$$

$$V_P = 0 \tag{7}$$

$$V_N = V_{DC} - V_{C1} \tag{8}$$

and voltage equations for lower-shoot-through (LST) states are given as:

$$V_{L2} = V_{DC} \tag{9}$$

$$V_P = -V_{DC} + V_{C2} \tag{10}$$

$$V_N = 0. \tag{11}$$

Let the switching period be T_{sw} and the combined time of shoot-through states be T_{st}. For symmetrical operation T_{st} is shared equally between UST and LST states. Performing inductor voltage averaging over one switching period, we have:

$$V_{C1} = V_{C2} = V_C = 2V_{DC} \cdot \left\{ \frac{1 - 0.5T_{st}/T_{sw}}{1 - T_{st}/T_{sw}} \right\}. \tag{12}$$

Using (12) and (5), the dc-link voltage for NST states is given as:

$$V_{i\_NST} = \frac{2V_{DC}}{1 - T_{st}/T_{sw}}. \tag{13}$$

Similarly, putting (12) into (8) and (10), the dc-link voltage for UST and LST states are given by:

$$V_{i\_UST} = V_{i\_LST} = \frac{V_{DC}}{1 - T_{st}/T_{sw}}. \tag{14}$$

Obviously, the lower dc-link voltage occurs during LST and UST states when energy is stored in inductors according to (14). This energy is released to capacitors during NST states for voltage boosting. The fundamental ac peak output line-to-line voltage for the ZNPC is given by [21, 22]:

$$\hat{V}_{ll} = m_I . V_{\_NST} = m_I . B . 2V_{DC}, \tag{15}$$

where

$$B = 1/(1 - T_{st}/T_{sw}). \tag{16}$$

In (15), $m_I \leq 1$ represents the modulation index whiles $B \geq 1$ represents the boost factor.

3. MODIFIED VSVM APPLIED TO Z-SOURCE NPC INVERTER

In this section, a modified VSVM strategy applied to the ZNPC inverter is presented. This modulation strategy is derived from the VSVM technique proposed in [19] which has

been proved to work very well for the conventional NPC inverter. The VSVM technique in [19] was developed by modifying the conventional SVPWM strategy to mitigate the problem of unbalanced input capacitor voltages. For a conventional SVPWM strategy, the reference vector is formed by selecting three nearest vectors. At times more than one switching state can be used to generate a vector. In such situations a combination of these switching states is used for controlling capacitor voltages.

Figure 3 shows the space vector diagram (SVD) with switching states and associated NP current for a conventional NPC inverter modulated using the conventional SVPWM strategy. The SVD is divided into six sectors (I to VI) and contain twenty-seven switching states classified as zero (V_0), small (V_{S1} to V_{S6}), medium (V_{M1} to V_{M6}) and large (V_{L1} to V_{L6}) vectors. Switching state 'P' means the top two devices of a phase leg are gated on, 'O' means the two middle devices are gated on while 'N' signifies the two bottom devices are turned on. If any output phase leg is in the 'O' state, there will be unequal charging/discharging of the top and bottom input capacitors. This leads to unequal capacitor voltages. To balance capacitor voltages effectively, it is required that average NP current in a switching cycle be zero. The conventional SVPWM technique is unable to achieve this because it uses the NP currents of small vectors to compensate those introduced by the medium vectors and it is not possible for the NP current introduced by the medium vectors to be fully compensated by those introduced by the small vectors. This is especially so when the modulation index is high and the power factor is low.
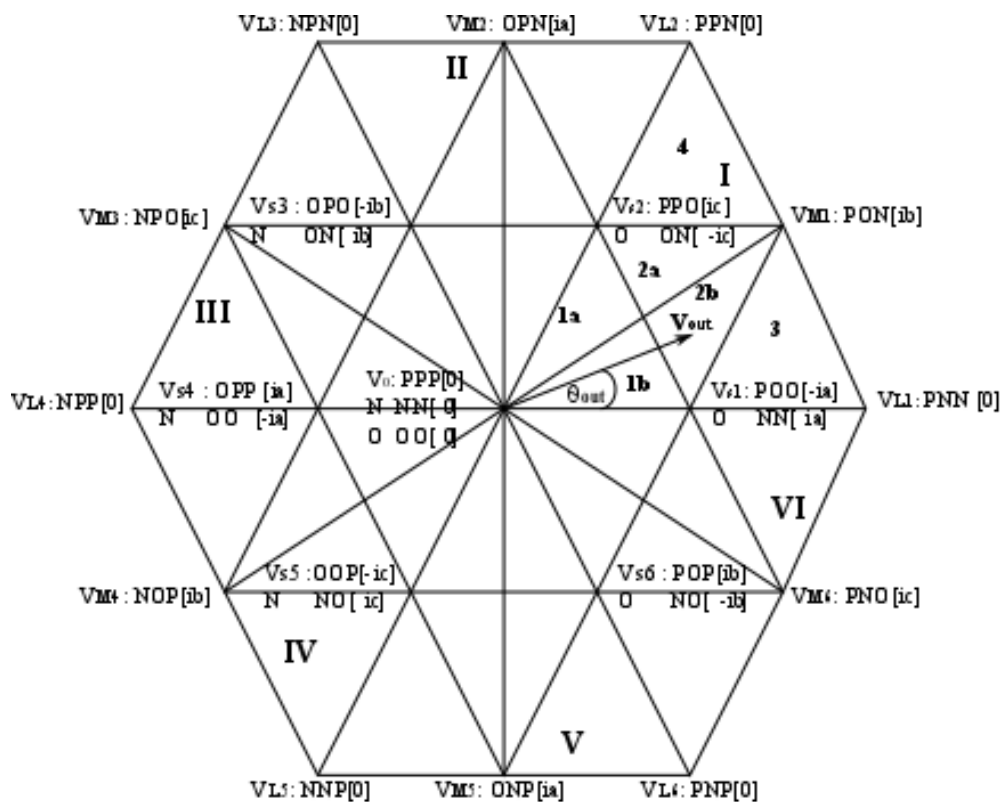

Fig. 3. Space vector diagram of conventional NPC inverter

In the VSVM technique, a new set of virtual vectors is defined to balance the capacitor voltages effectively. These virtual vectors are formed by combining vectors associated with certain switching states of the SVD shown in f*ig. 3*. Then the reference vector in each switching cycle is synthesized with nearest three virtual vectors. The virtual vectors formed have associated average NP currents equal to zero [1, 17, 19]. The virtual vectors for sector I are shown in *fig. 4* where $k_5, k_6, k_7 \in [0, 1]$ and $k_5 + k_6 + k_7 = 1$. Also $k_1,$ $k_2, k_3, k_4 \in [0, 1]$ with $k_1 + k_2 = 1$ and $k_3 + k_4 = 1$. The case shown in *fig.4* represents the situation where $k_5 = k_6 = k_7 = 1/3$ and $k_1 = k_2 = k_3 = k_4 = 1/2$.

- V_{V0} is formed with V_0, which obviously generates a NP current equal to zero because all output terminals are connected to an identical dc-link point, so there is no current flowing in the input capacitors.

- V_{VSi} are obtained from an equal combination of two switching states having the same associated NP current but opposite in sign. For example, if vector V_{VS1} is selected for a period of time $t_x,$ switching state ONN will be active for $0.5t_x$, and POO will be active for the remaining $0.5t_x$. Therefore, the average NP current during t_x will be:

$$\frac{1}{t_x}\{0.5.\,t_x.\,(i_a) + 0.5.\,t_x.\,(-i_a)\} = 0 \tag{17}$$

- V_{VMi} are obtained from an equal combination of three switching states having an associated NP current equal to i_a, i_b and i_c, respectively, and $i_a + i_b + i_c = 0$. For instance, if vector V_{VM1} is selected for a period of time t_z, switching state ONN will be active for $0.333t_z$, PON will be active for $0.333t_z$, and PPO will be active for $0.333t_z$. Therefore, the average NP current during t_z will be:

$$\frac{1}{t_z}\{0.333.\,t_z.\,(i_a) + 0.333.\,t_z.\,(i_b) + 0.333.\,t_z.\,(i_c)\} = 0 \tag{18}$$

- V_{VLi} are obtained from the switching states that define V_{Li}, all of them having an associated NP current equal to zero.
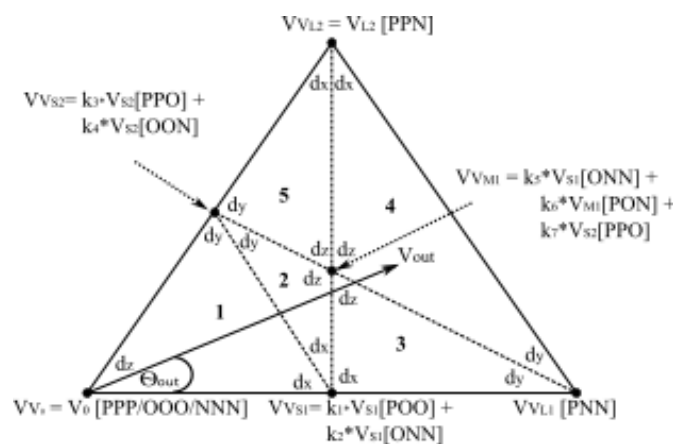

Fig. 4. Virtual space vectors for sector I

The duty ratios of selected virtual vectors in a switching cycle can be calculated as:

$$d_x . V_{V1} + d_y . V_{V2} + d_z . V_{V3} = \vec{V}_{out} \tag{19}$$

$$d_x + d_y + d_z = 1 \tag{20}$$

where V_{Vj} corresponds to the jth selected virtual vector {j=1, 2, 3}. The duty cycles of different switching states forming the virtual vectors can then be determined.

Finally, a decision of the application of different switching states over a switching cycle is made. The order of chosen switching states' is such that connection of each phase to the dc-link points (p, o, n) is symmetrical. For instance, virtual vectors V_{VM1}, V_{VL1} and V_{VL2} are selected to form the reference vector in triangle 4 of sector I. Using the VSVM technique, these virtual vectors are formed from V_{S1} (ONN), V_{S2} (PPO), V_{M1} (PON), V_{L1} (PNN) and V_{L2} (PPN). These vectors can then be applied to the output using the switching sequence: PPO → PPN → PON → PNN → ONN. For a switching period, T_{sw}, the active time of each vector is determined using (21) to (25).

$$t_1[PPO] = k_7 . d_z . T_{sw} \tag{21}$$

$$t_2[PPN] = d_x . T_{sw} \tag{22}$$

$$t_3[PON] = k_6 . d_z . T_{sw} \tag{23}$$

$$t_4[PNN] = d_y . T_{sw} \tag{24}$$

$$t_5[ONN] = k_5 . d_z . T_{sw} \tag{25}$$

In [19], the modification to the VSVM technique is seen in the switching sequence of the vectors applied to the output. The switching sequence is modified by introducing shoot-through states in phase legs of the ZNPC inverter for it to perform voltage buck-boost operation. Only the application of UST and LST states is considered in this work. An UST state means three top devices in a phase leg are turned on while a LST state represents turning on of three lower devices in a phase leg. A PWM switching sequence for achieving this goal is derived as discussed next.

Consider switching sequence PPO → PPN → PON → PNN → ONN for a conventional NPC inverter. An UST state can be inserted in a phase leg provided it is in the "O" state and the other phases are in the "N" or "O" state otherwise there will be a collapse of the output line-to-line voltages. In a similar way, a LST state can be inserted in a phase

leg if it is in the "O" state and the other two phases are in the "P" or "O" state [21]. Based on this reasoning, a LST state is introduced next to PPO (PPL) since this will not affect the output line-to-line voltage. Similarly, an UST is introduced next to ONN (UNN) with no adverse effect on the output line-to-line voltage. No UST or LST state can be introduced next to PON because that will breach the condition for insertion of shoot-through states. The resulting modified PWM sequence for the ZNPC inverter is shown in *fig*. 5 for triangle 4 of sector I.
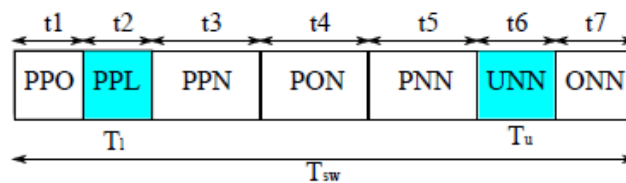
Fig. 5. Example VSVM switching sequence for the ZNPC inverter

4. RESULTS AND DISCUSSION

A simulation exercise in SABER® was undertaken to verify the modified VSVM technique for controlling the ZNPC inverter. The simulation results have been validated experimentally with a laboratory prototype. The parameters used for the simulation and experimental studies are presented in Table 1.

Table 1. Parameters used for simulation and experimental studies

| Symbol	Description	Value
$2V_{DC}$	Input dc voltage	120 V
C_{up}, C_{dn}	Input capacitors	100 μF
$L_{1,2}$	Inductors for Z-source network	1 mH
$C_{1,2}$	Capacitors for Z-source network	470 μF
L_{load}	Load inductance	20 mH
R_{load}	Load resistance	10 Ω
f_{out}	Output frequency	50 Hz
f_{sw}	Switching frequency	5 kHz

4.1. Simulation results

The main contribution of this paper is the balancing of input capacitor voltages to eliminate low-frequency oscillations in a ZNPC inverter. The ability of this converter to perform voltage buck-boost function with the introduction of shoot-through states is also demonstrated. These are shown through simulation analysis presented next.

The circuit diagram of the model used for the simulations as well as the experimental validation is shown in *fig.1*. The converter is supplied with a dc voltage of 120 V via two series connected input capacitors. A Z-source network comprising two inductors, two capacitors and two diodes connects the input capacitors to the NPC circuit. The NPC circuit comprises three phase legs with each leg consisting of four IGBTs with anti-parallel diodes and two clamping diodes. An R-L load consisting of 10 Ω resistors and 20 mH inductors was used. The ZNPC inverter was initially operated as a conventional NPC inverter using the VSVM technique described earlier with a modulation index of 0.9 and shoot-through ratio of 0, respectively. With this mode of operation, the output line-to-line voltage is expected to have a fundamental component of 0.9 x 120 = 108 V. This is obvious as shown in *fig. 6 (a)* with a peak fundamental component of 106.6 V.
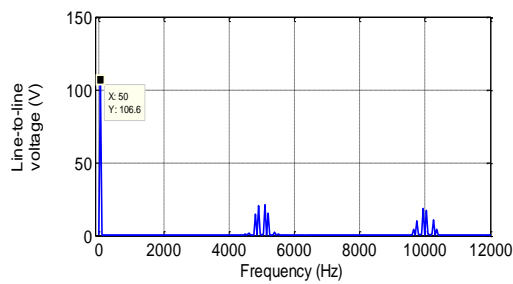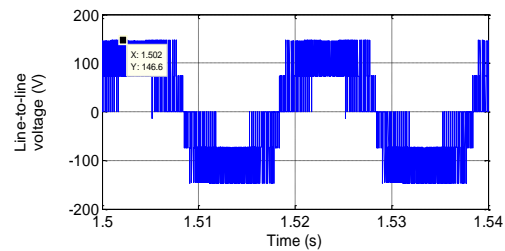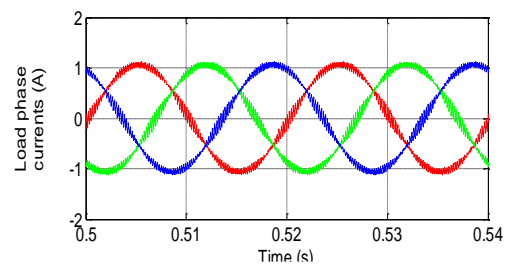

(a) FFT of line-to-line voltage, see (15)
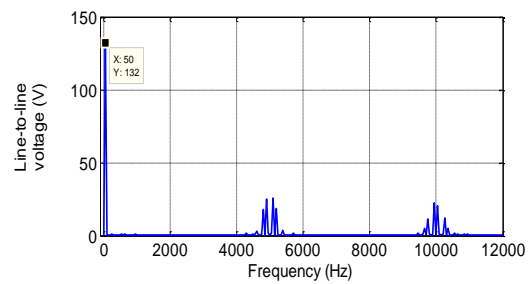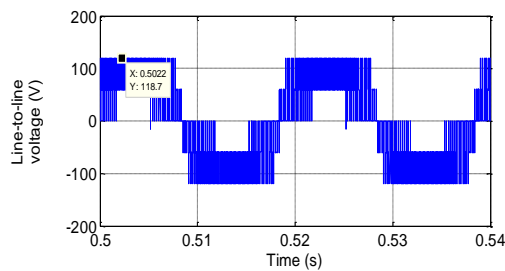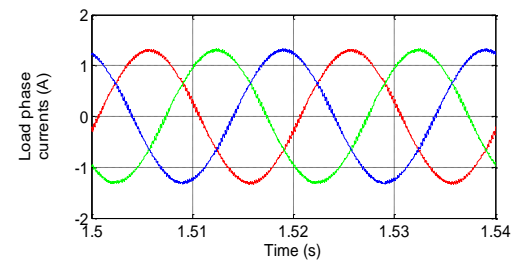

(b) Line-to-line voltage

(c) Load phase currents

(d) Input capacitor voltages

(a) FFT of line-to-line voltage, see (15)

(b) Line-to-line voltage

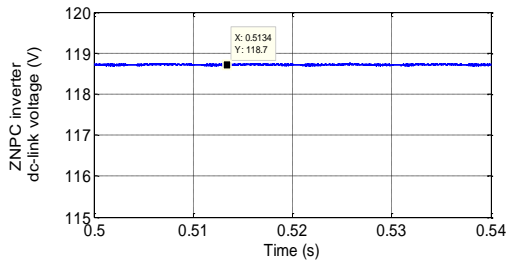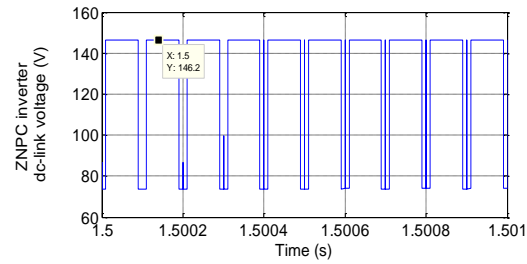*(c) Load phase currents*
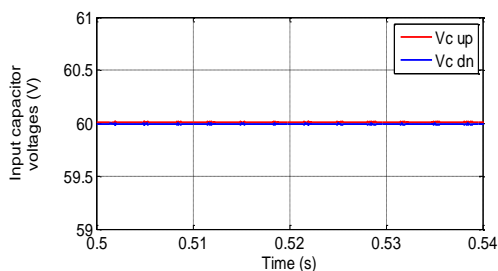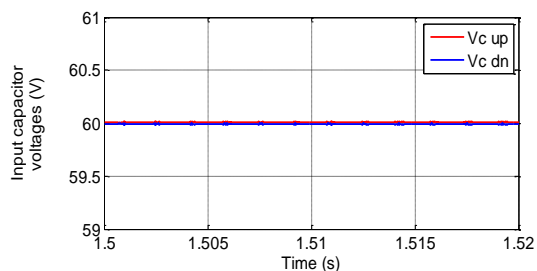
(d) Input capacitor voltages

(e) DC-link voltage seen by NPC circuit, see (13)

Fig. 6. Simulation results for voltage-buck operation

(e) DC-link voltage seen by NPC circuit, see (13) and (14)

Fig. 7. Simulation results for voltage-boost operation

The dc-link voltage appearing at the output of the Z-source network is clearly not stepped up and the output line-to-line voltage has a peak value of 118.7 V (*fig. 6(b)*) taking into consideration the voltage drops in the diodes. The corresponding load currents are shown in *fig. 6(c)*. The voltages of the input capacitors are also shown in *fig. 6(d)* where it is noted that they are well balanced with no low-frequency oscillations superimposed on them. Similarly, the dc-link voltage seen by the NPC inverter circuit stands at 118.7 V as expected (*fig. 6(e)*).

For voltage-boost operation, shoot-through states are inserted into selected phase legs as described earlier. Here the modulation index is maintained at 0.9 while shoot-through ratio is set to 0.2. This gives a boost factor of 1/0.8 (= 1.25) and hence the peak fundamental output line-to-line voltage expected is 108 x 1.25 (= 135 V). *Figure 7* shows the boosted waveforms. The FFT of the output line-to-line voltage shows a fundamental value of 132 V (*fig. 7(a)*). A boosted dc-link voltage of 146.6 V is shown in *fig. 7(b)*. The corresponding boosted load currents are shown in *fig. 7(c)*. The input capacitor voltages are shown in *fig. 7(d)* where it is clear that they are well balanced with all low-frequeny oscillations eliminated completely. The Z-source network output voltage is shown in *fig. 7(e)*. This clearly shows two levels of 146.2 V and 73.1 V, respectively, in accordance with (13) and (14).

4.2. Experimental results

To validate the simulation work carried out in section 4.1 an experimental prototype converter was set up. A 120 V dc supply was used to power the ZNPC inverter. The Z-source network comprises two inductors and two capacitors connected in an X-shape between the dc source and the back-end NPC circuit. The NPC circuit consists of three APTGL60TL120T3G NPC modules comprising four series-connected IGBTs with anti-parallel diodes and two clamping diodes. Heat sinks are attached to the IGBT modules for cooling purposes. Converter modulation is implemented using a DSP and an FPGA with a

series of circuits which allow information such as gate drive signals and measurement signals to be transferred to and from the power PCB board. *Figure 8* shows a schematic of the entire system used for the converter control. Experimental results were taken with a LeCroy Waverunner 6050 oscilloscope using a combination of differential voltage and current probes.

First, a buck mode of operation was commanded by using a modulation index and shoot-through ratio of 0.9 and 0 respectively. For this mode, the expected peak value of the fundamental output line-to-line voltage is limited to 0.9 x 120 (= 108 V). *Figure 9(a)* shows the experimental waveform for this condition with an actual value of 105 V. It is clearly seen that this matches well with the simulation result presented earlier. *Figure 9(b)* shows the output line-to-line voltage where a peak value of 117.7 V is recorded. The corresponding load currents are shown in *fig. 9(c)*. This result matches well those shown in *fig. 6(c)*. The waveforms for the input capacitors are shown in *fig. 9(d)*. The result clearly shows balanced capacitor voltages with no low-frequency oscillations. Finally, *fig. 9(e)* shows the ZNPC inverter dc-link voltage which obviously matches that of simulation shown in *fig. 6(e)*.
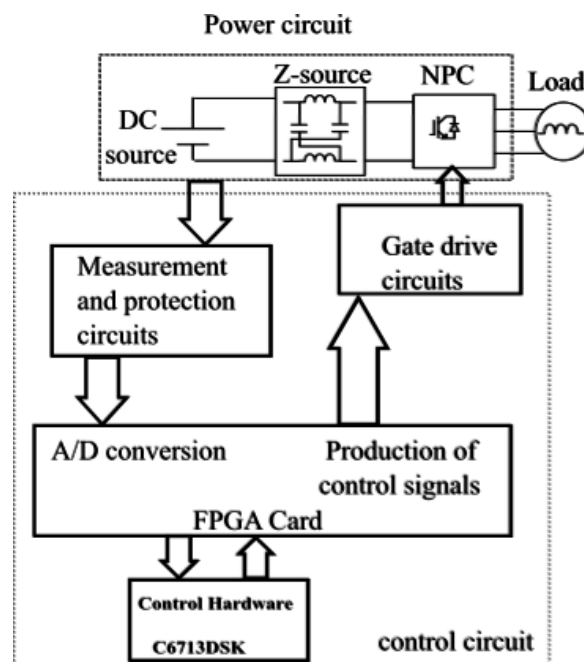

Fig. 8. Schematic of experimental set up

To command voltage-boost operation, the modulation index was maintained at 0.9 while the shoot-through ratio was set to 0.2. The boosted waveforms are shown in *fig. 10*. In these plots, we observe that there is a close matching with the simulation results. *Figure 10(a)* shows the boosted fundamental output line-to -line voltage with a peak value of 129.9 V. The corresponding output line voltage is shown in *fig. 10(b)*. The associated boosted currents are shown in *fig. 10(c)*, while the input capacitor voltages are shown in *fig. 10(d)*, respectively. The boosted ZNPC inverter dc-link voltage is also presented in *fig. 10(e)*.

These results clearly confirm effectiveness of the VSVM algorithm in balancing the input capacitor voltages of the ZNPC inverter in addition to voltage buck-boost operation.

(a) FFT of line-to-line voltage, see (15)

(a) FFT of line-to-line voltage, see (15)

(b) Line-to-line voltage

(b) Line-to-line voltage

(c) Load phase currents

(c) Load phase currents

(d) Input capacitor voltages

(d) Input capacitor voltages

(e) DC-link voltage seen by NPC circuit, see (13)

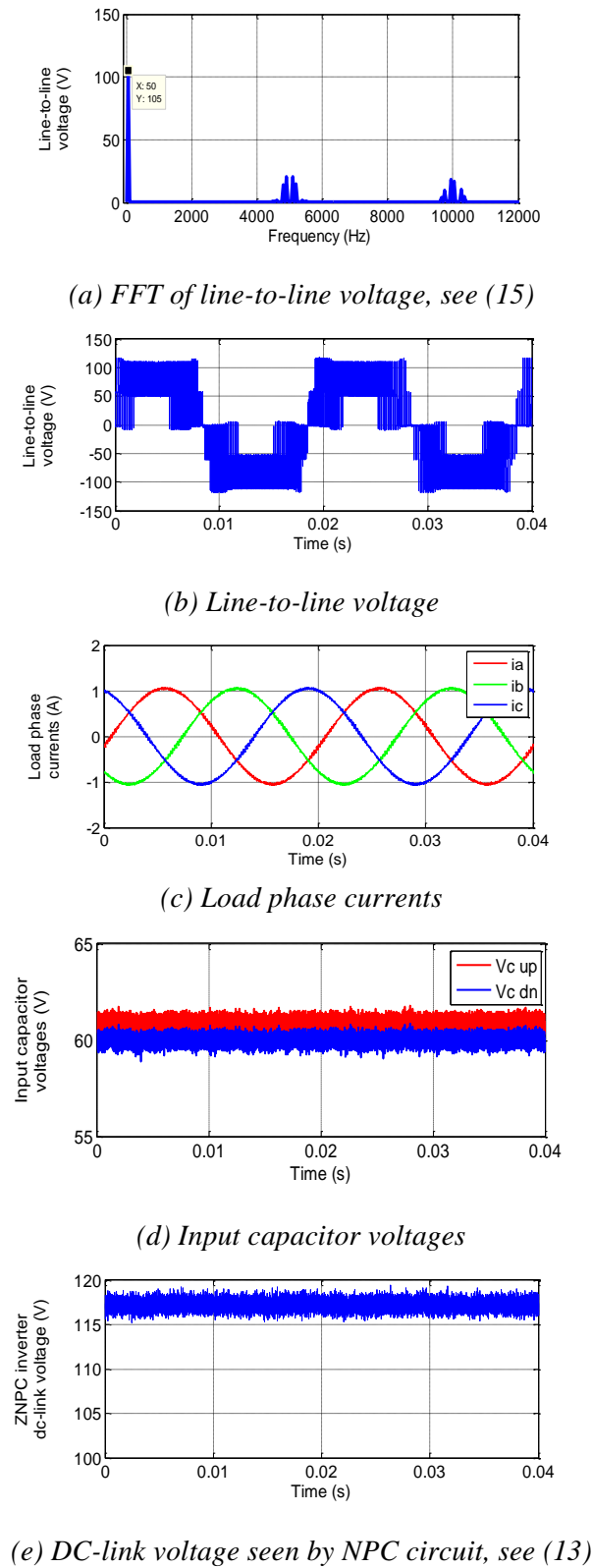*(e) DC-link voltage seen by NPC circuit, see (13) and (14)*

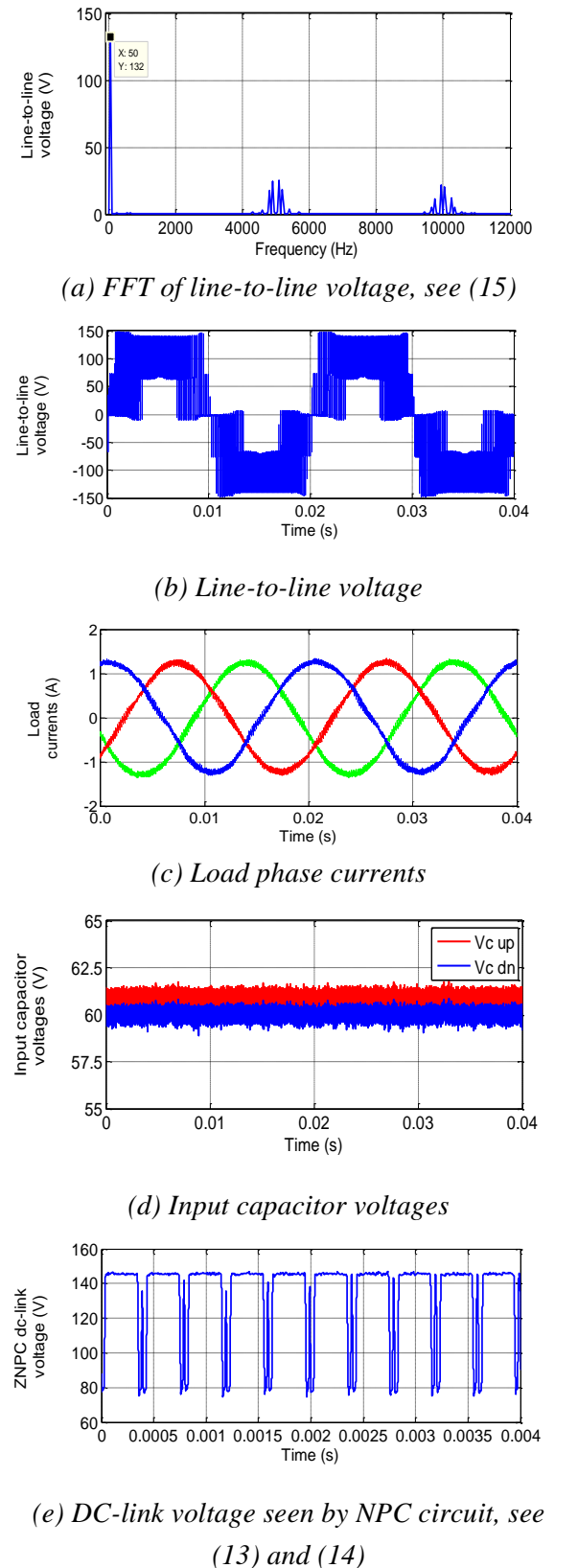*Fig. 9. Experimental results for voltage-buck operation*

Fig. 10. Experimental results for voltage-boost operation

5. CONCLUSIONS

A modified virtual space vector modulation approach used to control a Z-source neutral point clamped inverter has been presented. The ability of this converter to perform voltage buck-boost function has been verified. Balancing of the input capacitors of this converter by the modified virtual space vector modulation technique has also been confirmed through simulations and validated experimentally. The approach used here is superior to the conventional SVPWM in balancing the input capacitor voltages by eliminating completely all low-frequency oscillations on the capacitor voltages which may lead to premature failure of the converter. This benefit is however achieved at the expense of more switching commutations.

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