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Design & Analysis of Low-Power Low-Voltage Double-Tail Comparator

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Abstract- The need for ultra low-power, area efficient and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In the base paper, an analysis on the delay of the dynamic comparators will be presented and analytical expressions are derived. From the analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator design. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional double tail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. Post-layout simulation results in a 0.18-µm CMOS technology confirm the analysis results.

I. INTRODUCTION

Comparator is one of the building blocks in most of the Analog- to- Digital converter. High-speed comparators in ultra deep sub micrometer (UDSM) CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes [1]. Designing high-speed comparators is more challenging when the supply voltage is smaller. In this technology to achieve high speed, larger

transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Low –Voltage operation results in limited common-mode input range, which is important in many high-speed ADC architectures, such as flash ADCs.

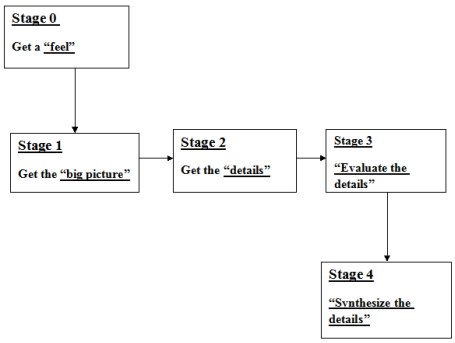
In electronics, a comparator is a device that compares two voltages or currents and outputs a digital signal indicating which is larger. It has two analog input terminals V_+ and V_- and one binary digital output V_o. The output is ideally

$$V0 = \begin{cases} 1, \text{if } V_+ > V_- \\ 0, \text{if } V_+ < V_- \end{cases}$$

A comparator consists of a specialized high-gain differential amplifier. They are commonly used in devices that measure and digitize analog signals, such as analog-to-digital converters (ADCs), as well as relaxation oscillators.

II.REVIEW PROCESS ADOPTED

A literature review is necessary to know about the research area and what problem in that area has been solved and need to be solved in future. This review process approach were divided into five stages in order to make the process simple and adaptable. The stages were:-



Stage 0: Get a "feel"

This stage provides the details to be checked while starting literature survey with a broader domain and classifying them according to requirements.

Stage 1: Get the "big picture"

The groups of research papers are prepared according to common issues & application sub areas. It is necessary to find out the answers to certain questions by reading he Title, Abstract, introduction, conclusion and section and subsection headings.

Stage 2: Get the "details"

Stage 2 deal switch going in depth of each research paper and understand the details of methodology used to justify the problem, justification to significance &novelty of the solution approach, precise question addressed, major contribution, scope & limitations of the work presented.

Stage 3: "Evaluate the details"

This stage evaluates the details in relation to significance of the problem, Novelty of the problem, significance of the solution, novelty in approach, validity of claims etc.

Stage 3+: "Synthesize the detail"

Stage 3+ deals with evaluation of the details presented and generalization to some extent. This stage deals with synthesis of the data, concept & the results presented by the authors.

III. VARIOUS ISSUES IN THE AREA

After reviewing 31 research papers on designing and implementation of Low-Power Low-voltage Double –Tail Comparator we have found following issues:

a) CONVENTIONAL DYNAMIC COMPARATOR

b) CONVENTIONAL DOUBLE-TAIL DYNAMIC COMPARATOR

c) DOUBLE-TAIL DYNAMIC COMPARATOR

IV. ISSUE WISE DISCUSSION

a) ***Issue1*:-** CONVENTIONAL DYNAMIC COMPARATOR

The schematic diagram of the conventional dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in Fig. 4.1 [1], [17]. The operation of the comparator is as follows. During the reset phase when CLK = 0 and M_{tail} is off, reset transistors (M7–M8) pull both output nodes Out_n and Out_p to VDD to define a start condition and to have a valid logical level during reset. In the comparison phase, when CLK = VDD, transistors M7 and M8 are off, and M_{tail} is on.

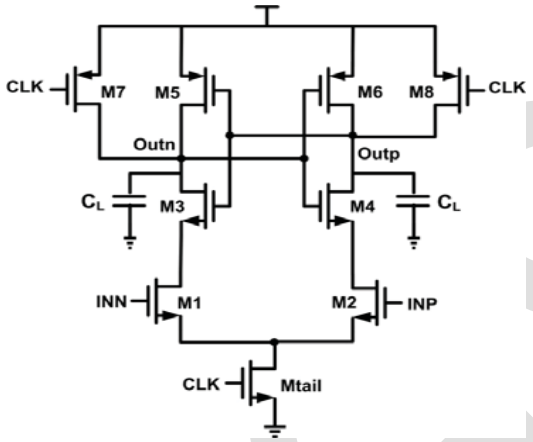


FIG. NO. 4.1 CONVENTIONAL DYNAMIC COMPARATOR

Output voltages (Out_{put}, Out_n), which had been pre-charged to VDD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where VINP > VINN, Outp discharges faster than Out_n, hence when Out_p (discharged by transistor M2 drain current), falls down to VDD–|Vthp| before Outn (discharged by transistor M1 drain current), the corresponding PMOS transistor (M5) will turn on initiating the latch regeneration caused by back-to-back inverters (M3, M5) and M4, M6). Thus, Outn pulls to VDD and Outp discharges to ground. If VINP < VINN, the circuits works vice versa. As shown in Fig. 3.1, the delay of this comparator is comprised of two time delays, t0 and t_{latch}.

The delay t0 represents the capacitive discharge of the load capacitance CL until the first p-channel transistor (M5/M6) turns on. In case, the voltage at node INP is bigger than INN (i.e., VINP > VINN), the drain current of transistor M2 (I2) causes faster discharge of Outp node compared to the Out n node, which is driven by M1 with smaller current.

b) ***Issue 2*:-** CONVENTIONAL DOUBLE-TAIL DYNAMIC COMPARATOR

A conventional double-tail comparator is shown in Fig. 3.2 [10]. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider Mtail2, for fast latching independent of the input common-mode voltage (Vcm), and a small current in the input stage (small Mtail1), for low offset [10].

The operation of this comparator is as follows , During reset phase (CLK = 0, Mtail1, and Mtail2 are off), transistors M3-M4 pre-charge fn and fp nodes to VDD, which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground. During decision-making phase (CLK = VDD, Mtail1 and Mtail2 turn on), M3-M4 turn off and voltages at nodes fn and fp start to drop with the rate defined by IMtail1/Cfn(p) and on top of this, an input-dependent differential voltage Vfn(p) will build up. The intermediate stage formed by MR1 and MR2 passes Vfn(p) to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise [10].

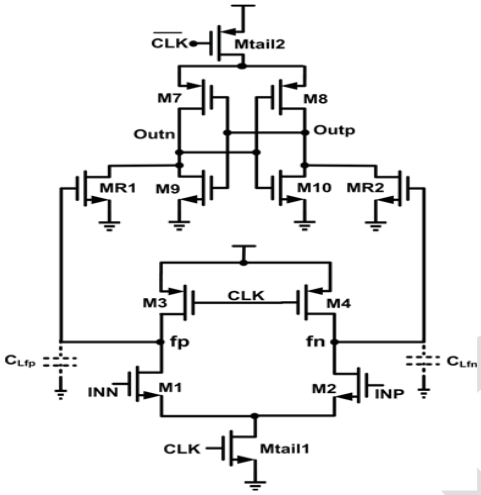


FIG. NO. 4.2 CONVENTIONAL DOUBLE TAIL DYNAMIC COMPARATOR

Similar to the conventional dynamic comparator, the delay of this comparator comprises two main parts, t0 and tlatch. The delay t0 represents the capacitive charging of the load capacitance CLout (at the latch stage output nodes, Outn and Outp) until the first n-channel transistor (M9/M10) turns on, after which the latch regeneration starts; thus t0 is obtained where IB1 is the drain current of the M9 (assuming VINP > VINN) and is approximately equal to the half of the tail current (Itail2). After the first n-channel transistor of the latch turns on (for instance, M9), the corresponding output (e.g., Outn) will be discharged to the ground, leading front p-channel transistor (e.g., M8) to turn on, charging another output (Outp) to the supply voltage (VDD).

a) ***Issue 3:-*** DOUBLE-TAIL DYNAMIC COMPARATOR

Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure. The main idea of the proposed comparator is to increase Vfn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (Mc1 and Mc2) have been added to the first stage in parallel to M3/M4 transistors but in a cross-coupled.

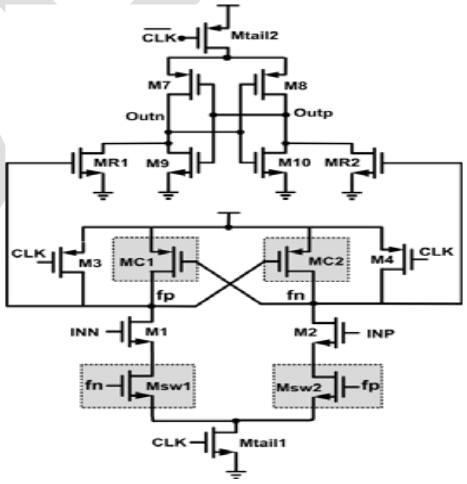


FIG. NO. 4.3 DOUBLE TAIL DYNAMIC COMPARATOR

V. Different Circuit Parameters used for Experimentation:-

TABLE I SUMMARY OF THE COMPARATOR PERFORMANCE

Item	Value
Technology	180-nm CMOS
Supply voltage	1.2 V
Average power dissipation per conversion @ freq. = 500 MHz	329 μW
Worst case delay (Vcm = 0.6 V, _Vin = 1 mV)	550 ps
Delay/log(_Vin)	69 ps/dec
Offset standard deviation (1-sigma) (σos)	7.8 mV
Energy efficiency	0.66 pJ

The performance of the conventional dynamic comparator, Double-tail dynamic comparator & proposed dynamic comparator & their structure can be compared by following table:-

TABLE II PERFORMANCE COMPARISON

Comparator structure	Double-tail Dynamic comparator	Proposed Dynamic Comparator	Conventional Dynamic comparator
Technology CMOS	180nm	180nm	180 nm
Supply voltage (V)	0.8 V	0.8 V	0.8 V
Maximum sampling frequency	1.8 GHz	2.4 GHz	900 MHz
Delay/log(_Vin) (ps/dec.)	358	294	940
Peak transient noise voltage at regeneration time(nV)	221 n	219 n	215n
Energy per conversion (J)	0.27p	0.24p	0.3p

VI. Result-

CONVENTIONAL DYNAMIC COMPARATOR FOR 130 nm

Conventional dynamic comparator is a design in which two voltages are comparing. Input voltage 1.2 V and we are comparing the results Vn and Vp voltages. In the starting we are giving the Vp > Vn . Vp = 1.0 v and Vn = 0.5 V.

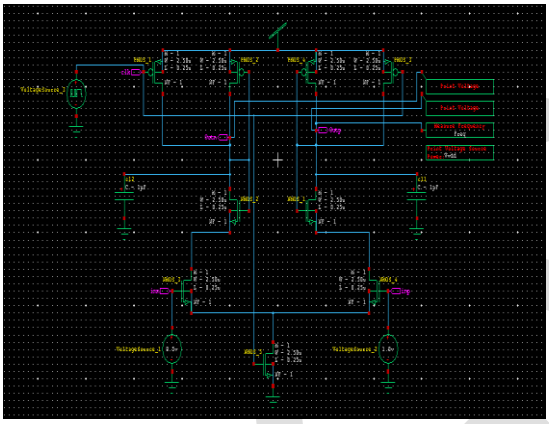


Fig. no. 6.1 Conventional dynamic comparator

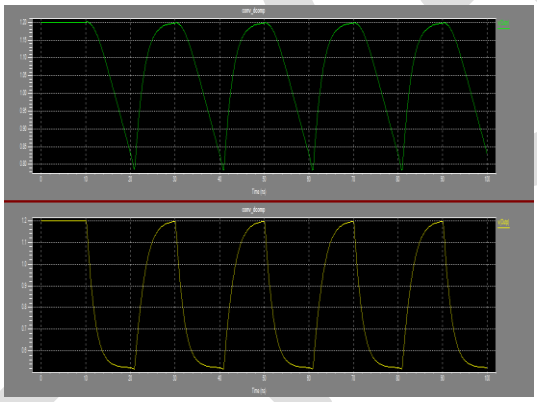


Fig. no. 6.2Waveform for Conventional dynamic comparator

CONVENTIONAL DOUBLE-TAIL DYNAMIC COMPARATOR AT 130 nm

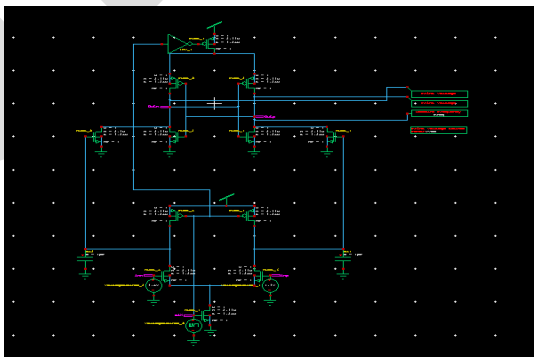


Fig. no. 6.3Conventional Double-Tail Dynamic Comparator

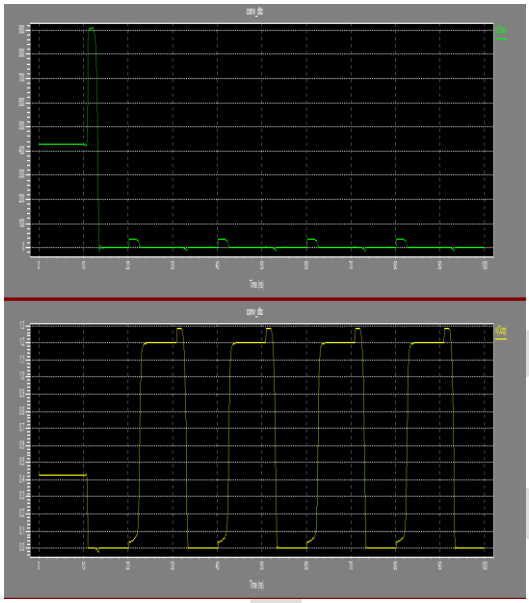


Fig. no. 6.4Waveform for Conventional Double-Tail dynamic comparator

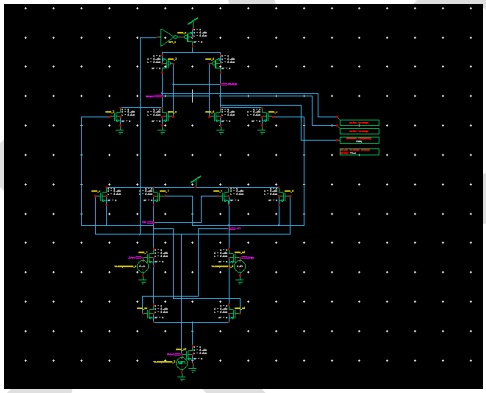


Fig. no. 6.5 Double-Tail Dynamic Comparator

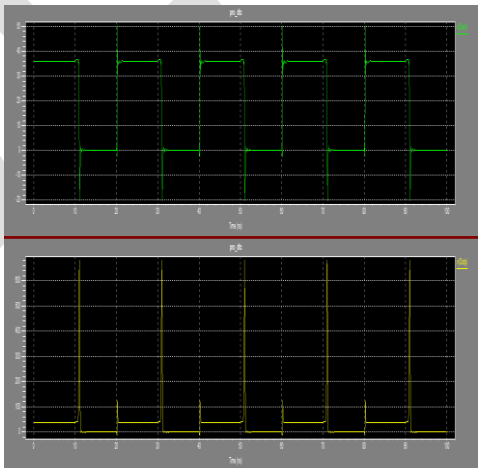


Fig. no. 6.6 Waveform of Double-Tail Dynamic Comparator

VII. Conclusion

In the total experimental work we presented a comprehensive delay analysis for clocked dynamic comparators and expressions were derived. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in 0.18-μm CMOS technology confirmed that the delay and energy per conversion of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator.

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