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Efficient Implementation of Multi-View Video Compression for High Performance Application

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Abstract: Multi-view applications provide viewers a whole new viewing experience and multi-view video coding (MVC) that plays a key role in distributing multi-view video contents through networks with limited bandwidth. The main objective of Multi-View video compression is to increase the compression ratio with minimum loss. The Hierarchical B picture (HBP) prediction structure is very helpful in multi-view video coding due to a reduction in the computational complexity in MVC and improves the coding efficiency. In this paper, Low Cost Multi-view Video Coding Discrete Wavelet Transform (LC-MVC-DWT) is introduced to improve the Peak-Signal-to-Noise-Ratio (PSNR) value, Application Specified Integrated Chip (ASIC) performances and Field Programmable Gate array (FPGA) performances. FPGA results showed that LUT, slices, flip flops, frequency improved and also ASIC results showed that area, power, delay, Area Power Product (APP) and Area Delay Product (ADP) improved in the LC-MVC-DWT technique compared to the existing methods.

Keywords: Discrete cosine transform, Discrete wavelet transform, Multi-view video coding, Discrete cosine transform, Peak-signal-to-noise-ratio, Mean square error.

1. Introduction

Multi-view Video Coding (MVC) 3D is a stereoscopic video coding standard for video compression that takes into account the proficient encoding of video sequences caught all the while from different camera points in a solitary video stream and it is an eminence active research area. In general video coding, temporal random access is one of the requirement, because it can be inserted intra-coded pictures. In MVC, random access is an essential parameter to decode and display the images [1, 2]. Hierarchical prediction structure is very helpful in MVC and it can be categorized the predictions like intra, inter-frame, and inter-view predictions. The main MVC responsibility is the efficient compression of multiple views. With the help of temporal and spatial prediction, compression of a video will be improved [3].

For improving the MVC standard, a novel scheme has been introduced that is 3-dimensional Motion Estimation (ME) and compensation method. This new scheme, which is used to decrease the computational time and to remove the random-access frame delay. In that one newer technique is also launched, namely 3D-ME-McFIS that is created using Dynamic Background Modelling (DBM). With the help of DBM, the Rate Distortion (RD) has been implemented with minimum computation time [4]. By using best-supporting mode, RD performance and encoding time is improved in H.264/AVC. This proposed algorithm takes the support from two well-organized predictive methods namely predictive skipping scheme with a sum of absolute difference (SAD) of each MB and filtering some sub-macro block (MB) level modes with an adaptive threshold [5].

Many techniques are needed in H.264 for reach a high coding performance of MVC such as Fast Mode Decision (FMD) method, ME, Disparity Estimation (DE), different prediction modes, all zero block decision techniques (AZB), and Hierarchical

B Picture (HBP) prediction structure [6]. Another extension of H.264 advanced video coding (AVC) is Scalable Video Coding (SVC). For the most excellent coding mode purpose, it chooses the exhaustive expensive decision mode. FMD algorithm in AZB technique is used to overcome these problems in SVC [7]. To get better coding efficiency, MVC encoder is required, which is based on the motion compensated prediction (MCP) and disparity compensation prediction (DCP) [8]. FMD algorithm is very helpful in MVC, which reduces the computational complexity and also saves coding time and it contains intra prediction and inter prediction algorithms. The redundant mode is removed, when mode distribution is correlated with adjacent views. The main role of this algorithm is dropping the MVC problems entirely [9]. To improve the image compression technique, two algorithms are used, namely Discrete Cosine Transform (DCT) and Discrete Wavelet Transform (DWT). During compression time DCT losses more information but it requires less processing power. On the other hand, DWT provides better compression ratio without losing more information to the image. [10]

In LC-MVC-DWT method, the visual quality of the algorithm is improved by using the Discrete Wavelet Transform (DWT). The quality of the compression is mainly depending upon the compression standard and motion estimation which is used. By changing DWT from DCT, we can increase the visual quality which leads to improve the Peak-Signal-to-Noise-Ratio (PSNR), Mean Square Error (MSE) and Structural Similarity (SSIM) metrics. In ASIC the area, power and delay minimized by implementing in cadence encounter tool with 180nm and 45nm library technology. In FPGA implementation, the number of LUTs, slice and flip-flop will be decreased in LC-MVC-DWT for different kinds of Virtex devices such as Virtex 6 and Virtex 7.

This paper is composed as follows. In section 2, described some previous related work. In section 3, shows LC-MVC-DWT design architecture. In section 4, mentioned experimental setup and results and discussion. The conclusion is made in section 5.

2. Literature review

P.A. Akiki and H.W. Maalouf [11] have presented a new technique which is based on multiple matrices of pictures (MOP). This technique was used to integrate multiple matrices of pictures (MOP) from different perspectives that produce one output. In this paper, MOP is required more time to perform the decoding process and also decoding speed is very slow.

C.S. Park, H.S. Kim and H.W. Cha [12] have presented histogram matching (HM) technique to develop MVC performance via color correction algorithm. This method is mainly based on histogram matching (HM). The proposed algorithm is an efficient histogram threshold for achieving a good coding efficiency of multi-view video sequences. The proposed algorithm achieves better coding efficiency, less computation time but PSNR value should be improved.

T.J. Jung, H.R. Lee and K.D. Seo [13] have presented a new design method named as Decoded Picture Buffer (DPB). This paper includes several operations such as marking process, reference picture reordering, and list construction. All these operations are used for developing the efficient coding of MVC. In this paper, Scalable video coding (SVC) algorithm also proposed to get decoded picture efficiency. This proposed method can deliver the advanced compression efficiency and also progress the video quality. The PSNR value of this paper is too low and also very difficult to decode the picture without any loss.

H. Narayanan and M.K. Sheeja [14] the author concentrated on removing the temporal and spatial redundancy. So, MVC uses the prediction structure. With the help of multiple camera systems, inter frame, intra-frame, and interview prediction can be combined to obtain the simultaneous video compression. In this paper to check the efficiency of spatial and temporal prediction algorithm to use MATLAB simulation of an IPP hierarchical prediction structure is achieved. But the visual quality improvement is still needed.

Karsten Muller [15] have defined an extension of the high-efficiency video coding (HEVC) standard. HEVC suggested a new 3D video coding framework for depth enhanced multi-view formats. Accordingly, MVC was standardized as an extension of H.264/MPEG-4 Advanced Video Coding. With a help of coded views, video quality can be approximately increased. But this proposed method achieves only half part of the bit rate are saved. Still, more improvement is required.

For existing work, they have used DCT and FFT for compression. That techniques are occupied more area, more power, high critical path, and more hardware utilization in FPGA implementation. For performance also less in conventional methods like PSNR, and quality of the picture. To overcome these problems, LC-MVC-DWT method is introduced to improve the PSNR performance, ASIC

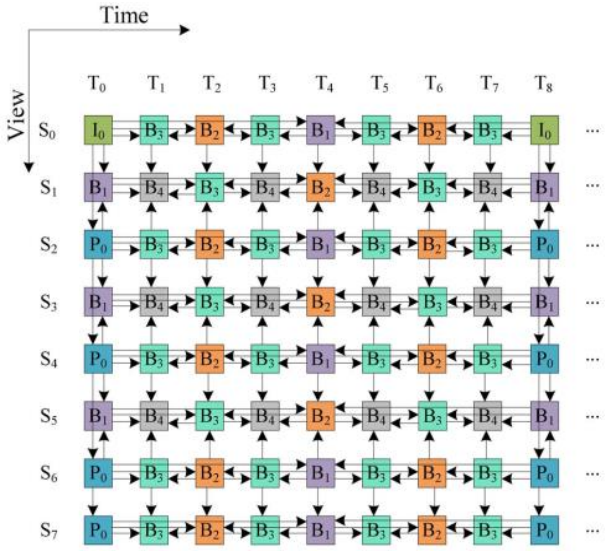


Figure.1 MVC-HBP prediction structure in JMVC

implementation results and FPGA implementation results.

3. LC-MVC-DWT methodology

The LC-MVC-DWT system of Hierarchical B picture (HBP) prediction structure is very helpful in multi-view video coding due to reduce the computational complexity in MVC and improve the coding efficiency.

Multi-view video coding - HBP prediction structure in JMVC is shown in fig 1. This structure consists of a sequence of views and group of pictures. It is denoted by Si i=0,1,…,7 and Ti i=0,1,....,7. Mainly two groups in HBP prediction structure such as odd view and even view. The Even view contains (S0, S2, S4, S6) and odd view contains (S1, S3, S5, S7). For removing the temporal redundancies, motion estimation (ME) is used in even views side. But in the odd side motion estimation (ME) and disparity estimation (DE), both are used. Below the fig shows the seven different views of candidates for the variable block size mode selection but all the seven views can be verified orderly. So candidate views are grouped into two categories likes S is the inter mode set and T is the non-inter mode set.

The Performance can be determined through Computation time, Quality of the decompressed frame and Compression ratio. The quality of the decompressed frame can be measured by using the performance parameters like MSE, PSNR, and SSIM. Similarly, computation time for decompression is one of the important parameters which are used to measure the performance of the compression. Several methods have been proposed previously like 3D-ME-McFIS, DCP, MCP etc. for multi-view video compression to increase the performance in terms of computation time as well as visual quality. In order to improve the visual quality and performance of the compression, the proposed DWT scheme is utilized instead of DCT method.

In LC-MVC-DWT method, we are increasing the visual quality performance by keeping the computation time as same. Similarly, it depends upon the prediction capability of the algorithm. The LC-MVC-DWT method can provide better visual quality because we are going to use DWT instead of DCT. Block diagram of the LC-MVC-DWT method compression can be shown in fig. 2. Main blocks are motion estimation, the motion compensation block, 2D-DWT, rounding, entropy encoding, and IDWT.

A multiplexer block is used to select the frames which are fed to the compression block. For increasing the visual quality and compression performance, our proposed method is introduced. Finally, to get binary bit stream will be generated by using entropy coding and bit streams are compressed bits.

3.1 LC-MVC-DWT block diagram

Fig. 2 shows the working of our LC-MVC-DWT method and the main goal of our LC-MVC-DWT method is to compress the images.

Initially, one input image frame can view in various viewpoints its indicating as v0, v1, v2, ...,vn is showed in the Fig.2. Views multiplexer is evaluated the all different views and the multiplexer is performed as many inputs with one output switch. Next input frame goes to the ME process as well as subtract operation process. ME is the most important process in video compressing technique because it will decrease the temporal redundancy in video data. To develop the image sequence, there is a need to estimate the motion of the image sequence. Next Motion compensation (MC) takes the image from ME, it also the main technique in image compression process. Subsequently, input values and MC values are subtracted, later one single frame is moved to the 2D-DWT. Each frame is coming to the 2D-DWT, for example, the original image sizes are 256x256 is first divided into 16x16. Each 16x16 frames are again decomposed with a help of 2D-DWT. The only low-frequency coefficients (LL) is passed to the next stage using exact low-frequency component where the high-frequency coefficients are discarded. The lowest frequency coefficients are passed to the IDWT, to reconstruct the frequency modules. So once all the process is done means finally we get a compressed output. In our proposed method of evaluating some following processes.

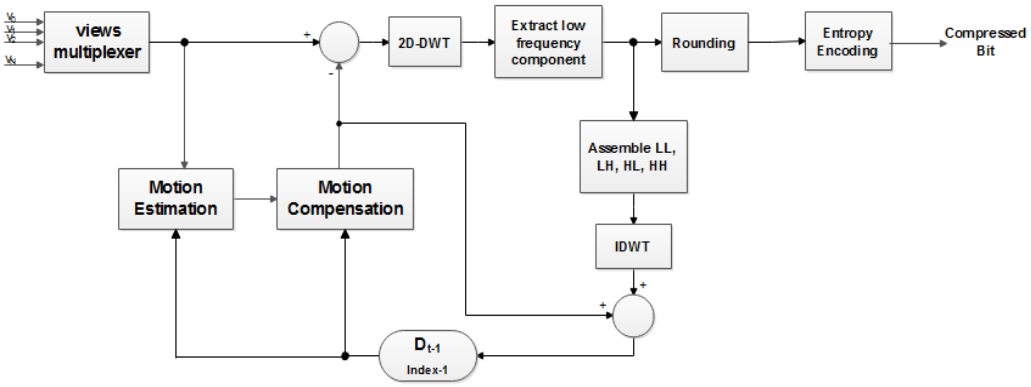


Figure.2 Block Diagram of LC-MVC-DWT Method

3.1.1. Motion estimation

This is one of essential video compression schemes because it will produce better PSNR and reduce the complexity. The main aim of the ME is to extract the matching objects from the image frame, after that, the objects are forward to the MC. This process examines the past or future frames to recognize blocks that have similar, and motion vectors are stored in place of blocks. The process of video compression using ME is also known as interframe coding. With a help of this method, PSNR value is improved, reduce the image complexity and also get better compression result.

3.1.2. Motion compensation

Motion compensation scheme is used as part of the predictive process. If an image sequence shows moving objects, then their motion within the scene can be measured, and the information used to predict the content of frames later in the sequence. MC technique expresses the transformation of a reference frame to the current frame. The reference frame may be previous or taken the frame later. When the current frames can be accurately synthesized from previously transmitted or stored frames, the compression efficiency can be improved.

3.1.3. 2D-DWT

Two-dimensional DWT is a multilevel decomposition technique and it is an essential for multimedia applications. 2D-DWT is converting the images from the spatial domain to frequency domain and it is a multilevel decomposition technique that decomposes into four subbands such as HH, HL, LH, LL. In 2D-DWT, initially select the decomposition level and after that select, the recovered image should match the original input image. This technique is processed by performing low-pass and high-pass sorting of the picture pixels. 2D-DWT calculations more often than not have normal and steady examples. Some 2D-DWT implementations utilize a few coefficients that are unmodified through the full execution of the function. The number of these coefficients is usually small and they can be stored in media registers rather than the memory hierarchy.

3.1.4. Inverse discrete wavelet transform (IDWT)

Normally, IDWT is the converse of DWT and it is an intense instrument for picture coding and decoding frameworks. IDWT requests huge calculations, subsequently it requires a parallel and pipelined design to perform continuous or online video and picture coding and decoding. This strategy is high-effectiveness and low power design and IDWT will change over the frequency to spatial. DWT and IDWT designs have a standard structure, nearby correspondence, and versatile channel length.

3.1.5. Entropy encoding

Entropy encoding is a lossless information compression plot that is autonomous of the particular qualities of the medium. Entropy encoders compress the information by supplanting each settled length input image with the comparing variable-length of the output code word. In Entropy encoding, the combination of change and quantization result altogether decrease the information measure. An entropy encoder additionally packs the quantized values in lossless to give better pressure proportion. It utilizes a model to precisely decide the probabilities for each quantized value and delivers a proper code in light of these probabilities the resultant output code stream will be littler than the input stream. Thus entropy encoding module is a very important module for any type of multimedia data for efficient code bit assignment.

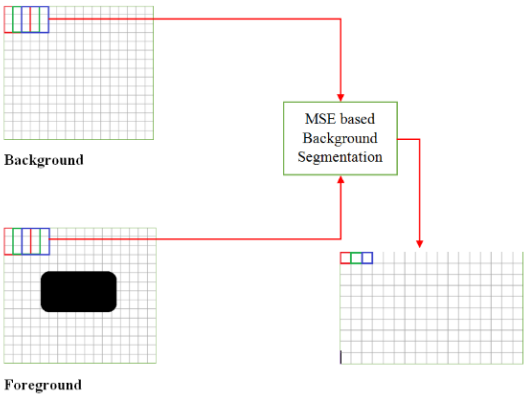


Figure.3 MSE based background segmentation

3.2 MSE based background segmentation

MSE estimator will measure the average of the square of the error, to improve the image visual quality we find the MSE values.

The MSE operation of background segmentation is shown in fig.3. Normally, the input frame contains background and foreground images. Each frame contains pixels; each pixel is divided into NxM array matrix in both images. MSE based background segmentation contains two values like one value is taken from Background process and the second value is taken from Foreground process then, MSE operation is performed. After that, MSE values indicate the similarities of the background and foreground images. After the MSE operation, we get the accurate resultant value which is the exact output of the compressed image. Image and video quality assessment occurs when you have to measure the degree of fidelity of an encoded copy of a picture or a clip of their original version.

According to the MSE,

$$MSE = \frac{1}{nxm}\sum_{i=0}^{n=1}\sum_{j=0}^{m=1}[x(i,j) - y(i,j)]^2 \quad (1)$$

Where NxM is the array matrix of the image. x and y are the foregrounds and backgrounds images and row and columns are indicating as i and j. Most of the time MSE value is less. Obviously, the greatest similarity is achieved if the MSE value is zero, through x and y values.

The RTL schematic of overall encoder and decoder circuits shown in Figs. 4 and 5. This schematic is obtained from a Synplify Pro by using Verilog code. We have a separate code for each block such as address generation, Huffman encoding process, Huffman decoding, motion estimation, DWT, overall encoder, and overall decoders.

4. Results and discussion

The LC-MVC-DWT method for Video compression is implemented in MATLAB version R2015b and Cadence 180nm for area, power and delay analysis. The complete work is done by using the I7 system with 8 GB RAM. A better quality video is achieved by using DWT in the proposed algorithms.

4.1 PSNR

PSNR is most commonly used to measure the quality of reconstruction of lossy compression codes (e.g., for image compression). PSNR is easily defined by mean squared error. Mathematically PSNR is illustrated below in Eq.(2),

$$PSNR(dB) = 10\log_{10}(\frac{255^2}{MSE}) \quad (2)$$

4.1.1. Bitrate

Bit rate defines that the number of bits are conveyed or processed per unit time. This bit rate is calculated by using this formula.

Frequency x Bit width x channels = Bit rate

4.1.2. Computation time

Computational time is the length of time required to perform a computational process. Representation a computation as a sequence of rule applicat ions, the computation time (tc) is proportional to the number of rule applications (ar).

tc ∞ ar

The Performance comparison of the PSNR, Bit rate, Computation time, and Bit rate is given in tab.1. From this table its clears that all the parameters have been improved in LC-MVC-DWT method than existing method. In table 2, three different camera frame taken and calculate PSNR and computation time.

4.2 ASIC synthesis

ASIC synthesis is implemented in Cadence tool for different technology like 180nm and 45nm. From this tool, the parameter performance will be calculated such as area, power, and delay.

4.2.1. Area

With contracting framework measure ASIC ought to have the capacity to accommodate most extreme usefulness in less range. The designer will determine region limitation and cadence instrument

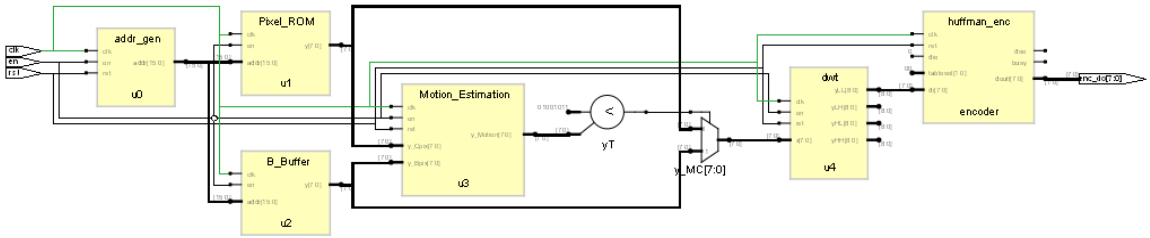


Figure.4 RTL schematic diagram for Overall encoder

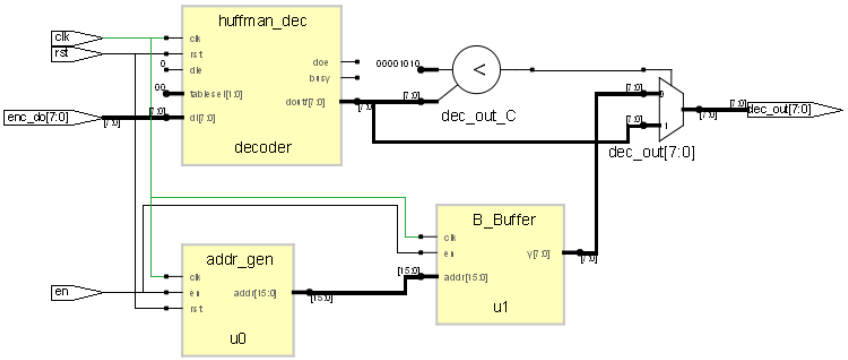


Figure.5 RTL schematic for Overall Decoder

Table 1 Performance comparison

Methods	PSNR (dB)	Bitrate	Computational time T (s)	ΔPSNR (dB)	Δ Bitrate (%)	ΔT (%)
Existing	72.9131	128000	23.3460			
Proposed method	74.6404	184649.7383	8.8543	1.7273	0.4426	-62.070

ΔT – Time-saving ratio, T- computational time

Table 2. Area, power and delay of existing encoder and decoder circuits

	Area	Power (nw)	Delay (ps)
Encoder	762166	73268623.50	93
Decoder	323768	37866413.68	525

Table 3. Performance comparison of the three CAMs

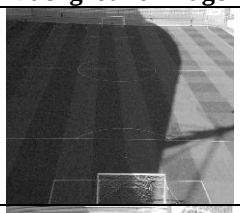
Cam No	Background image	Current frame	PSNR(dB)	Computational time (seconds)
Cam1			74.2194	4.7628
Cam2			75.5677	1.1988
Cam3			74.1342	1.1945

Table 4. The performance of area, power and delay the LC-MVC-DWT method for 180nm and 45nm technology.

Technology	Method	Area (um2)	Power (nW)	Delay (ps)	APP (um2 * nW)	ADP (um2 * ps)
180nm	Existing [6]	1249575	138764512	98.2	173396665082400	122708265
	LC-MVC-DWT	1046188	107733257	96.8	112709240674316	101270998
45nm	Existing [6]	145615	15254311	275.3	2221256496265	40087809
	LC-MVC-DWT	127180	13507326	273.8	1717861720680	34821884

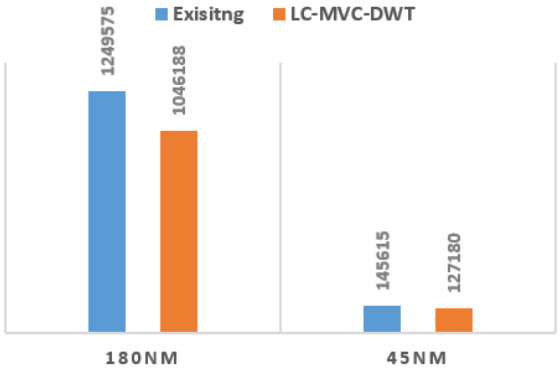


Figure.6 Comparison of area performance for 180nm and 45nm

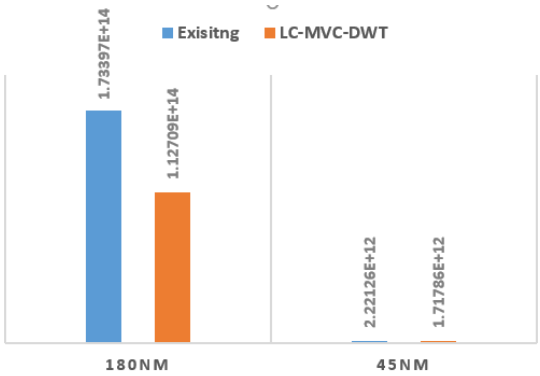


Figure.9 Comparison of APP performance for 180nm and 45nm

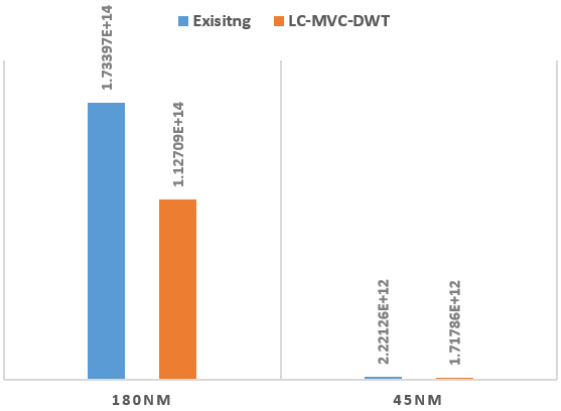


Figure.7 Comparison of power performance for 180nm and 45nm

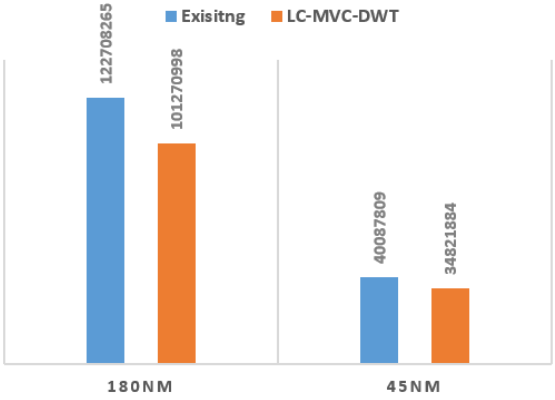


Figure.10 Comparison of ADP performance for 180nm and 45nm

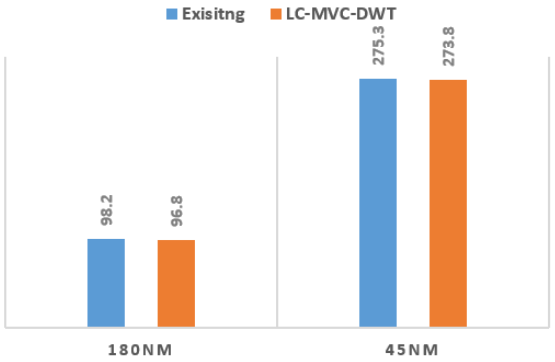


Figure.8 Comparison of delay performance for 180nm and 45nm

is utilized to optimize the area performance. The zone can be upgraded by having lesser number of cells and by supplanting various cells with a single cell that incorporates the two functionalities.

4.2.2. Power

Improvement of hand-held gadgets has prompted a diminishment of battery estimate and consequently give low power expending systems. Low power utilization has turned into a tremendous requirement for a ton of designers.

4.2.3. Delay

The designer specifies the maximum delay between primary input and a primary output. This is taken as maximum delay across any critical path.

Table 5. Reduced percentage of area, power, delay, APP, and ADP for LC-MVC-DWT method

Technology	Reduced % of Area	Reduced % of power	Reduced % of Delay	Reduced % of APP	Reduced % of ADP
180nm	16.27	22.36	2.24	34.99	17.47
45nm	12.66	11.45	0.5	22.66	13.13

Table 6. Implemented on different Xilinx FPGA devices for Existing and LC-MVC-DWT

Target FPGA	Circuit	LUT	Flip-flop	Slice	Number of DSP	Frequency (MHz)
Virtex6 xc6vcx240t	Existing [6]	548/150720	81/674	212/301440	34/768	108.2
	LC-MVC-DWT	543/150720	76/674	207/301440	30/768	110.81
Virtex6 xc6vlx75tt	Existing [6]	545/150720	79/674	209/301440	32/768	75.32
	LC-MVC-DWT	543/150720	76/674	207/301440	30/768	80.921
Virtex7 xc7vx330t	Existing [6]	549/204000	77/674	216/408000	36/1120	110.35
	LC-MVC-DWT	542/204000	75/674	207/408000	30/1120	127.905

The comparison of the area, power, delay, APP, and ADP for different technologies such as 180nm and 45nm is given in table 3. In the existing methods, DCT has used, which occupies more area. In LC-MVC-DWT method, DWT is used, which required less space. Due to this DWT, the area, power, delay, APP, and ADP is minimized in LC-MVC-DWT architecture than conventional methods.

The comparison graph of area, power, delay, area power product, and area-delay product is shown in Figs. 6 - 10. That results are drawn by using 180nm and 45nm technology for different methodologies. According to that graph, the blue color is existing technology and the orange line is represented as LC-MVC-DWT. From this graph, it is cleared that LC-MVC-DWT method consumes less area, less power, less delay, less area power product and less area-delay product than the conventional methods.

Table 2 presents the reduced percentage of area, power, delay, APP, and ADP for LC-MVC-DWT. This architecture result has been taken in both 180nm and 45nm technology. In 180nm technology, 16.27% of area, 22.36% of power, 2.24 % of delay, 34.99 % of APP, and 17.47% of ADP is reduced in LC-MVC-DWT as well as in 45nm technology, 12.66% of area, 11.45% of power, 0.5 % of delay, 22.66% of APP, and 13.13% of ADP is reduced in LC-MVC-DWT method than the conventional methods.

4.3 FPGA synthesis

This FPGA synthesis is implemented in Xilinx tool for different devices such as Virtex-6, and Virtex-6. From this tool, the performance parameter like LUT, flip-flop, Slices, and Frequency has been calculated.

4.3.1. LUT

A LUT, which stands for Look Up Table, in general terms is essentially a table that figures out what the output is for any given input(s). With regards to combinational logic, it is reality table. This reality table effectively characterizes how combinatorial logic acts.

4.3.2. Flip-flop

Flip-flops are paired move registers used to synchronize logic and spare sensible states between clock cycles inside a FPGA circuit. On each clock edge, a flip-flop latches the 1 or 0 (TRUE or FALSE) value on its information and holds that esteem consistent until the point when the following clock edge.

4.3.3. Slices

Logic resources are assets on the FPGA that can perform logic capacities. Logic assets are assembled in slices to make configurable logic squares. A slice contains a set number of LUTs, flip-flop, and multiplexers. A LUT is a gathering of logic gates hard-wired on the FPGA.

4.3.4. Frequency

Frequency is defined as the rate at which something occurs over a particular period of time or in a given sample.

Table 6 presents the comparison of FPGA method to analyzing performance parameters such as LUTs, the number of flip-flops, slices, number of DSP, and operating frequency for different FPGA devices such as vertex 6, and vertex 7. From this table, it clears that the LUT, flip-flop, slices are

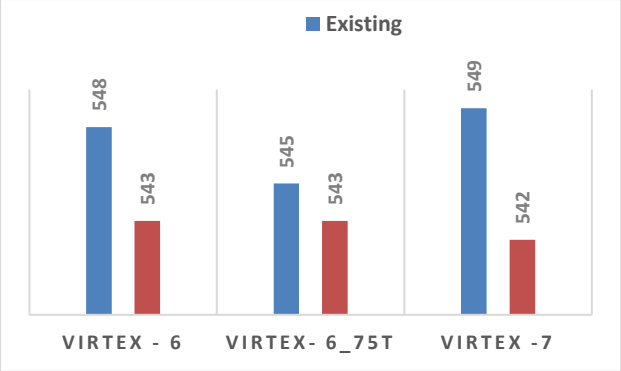


Figure.11 Comparison of the LUT performance for different Virtex devices

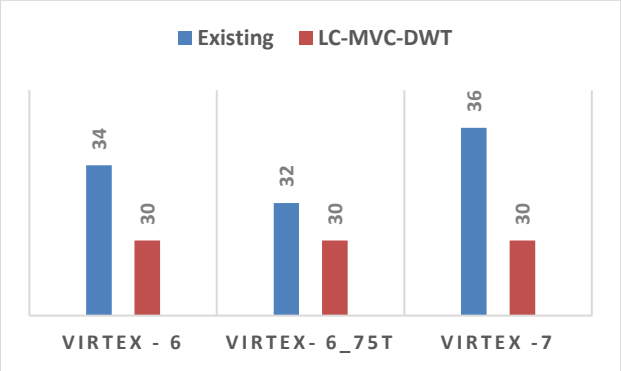


Figure.12 Comparison of the DSP performance for different Virtex devices

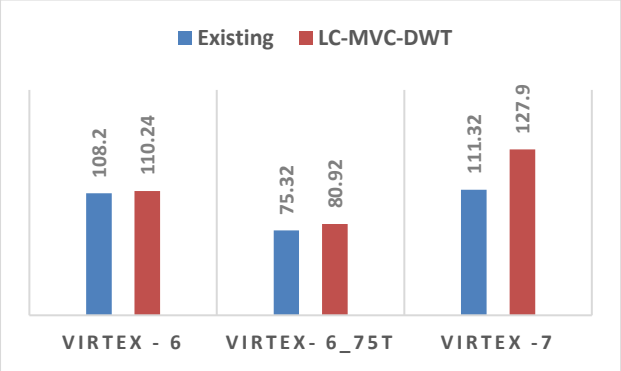


Figure.13 Comparison of the frequency performance for different Virtex devices

reduced and operating frequency is increased in LC-MVC-DWT method than the existing methods. Due to the reduction of those parameters, the area has been minimized in LC-MVC-DWT.

FPGA performance of different device is shown in Fig.11, Fig.12, and Fig.13. In that graph, LUT, number of DSP, and Frequency has been analysed for different FPGA devices such as, vertex 7 and vertex 6. In Virtex 6, two family has been analysed like Virtex6 xc6vcx240t and Virtex6 xc6vlx75tt. From this graph, it's clears that all the FPGA performance is improved in LC-MVC-DWT design than conventional design.

Total Area	Switching (nW)	Delay (ps)
127180.30	13507326.13	33.30
36569.73	3996102.49	
1446.38	3358555.07	0.00
191.94	254744.18	37.10
103.25	39420.19	0.00
197.58	349963.33	26.90
34891.99	286385.19	0.00
90610.57	9098260.09	273.80
1842.94	3824519.90	
346.34	376251.10	
99.02	0.00	

Figure.14 Implementation of the decoder in cadence 180nm tool

The RTL schematic of LC-MVC-DWT is shown in fig.15, which is taken from cadence tool. For ASIC implementation, same code is used for the FPGA implementation. Cadence RTL compiler is used to convert RTL Verilog into Gate level Verilog. Verilog codes are read by using a .tcl file and corresponding libraries also set into the tcl file. After synthesizing, Area, Power and Delay, result is displayed in cadence tool. The overall cadence output of LC-MVC-DWT method is shown in Fig.14. From cadence tool, we get this results, which is shown as screenshot for verification purpose. From this screenshot, it's clears that total area, total delay, total power, APP and ADP is reduced in LC-MVC-DWT method compared to the conventional methods.

5. Conclusion

In this paper, we have implemented a low-cost multi-view video compression based DWT. For compression, DCT and FFT have been implemented in conventional methods which required more area, and power. But DWT method, ASIC and FPGA performance has been improved. By using DWT, we have achieved less computational time, improved Bitrate. Performance metrics are calculated by using MATLAB with different frames of football video with three different views and achieved better performance. The LC-MVC-DWT architecture is implemented in 180nm and 45nm technology using cadence tool and achieved better results in area, power and delay when compared to the conventional implementation. In 180nm technology, 16.27% of area, 22.36% of power, 2.24 % of delay, 34.99 % of APP, and 17.47% of ADP is reduced in LC-MVC-DWT as well as in 45nm technology, 12.66% of area, 11.45% of power, 0.5 % of delay, 22.66% of

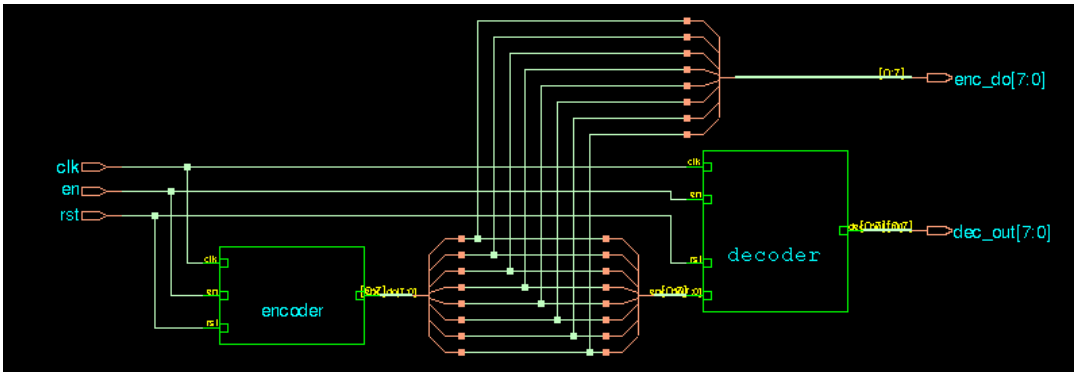


Figure.15 RTL schematic of LC-MVC-DWT method

APP, and 13.13% of ADP is reduced in LC-MVC-DWT method than the conventional methods. In future work, Curvelet transform will be used to improve the values of PSNR, bit rate, ASIC and FPGA performances.

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