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A MODIFIED TWO SWITCHED-INDUCTOR QUASI Z-SOURCE INVERTER

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Abstract:

In this paper, the technique of bootstrap capacitor is applied to the (cSL-qZSI) topology to improve its features such as increasing its total gain and minimizing the total stress across the used component Using switched inductor principle has improved the boosting gain of the applied topology at the same shoot through duty cycle *(D)* compared with the convention one. This also leads to operate at higher modulation index *(M)* and so low stress over the components is resulted. Switched inductor cell is applied to classic qZSI topology instead of the two main inductors to give anew topology that has been called a continuous input current switched inductor quasi Z-Source Inverter (cSL-qZSI)

Keywords-- **Z source inverter, bootstrap capacitor, Voltage gain**

I. INTRODUCTION

In 2002, a single stage inverter called Z-Source Inverter (ZSI), shown in Fig. 1, has been proposed to overcome the limitations of traditional voltage source inverter (VSI) and the traditional current source inverter (CSI) [1] - [4]. ZSI utilizes shoot-through zero state where two switches in the same leg or all switches are gated on simultaneously to boost the output voltage. In ZSI, the six permissible active switching states of VSI remains unchanged; and the zero states can be partially or completely replaced by the shoot-through states depending on the desired boosting voltage. However, these topologies of ZSource Inverter have some limitations, such as small boost factor, high voltage stress across the switches and capacitors and huge inrush current. Several improvements of the basic ZSI topology have been recently developed to overcome these limitations and to improve its features [5]-[9].Also, the concept of the switched inductor (SL) technique [10] has been integrated into the classical Zsource impedance network; consequently a new SL Z-source impedance network topology has been obtained [11]. Using switched inductor principle has improved the boosting gain of the applied topology at the same shoot through duty cycle *(D)* compared with the convention one. This also leads to operate at higher modulation index *(M)* and so low stress over the components is resulted. Switched inductor cell is applied to classic qZSI topology instead of the two main inductors to give anew topology that has been called a continuous input current switched inductor quasi Z-Source Inverter (cSL-qZSI) [12], as shown in Fig. 2. Recently, a bootstrap capacitor is used to replace the middle diode in the switched cell; and it is applied to one switched inductor (qZSI) [13].

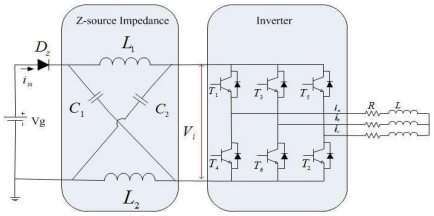


Fig. 1. Classical Z-Source inverter (ZSI)

In this paper, the technique of bootstrap capacitor is applied to the (cSL-qZSI) topology to improve its features such as increasing its total gain and minimizing the total stress across the used component. The proposed topology is presented in section II. Then, the theoretical analysis is explained in details in section III. A comparison with the classic one (cSL-qZSI) is explained in section IV; afterward the simulation results are given in section V and the experimental set-up including their results are illustrated in section VI. Lastly the conclusion is given in section VII. duty cycle *(D)* and modulation index *(M)*. From cost point of view, the capacitor is less expensive than the diode; and from

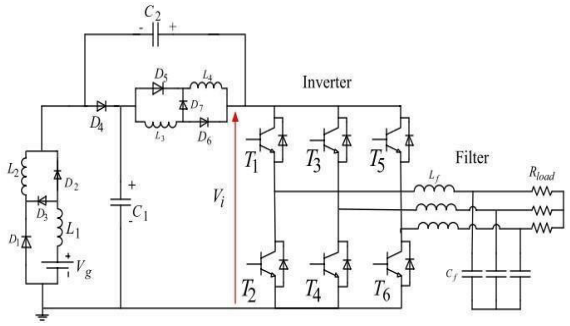


Fig. 2.Classical cSL-qZSI topology.

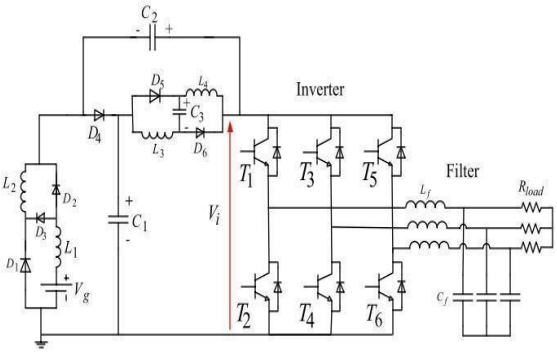


Fig.3.The proposed topology (MTSL-QZSI).

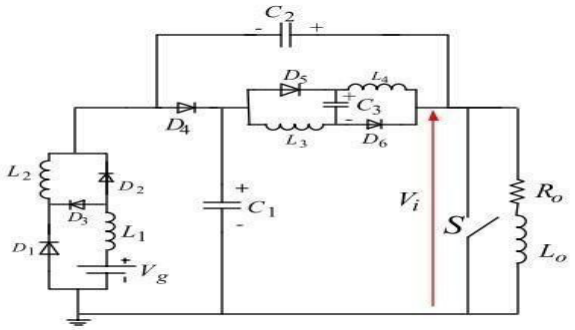


Fig. 4. Equivalent circuit of the proposed topology

II. THE PROPOSED TOPOLOGY

The proposed topology is shown in Fig. 3. The construction of the proposed topology is similar to the cSLqZSI topology; the main difference in the construction between them is the replacement of the diode in the second switched cell *(D7)* with a bootstrap capacitor *(C3)* without increasing the number of component in the circuit.

It contains four inductors (*L1, L2, L3, L4*), three capacitors (*C1, C2,C3*) and six diodes (*D1, D2, D3, D4, D5, D6*). The proposed topology (MTSL-QZSI) has the merits of continuous input current drawn from the DC source due to the direct connection between the inductor (*L1*) and the DC voltage source (V_g); and it has a common mode connection between the DC source and the inverter bridge.

III. THEORETICAL ANALYSIS OF THE PROPOSED TOPOLOGY

Due to the balancing of output AC load, the inverter side can be presented as equivalent R-L load; and the equivalent circuit of the proposed topology (MTSL-qZSI) is shown in Fig. 4. Furthermore, the operating states are simplified into shoot-through state when the switch (*S*) is on and non shoot through state when the switch is off.

Besides, all the analysis will be done under the following assumptions:

- The current of the four inductors operates in Continuous Conduction Mode (CCM).
- All components are ideal.

The voltages across the L_1, L_2, L_3, L_4, C_1, C_2 and C_3 are V_{L1}, V_{L2}, V_{L3}, V_{L4}, V_{C1}, V_{C2} and V_{C3}, respectively. The polarity of these voltages remain the same in the shoot through state and non-shoot through state to simplify the analysis of the circuit. The period of shoot through state is (DT) and the period of non-shoot through state is $(1\text{-}D)T$ where $T$is the switching cycle and D represents the duty ratio of the shoot through for each cycle.

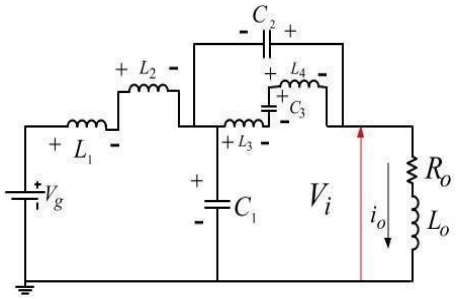
A.Non Shoot-Through State

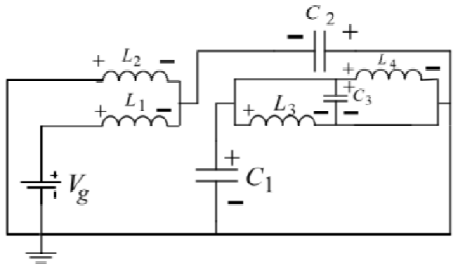
As shown in Fig. 5, during this state, the diodes D_1, D_2, $D_5$and D_6 are turned off, whereas the diodes D_3 and $D_4$are in conducting mode. The inductors $L_1$and L_2 are connected in series; whereas L_2, L_3, and $C_3$are also connected in series. L_1, L_2, L_3, $L_4$and C_3 are discharged and transfer energy from the DC source to the load whereas C_1 and C_2 start to charge,

Thus the following equation can be obtained,

$$\left.\begin{aligned} V_{L1}+V_{L2} &= (V_g - V_{C1}) \\ V_{L3}+V_{L4} &= (V_{C3} - V_{C2}) \\ V_i &= (V_{C1}+V_{C2}) \end{aligned}\right\} \quad (1)$$

Where, $V_i$represents the peak DC link voltage.





$$\left.\begin{aligned} V_{L1} &= (V_g + V_{C2}) \\ V_{L2} &= V_{C2} \\ V_{L3} &= V_{L4} = V_{C3} = V_{C1} \end{aligned}\right\} \quad (2)$$

$$\left.\begin{aligned} V_{C3} &= \left(\frac{1-2D-3D^2}{1-2D+D^2}\right)V_{C2} - \left(\frac{2D}{1-2D+D^2}\right)V_g \\ V_{C3} &= \left(\frac{1-D}{1+D}\right)V_{C2} \end{aligned}\right\} \quad (6)$$

Equation (2) can be rewritten as:

$$\left.\begin{aligned} V_{L1}+V_{L2} &= (V_g + 2V_{C2}) \\ V_{L3}+V_{L4} &= 2V_{C3} = 2V_{C1} \end{aligned}\right\} \quad (3)$$

From (1) and (3) and based on the voltage second balance principal for the inductors L1, L2, L3 and L4, yields,

By solving (4), obtained,

$$\left.\begin{aligned} V_{C1} &= \left(\frac{1}{1-D}\right)(2DV_{C2} + V_g) \\ V_{C3} &= \left(\frac{1-D}{1+D}\right)V_{C2} \\ V_{C1} &= \left(\frac{1-D}{2D}\right)(V_{C2} - V_{C3}) \end{aligned}\right\} \quad (5)$$

By reduction (5) leads to,

Then, equation (6) yields to,

$$V_{C2} = \left(\frac{1+D}{1-4D-D^2}\right)V_g \qquad (7)$$

By Substituting (7) into (5); the capacitor voltage V c1 is

By Substituting (7) into (5); the capacitor voltage V c1 is

$$V_{C1} = V_{C3} = \left(\frac{1-D}{1-4D-D^2}\right)V_g \qquad (8)$$

So the peak DC link voltage can be obtained by
Substituting
(7) and (8) into (1),

$$V_i = \left(\frac{2}{1-4D-D^2}\right)V_g \qquad (9)$$

Subsequently, the boost factor (B) which represents the ratio between the peak DC link voltage (Vi) and the DC source voltage (Vg) can be presented as:

$$B = \frac{V_i}{V_g} = \frac{2}{1-4D-D^2} \qquad (10)$$

Also, the total gain (G) of the proposed topology can be written as:

$$G = BM = \frac{2M}{1-4D-D^2} \qquad (11)$$

Where M represents the modulation index.

It worth to mentioned that, the above equations are valid only in the case of boosting mode where shoot through duty cycle is larger than zero (D>0). Else, the following equation is valid:

$$\left.\begin{aligned} V_{C1} &= V_g \\ V_{C2} &= V_{C3} = 0 \\ V_i &= V_g \end{aligned}\right\} \qquad (12)$$

According to (11), the proposed topology has larger boost factor at small value of shoot through duty cycle where theoretically it equals to infinity value at D=0.24 as shown in Fig. 7.

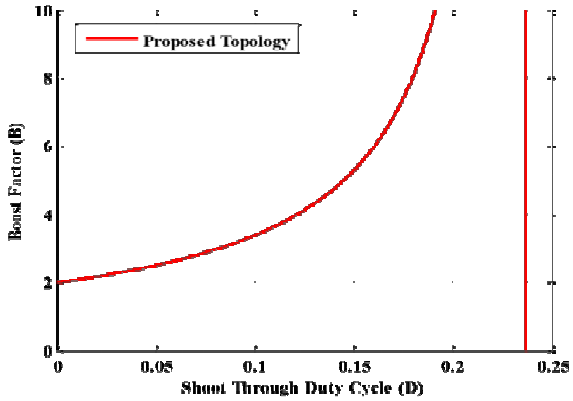


Fig.7. Boost Factor (B) versus Shoot Through Duty Cycle (D).

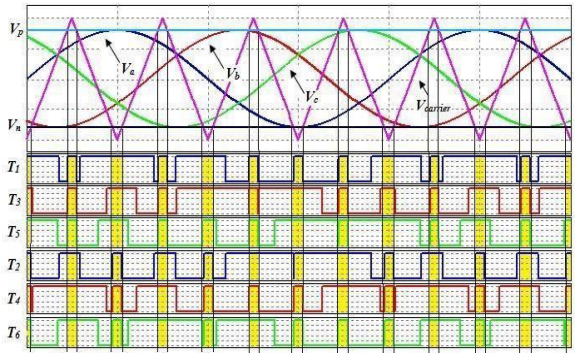


Fig.8. Simple boost control technique.

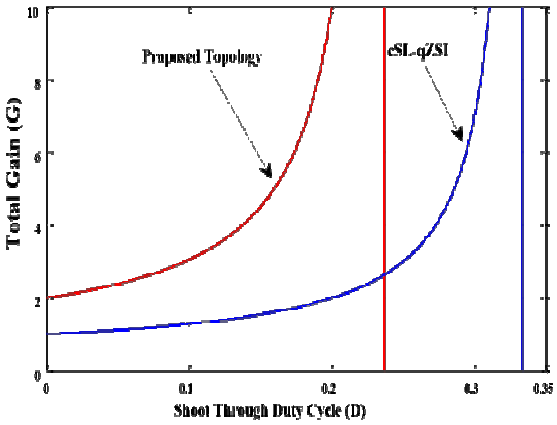


Fig. 9 Total Gain (G) versus shoot through Duty Cycle (D) for the proposed topology versus the conventional cSL-qZSI topology.

IV. COMPARSION WITH CSL-QZSITOPOLOGY

The comparison between the proposed topology (MTSLqZSI) and the classic one (cSL-qZSI) can be organized fromthe following points of view,

A.The boost ability

The boost factor of (cSL-qZSI) can be expressed as [12],[14]

By applying the same PWM control methods to generate the shoot through duty cycle of the two topologies; if they

have the same shoot through duty cycle *(D),* they will have the same modulation index *(M)*, but the MTSL-qZSI has larger boost factor *(B)* than cSL-qZSI so it has the largest total gain as shown in Fig. 9.

Thus, to obtain the same total gain (*G*) from the two topologies, (MTSL-qZSI) topology requires a smaller shoot through duty cycle *(D)* than with (cSL-qZSI) topology, this leads to the proposed topology to operate at higher modulation index *(M)* which improves the performance of the topology in reduction the total harmonics distortion in the output of the inverter. Therefore, a low size filter is used to get sinusoidal output voltage.

B.Voltage Stress

The voltage stress across the used capacitor effect on the cost of the system where larger voltage stress requires using a capacitor that can withstand that high voltage stress across it and this will be costly [15]. As a larger gain is obtained with small shoot through, the voltage stress across the used capacitors and switched devices may be smaller. The voltage across the capacitor *C1*and

*C2*for (cSL-qZSI) topology can be written as [12],

As shown in Fig.10, at the same total gain *(G)* the stress across the capacitor *C1* is smaller for the proposed topology compared to cSL-qZSI topology. On the other gain *(G),*so the proposed topology give an improvement in the

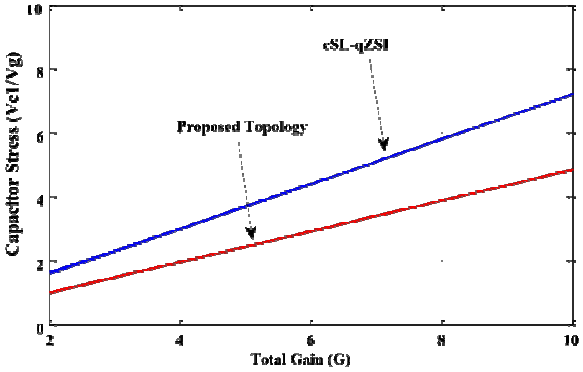
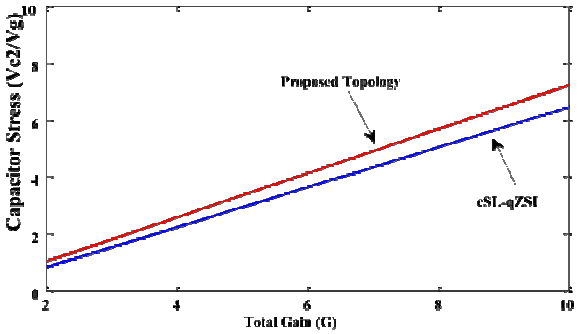


Fig. 10. Voltage stress across C1 versus the total gain (G) for the proposed topology versus the conventional cSL-qZSI topology.



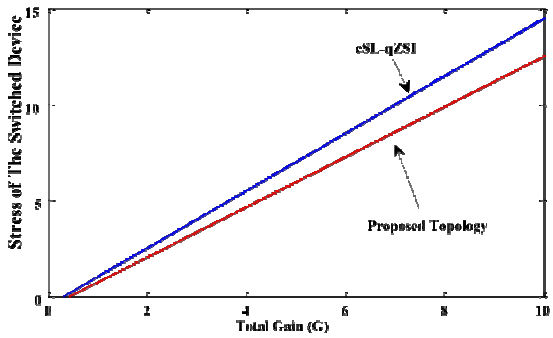


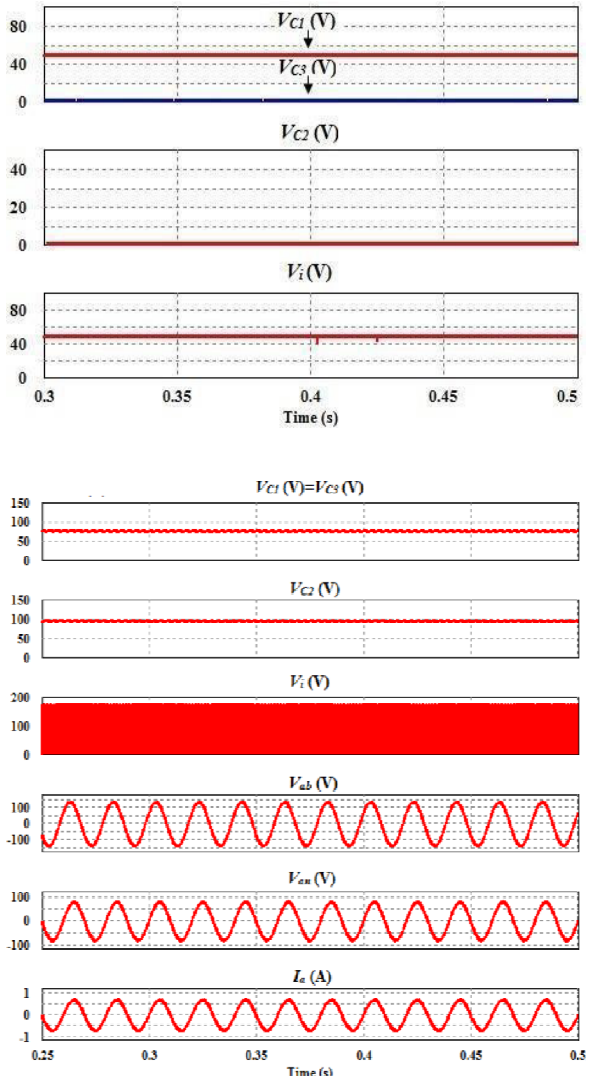
Fig.11. Voltage stress across C2 versus the total gain (G) for the proposed topology versus the conventional cSL-Qzsi topology.

In Fig. 12; it is obviously that at the same total gain, the voltage stress V_S across the switched devices (IGBTs) for the proposed topology is smaller than that for cSL -qZSI topology. This can be explained as it requires small shoot

through duty cycle *(D)* to give the same total gain, so it has larger modulation index (*M)*. So, the proposed topology has more freedom in selecting the switched devices rating compared to cSL-qZSI.

V. SIMULATION RESULTS

Simulation under PSIM program has been performed to validate the feasibility of the proposed topology. The simulation is applied to the proposed topology based on the parameters listed in Table I.



Firstly, the simulation work is implemented with shoot through duty cycle at D=0.1. According to (7) to (11) and (13), the following values can be evaluated at D=0.1:0.9, B= 3.389, G= 3.05, Vi= 169.5V, $VC1$= 76.27V, $VC2$= 93V, $VC3$= 76.27V, Van (rms) = 53.9V, Vab (rms) = 93.4V and Ia (rms) = 0.49A.The simulations results are presented in Fig. 13, where the capacitor voltages $VC1$ and $VC3$ have the same value of 78V, the capacitor voltage $VC2$ equals 96V, the peak value of DC -link voltage Vi equals 174V, the rms value of line voltage equals 100 V, the rms value of phase voltage equals 57.7V and the rms value of output load current equals 0.52A.

Secondly, simulation work is performed at $D = 0$ to show the validation of (12) and the following values can be calculated at $D = 0$:

M= 1, B= 1, G= 1, Vi= 50V, $VC1$= 50V, $VC2$=$VC3$= 0V. The simulations results are presented in Fig. 14, where the

Fig. 14. Simulation results at D=0.

Capacitor voltages $VC1$ equals 50V, the capacitor voltage $VC3$ equals 0 V, the capacitor voltage $VC2$ equals 0V, the peak value of DC-link voltage Vi equals the value of the input DC source 50V.

VI. EXPERIMENTAL RESULTS

The experimental work is carried out for the proposed topology with the same parameters applied in the simulation test. The control is developed using the digital signal processing kit TMDSCNCD28335 which is linked with PSIM program. A laboratory prototype for the proposed topology (MTSL-qZSI) is constructed and the experimental setup is shown in Fig. 15. The shoot through duty cycle *(D)* for experimental work is taken as the same value of shoot through duty cycle in simulation work D=0.1. Also, the firing scheme from the control kit before the gate

drive circuit for upper and lower switch in one phase leg of the inverter is shown in Fig.16.

The measurements for DC side of MTSL-QZSI are shown in Fig. 17 where the input voltage of the DC source equals 50V, the voltage across the capacitor $C1(VC1)$ equals 76.5V, the voltage across the capacitor $C2$ $(VC2)$ equals 79.27V and the peak DC link voltage (Vi) equals 155.5V. The measurements for AC side are shown in Fig. 18 where the rms value of line to line voltage (Vab) equals 87V, the rms value of phase voltage (Van) equals 48.89V and the rms value of load current equals 447mA.There is a slightly difference between the theoretical results and experimental results due to the parasitic impedances for the used components.

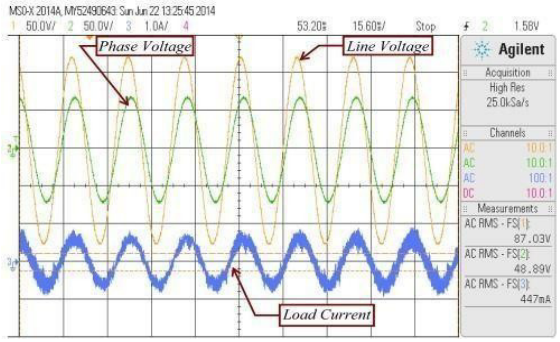


Fig. 16. Firing pulses for the two switches of one phase.

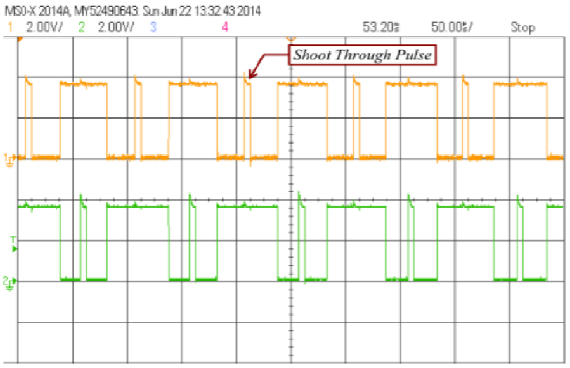


Fig.17. DC side measurements.

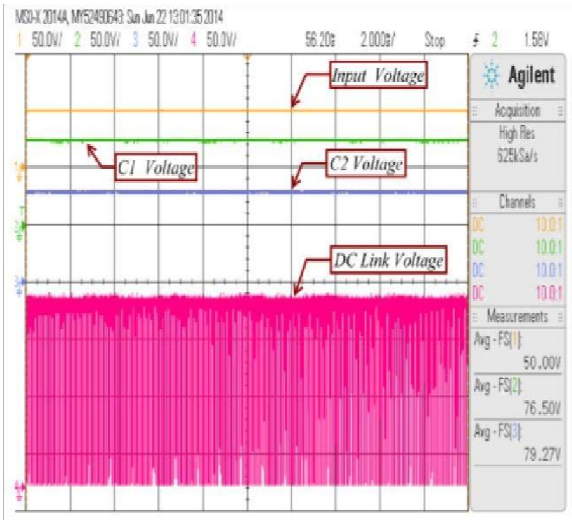


Fig. 18. AC side measurements

VII. CONCLUSION

This paper presents a modified topology for the development of the features of Z-source Inverter (ZSI) as a single stage inverter. The principal of the proposed topology depends on using the idea of bootstrap capacitor instead of the middle diode in the second switched cell in the continuous two switched inductor quasi ZSI (cSL- qZSI) topology. It can be summarized the following advantages for the proposed topology (MTSL-qZSI):

Larger boost factor (B) than any other topology that related with Z-source Inverter field, up till now.

- ✓ Continuous input current drawn from the source.
- ✓ Common mode feature.
- ✓ Slightly improving in capacitor stress compared to similar classic one cSL-qZSI.

Obtaining larger gain with short shoot through lead to operating at higher modulation index (M) which results in reducing the stress on the switched devices and improving the total harmonic distortion for the inverter output so, low size output filter is required. Improving in conversion efficiency due to

using the capacitor instead of the diode compared to cSL-qZSI.

Therefore, the above advantages allow the proposed topology (MTSL-qZSI) to be widely used as an inverter topology.

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