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Research Article

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D.C conductivity, Hall effect of amorphous Arsenic and I-V characteristic of a-As/c-Si Heterojunction

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Abstract In this research the a-As films have been prepared by thermal evaporation with thickness 500 nm and rata of deposition $r_{d|}$(2.083nm/sec) as function to annealing temperature (373 and 473K), from d.c conductivity found the electrical activation energy E_a increase from (0.296 to 0.340) ev with increasing of annealing temperature. Hall measurement showed that all films are n-type. Electrical properties of a-As/c-Si heterojunction include I-V characteristic in dark and under illumination at different annealing temperature.

Keywords D.C conductivity, Hall effect, Arsenic, a-As/c-Si Heterojunction

Introduction

The heterojunction device of the amorphous- crystalline semiconductor type have been much attention considerable interest from researchers both from a fundamental physics and technological field, for example Mimerand Hatenaka 1987 [1] showed that a-Si:H/c-Si has application to imaging devices, Kentaro and Nakazawa 1988; Lovejoy 1992 have also studied amorphous-polycrystalline of silicon films have possible application in a photoelectonics [2]. Amorphous arsenic generally, were among the first and most widely investigated amorphous semiconductors [3], the understanding of the behavior of arsenic in highly doped near surface silicon layers is of crucial importance for the formation of *n* -type ultra shallow junctions in current and future very large scale integrated technology [4]. This is of particular relevance when studying recently developed implantation and annealing methods, The use of arsenic as *n*-type dopant silicon has been extensively investigated and applied for the past and present semiconductor technology. Compared to other *n*-type dopants, arsenic offers a relatively high solid solubility and a high mass that gives low penetration depth when the dopant atoms are introduced by ion implantation [5]. In this paper we will study the D.C conductivity and Hall effect of amorphous Arsenic films and study dependence of I-V for a-As/c-Si on T_a.

Experimental Details

Substrate of p-type single crystal Si wafers with orientation (111) were used in the present study. After scribing these wafers in to small pieces (typically 1 cm^2 in size), with one surface polished with 3ml HNO_3 1ml H_2O for 1-3 minutes and they where dried by using blower and wiped with soft paper before arsenic deposition [6]. The films of a-As were prepared by thermal evaporation under vacuum of the order of 10^{-5} Torr, of deposition was ≈ 2.083 nm/sec onto clean Silicon mirror-like side substrate at room temperature (~300 K). The average thickness of the deposit were determined by microbalance method The maximum error in the determinate of thickness was of the order of 10% estimated for the thinnest films (As/Si films of thickness 500 nm). Ohmic contact of Al study on the electrical properties a-As/c-Si Heterojunction aluminum were evaporated on the Silicon side and As/Si side.

Results and Discussion

D.C conductivity of a-As films

The d.c conductivity for a-As films has been studied as a function of 1000/T.

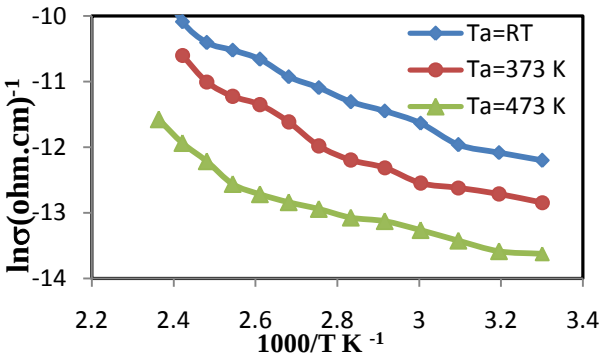

Figure 1: Lnσ as a function of 1000/T for a-As

Table 1: D.C activation energy

T_a K	E_a (eV) (303-423)K	$\sigma_{R.T} \times 10^{-7}(\Omega.cm)^{-1}$
300	0.296	56.7
373	0.307	30.1
473	0.340	12.6

Table (1) shows the effect of annealing temperature on (E_a) at (T_a=373 and 348K) for a-As. It is found that the activation energy tends to increasing with the increasing of the annealing temperature. This increasing is obviously due to the increasing in the energy gap, which may be due to the dense in the V.B & C.B. The effect is shown clearly by the improvement in crystallinity during annealing these results are agreement with [7].

Hall Effect

The type of charge carriers, carrier concentration (n_H), Hall mobility (μ_H) of charge carriers have been estimated from Hall measurements. The variation of Hall voltage with current for a-As films deposition at R.T for different annealing temperatures are shown in figure (2) and figure (3).

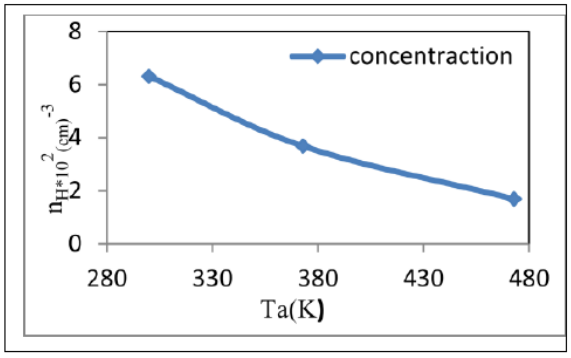

Figure 2: Hall concentration decrease with increasing annealing temperature

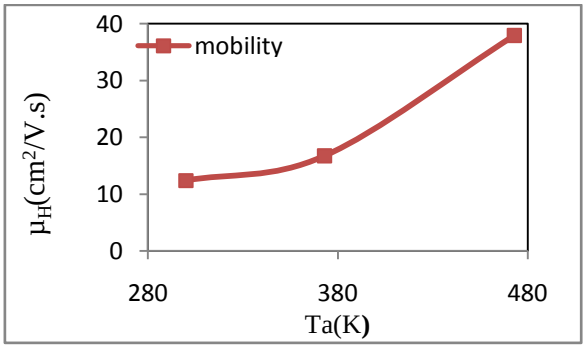

Figure 3: Hall mobility increase with increasing annealing temperature

It can be observed from these figures that the carrier's concentration decrease and mobility increases on increasing annealing temperatures. This may be due to the decrease in the dangling band inside the energy gap due and to the amorphous-to-polycrystalline transformation which increases with the increasing of annealing temperature. These results are in agreement with Akram [8].

I-V characteristic of a-As /c-Si

(a) Under dark

The I-V characteristic of a-As/c-Si as show the forward I-V characteristic for a junction is described by the thermionic emission relation:

$$J_F = J_S \exp qV_F/nK_BT$$

A sime –log J-V plot under forward bias for annealed and unannealed for a-As/c-Si heterojunction at forward and reverse bias voltage is presented in figure (4). The ideality factor of the diodes is in value (1.5-2) for sample prepared at RT and annealing with 473K. This value reflected that the carriers transport is taken place by tunneling and recombination mechanisms associated with the thermionic emission mechanism.

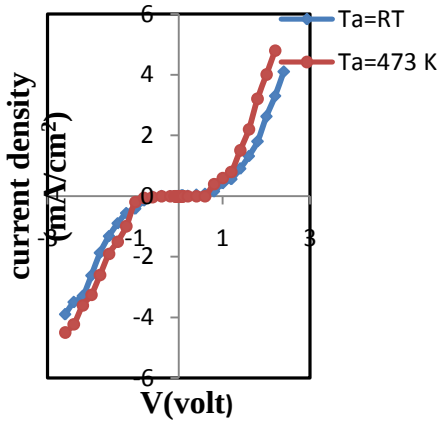

Figure 4: Forward J-V characteristic for a-As/c-Si annealed and unannealed heterojunction

In general the forward dark current is generated due to the flow of majority carriers and the applied voltage injects majority carriers which lead to the decrease of the built-in potential, as well as the width of the depletion layer. We also observed that the current increases slightly with increasing of annealing temperature because the increasing of temperature causes as rearrangement of the interface atoms and reduce the dangling bond , surface state and dislocation at interface layer between a-As and c-Si which leads to improvement of the junction characteristics this behavior are agreement with [9] .

(b) I-V characteristic of a-As /c-Si under illumination

The (I-V) for a-As/c-Si characteristic under illumination shown in figure (3) , in the forward bias the current increased exponentially with voltage as expected, but in reverse bias the current was found to be increasing slowly with voltage (soft break down) and did not show any trend of saturation or sharp breakdown ,From this figure we can see that the V_{oc} increase with T_a, this may be associated with reduction the recombination center in term important the crystal structure similar variation have been pointed in ref [10].

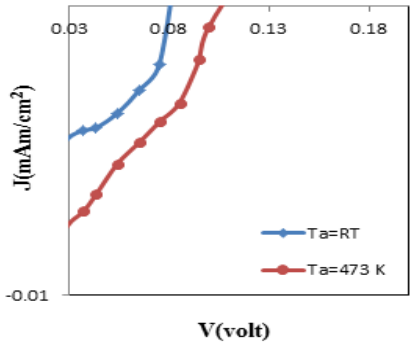

Figure 5: I-V characteristic under illumination for a-As/c-Si heterojunction at 300K and 473K

We observe the photocurrent density increases with increasing of the bias voltage

Table 1: Value of V_{OC}, $J_{Sh.C}$, J_{sh}, V_{max}, $I_{s\,max}$ and ideality factor for a-As/c-Si heterojunction

Th .µm	T_a K	n	$J_s \times 10^{-7}$ (Am)	V_{oc} (Volt)	I_{sc} (mA/cm)	V_{max} (Volt)	$I_{s\,max}$ (mA/cm^2)
0.5	R.T	2.08	18	0.09	0.012	0.06	0.01
	473	2.03	12	0.11	0.019	0.08	0.04

Conclusion

From what has been mentioned, we can concluded that the activation energy increase with increasing annealing temperature, from Hall measurement we notice that all films are n-type, the current-voltage measurement of a-As/c-Si in the dark case to deduce that the value of ideality factor decrease with increasing of annealing temperatures, also the J_{sc} and V_{oc} increase with the increasing of annealing temperature.

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