Available online www.ejaet.com

European Journal of Advances in Engineering and Technology, 2015, 2(7): 82-87

Research Article ISSN: 2394 - 658X

Low Power and Low Frequency CMOS Ring Oscillator Design

Venigalla Ravi Kanth and K Naresh Kumar

Department of Electronics and Communication
Gayatri Vidya Parishad College of Engineering (Autonomous), Visakhapatnam, Andhra Pradesh, India
ravikanthvenigalla90@gmail.com

ABSTRACT

This paper presents the concept of ring oscillator design using CMOS thyristor techniques. They generate extremely low frequency signals. They are implemented in 180nm technology with 1.8 volt (or) 2.5 volt power supply and 0.8pF load capacitance. Conventional CMOS ring oscillator generates the frequency of the order of MHz. In order to generate low frequency signals CMOS thyristor technique is introduced. It generates the frequency of the order of Hz. To further reduce the frequency of the output waveform CMOS thyristor with current mirrors are introduced. They generate the frequency of the order of few Hz hence these are the proposed circuits. The power consumption of these proposed circuits are less when compared to the conventional CMOS ring oscillator.

Key words: CMOS Thyristor, Extremely Low Frequency, Current Mirror

---

INTRODUCTION

Extremely low frequency signals have various applications. For example, the use of extremely low frequency signals having the frequency of the order of 0 to 300Hz is widely used in Navy as radio band and radio communication. In power grids 60Hz or 50Hz are used to generate for alternating current. The conventional CMOS ring oscillator generates the frequency of the order of MHz. To generate low frequency signals of the order of hundreds of Hz using conventional CMOS ring oscillator not only increases the number of inverters but also increases the static power dissipation of the circuit. In order to generate low frequency signals CMOS thyristor technique is used. It generates the low frequency signals having the frequency of the order of hundreds of Hz as well as it reduces the static power dissipation of the overall circuitry. In this paper few circuits using CMOS thyristor with current mirror are proposed to achieve the objective, which generate the output waveform having the frequency of the order of Hz. It consumes less average power than the conventional CMOS ring oscillator.

Firstly the design of conventional CMOS ring oscillator and operation of CMOS thyristor technology is discussed. In next part the information of CMOS thyristor based current mirrors and proposed circuits is presented. The proposed circuits are CMOS thyristor with cascode current mirror and CMOS thyristor with triple cascode current mirror. They generate the frequency of the order of few Hz.

CONVENTIONAL CMOS RING OSCILLATOR

Conventional CMOS ring oscillator is implemented by connecting odd number of CMOS inverters in a closed loop. In Figure 1, the conventional CMOS ring oscillator is designed by connecting 3 numbers of CMOS inverters. Each CMOS inverter has one PMOS and one NMOS [1-3]. If logic '1' is given as an input to the inverter then logic '0' is the output of the inverter and vice-versa. In order to get sustained oscillations in the loop, Barkhausen Criterion should be satisfied. According to Barkhausen criterion, the loop gain is equal to unity.

To get sustained oscillations in the loop, odd number of inverters is connected in the loop. This means, the output of last inverter stage is connected to the input of the first inverter stage. The conventional CMOS ring oscillator generates the frequency of the order of MHz.

The frequency of the output waveform is given by $F_{out} = 1/(2.N.T_P)$
Where N – The odd number of CMOS inverters.
T_P – The average propagation delay from high to low and from low to high transition of each CMOS inverter stage.

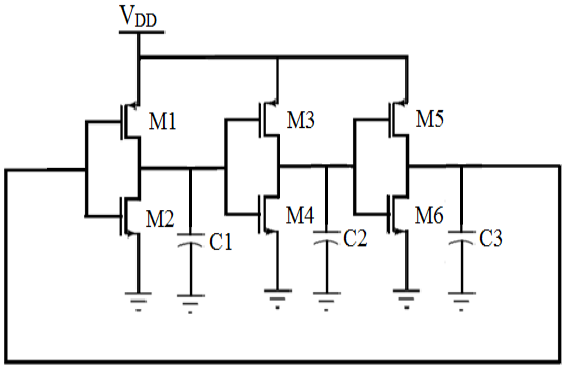

Fig. 1Conventional CMOS Ring Oscillator

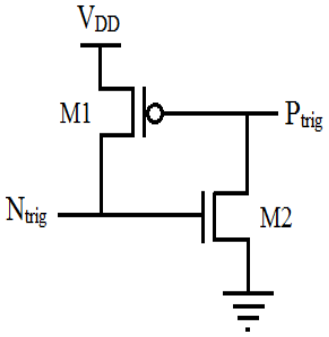

Fig. 2 CMOS Thyristor Circuit

To generate low frequency signals of the order of hundreds of Hz using conventional CMOS ring oscillator not only increases the number of inverters but also increases the static power dissipation of the circuit. The conventional CMOS ring oscillator is implemented in Tanner EDA Tools then the frequency of the output waveform is 16.89MHz. Keeping (W/L) ratios constant, around 600 CMOS inverters are required to generate the frequency of the order of KHz hence the chip area of the circuit is increased and the static power dissipation of the circuit is also increased. In order to generate low frequency signals, CMOS thyristor technique is used to design ring oscillator. It generates the frequency of the order of Hz and improves the static power dissipation of the circuit.

CONVENTIONAL CMOS THYRISTOR TECHNIQUE

To solve the above problem, CMOS thyristor based inverter is introduced. It is less sensitive to voltage variation and it mainly operates on leakage currents. It acts as a delay element. The operation of the CMOS thyristor circuit is explained with the help of figure shown in fig. 2.

It has two triggering modes Ntrig and Ptrig. No current is passed through the CMOS thyristor until it is triggered. If Ptrig is precharged to V_{DD} and Ntrig is predischarged to ground then the CMOS thyristor is turned OFF. The thyristor is triggered with the voltage of either Ptrig or Ntrig. Without loss of generality, Ptrig is taken as the triggering mode. When Ptrig is discharged down to $V_{DD} - V_T$, M1 conducts at most the subthreshold current. This feature provides negligible power consumption before turn ON of the thyristor. Once M1 is turned ON, M1 charges Ntrig and M2 discharges Ptrig in turn. The positive feedback mechanism in this turn ON operation provides a quick flipping of the state and reduces the dynamic power consumption. This CMOS thyristor is operated with a low supply voltage down to $1.5V_T$ since there is no stacked structures which require more voltage margin. This gives the low voltage operation of the delay element [4].

The basic structure for ring oscillator using CMOS thyristor is shown in figure 3. It has two numbers of inputs R and R_bar. It also has two complementary outputs Q and Q_bar. These inputs and outputs are connected in cascaded form as shown in figure 4 then ring oscillator using CMOS thyristor technique can be realized [5]. M1 and M2 are CMOS thyristor circuit elements. M3 and M4 are connected to CMOS thyristor circuit. Initially, Q is precharged to V_{DD} (logic 1) and Q_bar is predischarged to ground (logic 0) then the CMOS thyristor is in OFF state. There are two cases. One is, R and R_bar are logic 0 and logic 1 respectively. In this case M3 and M4 are turned ON. M3 brings Q to strong 1 and M4 brings Q_bar to strong 0 even if leakage currents occur in CMOS thyristor circuit elements M1, M2. So CMOS thyristor remains in OFF state. Hence Q and the Q_bar values do not change i.e. logic 1 and logic 0 respectively. In the second case, R and R_bar are logic 1 and logic 0 respectively. In this case, M3 and M4 are turned OFF. Owing to leakage currents, CMOS thyristor circuit is turned ON. The values of Q and Q_bar are changed as logic 0 and logic 1 respectively. The CMOS thyristor element is implemented in Tanner EDA Tools. The frequency of the output waveform is 53.64Hz.

To further reduce the frequency of output waveform, CMOS thyristor with footer transistor is introduced and is shown in figure 5. It has footer transistor. This footer transistor acts as an active load hence the charging and discharging time of the load capacitor increases thus lowering the frequency of output waveform. It has two numbers of inputs R and R_bar and two numbers of outputs Q and Q_bar. By connecting inputs and outputs in cascaded form as shown in figure 4, ring oscillator using CMOS thyristor with footer transistor technique can be realized [5].

M1 and M2 are CMOS thyristor circuit elements and M6 is the footer transistor. CMOS thyristor with footer transistor generates large time delay when compared to previous circuits hence low frequency is obtained. The operation of the CMOS thyristor circuit is same as discussed earlier. The CMOS thyristor with footer transistor is implemented in Tanner EDA Tools. The frequency of the output waveform is 53.50Hz.

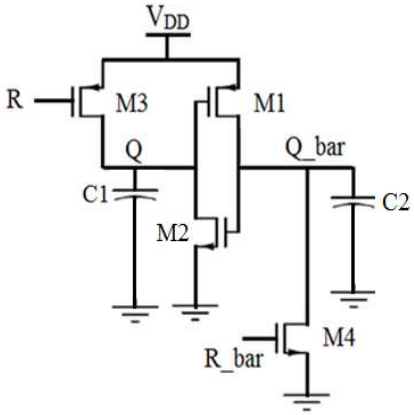

Fig. 3 CMOS Thyristor Element

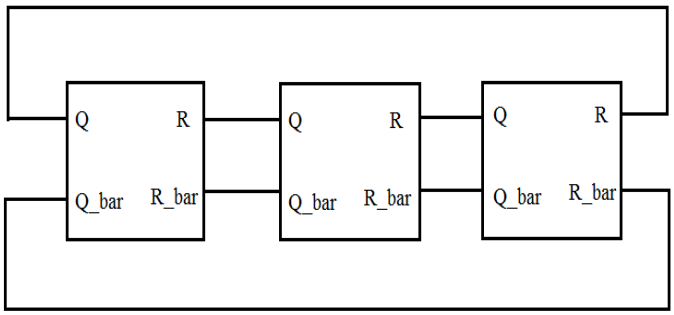

Fig. 4 Block Diagram for Ring Oscillator Design Using CMOS Thyristor

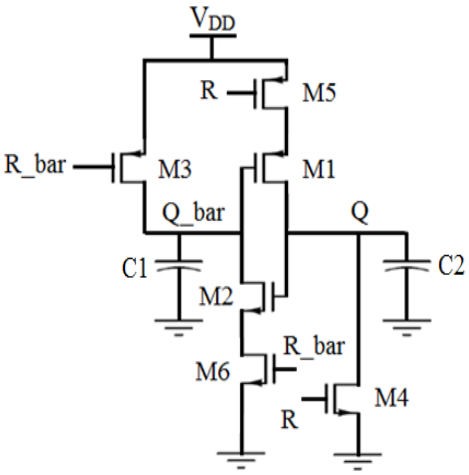

Fig. 5 CMOS Thyristor with footer Transistor for Ring Oscillator Design

CMOS THYRISTOR WITH CURRENT MIRRORS

Ring oscillator is designed by using CMOS thyristor technique along with current mirror. The CMOS thyristor with single current mirror is shown in figure 6, which has two complementary outputs i.e. Q and Q_bar. It has two numbers of inputs i.e. R and R_bar. By connecting outputs and inputs in cascaded form as shown in figure 4, ring oscillator using CMOS thyristor with single current mirror technique can be realized [6].

CMOS thyristor with single current mirror has one current mirror pair M3-M5. This current mirror acts as an active load and it controls the current through the CMOS thyristor transistors M1-M2. That means, very less leakage current flows through the CMOS thyristor transistors M1-M2. The CMOS current mirror allows less current to the transistor M7 hence the charging and discharging time of load capacitor at M7 transistor increases thus lowering the frequency of output waveform. The operation of the CMOS thyristor circuit is same as discussed earlier. The CMOS thyristor with single current mirror is implemented in Tanner EDA Tools then the frequency of the output waveform is 37.16Hz.

To further reduce the frequency of the output waveform, one more current mirror pair M4-M6 is added to the CMOS thyristor with single current mirror then this circuit is called CMOS thyristor with double current mirror. It is shown in figure 7. It has two numbers of inputs R and R_bar. It also has two numbers of outputs Q and Q_bar. By connecting inputs and outputs in cascaded form as shown in figure 4, ring oscillator using CMOS thyristor with double current mirror technique can be realized [6].

Current mirror pair M4-M6 acts as an active load which further reduces the current through the transistor M8 hence charging and discharging time of load capacitor at M8 transistor increases thus lowering the frequency of output waveform. In both of the single and double current mirrors with CMOS thyristor structures, the ratio of mirrored current to the reference current is kept at 1:1. The operation of the CMOS thyristor circuit operation is same as discussed earlier. The CMOS thyristor with double current mirror is implemented in Tanner EDA Tools then the frequency of the output waveform is 8.51Hz.

To further reduce the frequency of the output waveform, CMOS thyristor with cascode current mirror and CMOS thyristor with triple cascode current mirror are introduced. These circuits are proposed circuits because they generate the frequency of the order of below 2Hz. The CMOS thyristor with cascode current mirror is shown in

figure 8. It has two numbers of inputs R and R_bar. It also has two complementary outputs Q and Q_bar. By connecting inputs and outputs in cascaded form as shown in figure 4, ring oscillator using CMOS thyristor with cascode current mirror technique can be realized. Cascode current mirror has large output impedance than simple current mirror hence it allows less leakage current to the CMOS thyristor transistors M1-M2.

Cascode current mirror allows less current to transistors M11 and M12 hence the charging and discharging time of the load capacitors at M11 and M12 increases thus lowering the frequency of output waveform. The operation of the CMOS thyristor circuit is same as discussed earlier. If CMOS thyristor with cascode current mirror is implemented in Tanner EDA Tools then the frequency of the output waveform is 1.038Hz.

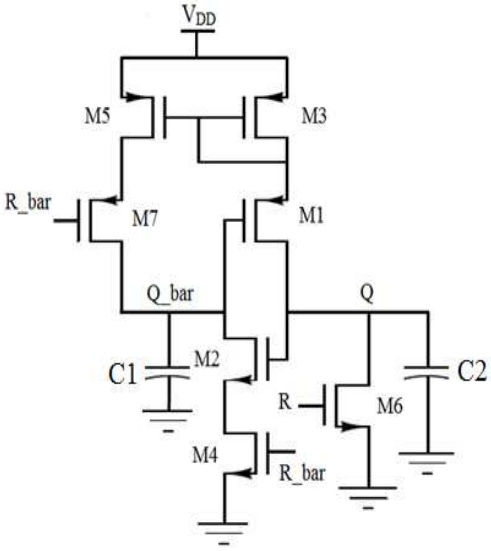

Fig. 6 CMOS Thyristor with Single Current Mirror

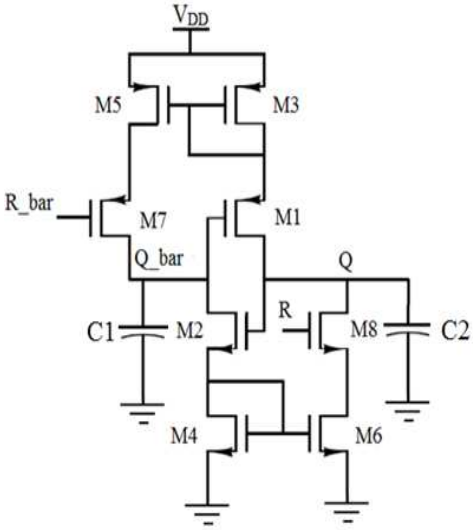

Fig. 7 CMOS Thyristor with Double Current Mirror

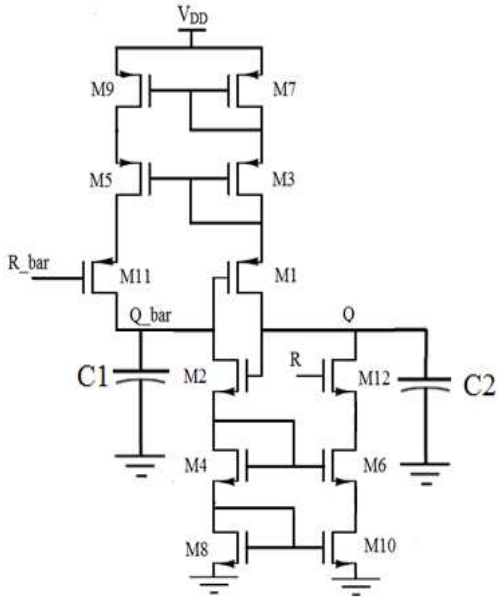

Fig. 8 Proposed CMOS Thyristor with Cascode Current Mirror

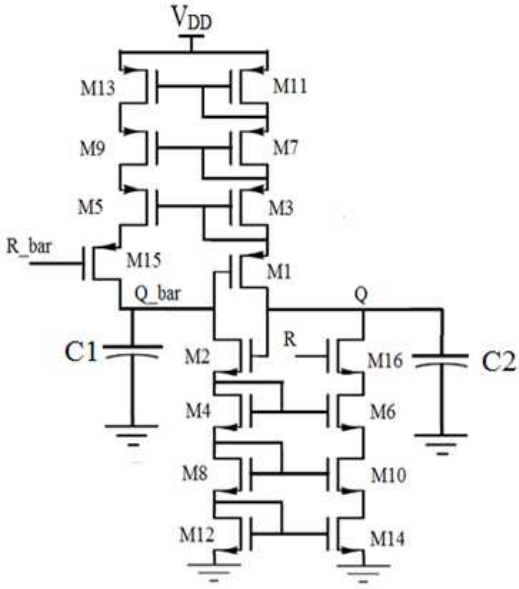

Fig. 9 Proposed CMOS Thyristor with Triple-Cascode Current Mirror

To further reduce the frequency of output waveform, CMOS thyristor with triple cascode current mirror is introduced and is shown in figure 9. It has two numbers of inputs R and R_bar. It also has two complementary outputs Q and Q_bar. By connecting inputs and outputs in cascaded form as shown in figure 4, ring oscillator using CMOS thyristor with triple cascode current mirror technique can be realized. The triple cascode current mirror has large output impedance than cascode current mirror and simple current mirror hence it allows less leakage current to the CMOS thyristor transistors M1-M2. The triple cascode current mirror allows less current to transistors M15 and M16 hence the charging and discharging time of the load capacitors at M15 and M16 increases thus lowering the frequency of output waveform. The operation of the CMOS thyristor circuit is same as discussed earlier. The CMOS thyristor with triple cascode current mirror is implemented in Tanner EDA Tolls then the frequency of the output waveform is 0.303Hz.

Figure 10 and 11 show the transient responses for the proposed structures shown in figure 11 and 12 respectively. Table -1 shows the comparison of conventional CMOS ring oscillator, CMOS thyristor element and CMOS thyristor with footer transistor for ring oscillator design. Table -2 shows the comparison of different CMOS thyristor based techniques for ring oscillator design. Table -3 shows effect of voltage variations on the time periods of output waveforms of different CMOS thyristor based techniques for ring oscillator design.

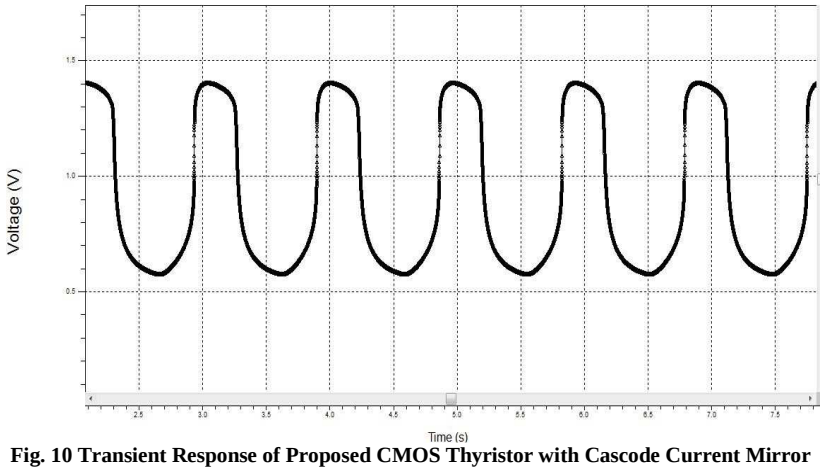

Fig. 10 Transient Response of Proposed CMOS Thyristor with Cascode Current Mirror

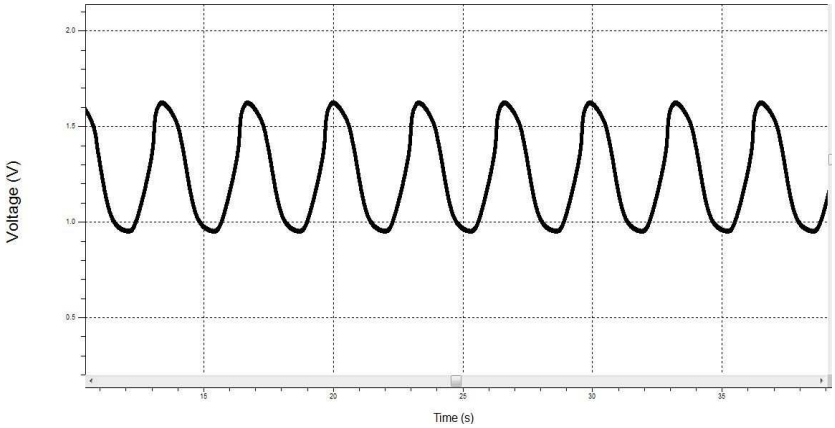

Fig. 11 Transient Response of Proposed CMOS Thyristor with Triple Cascode Current Mirror

Table -1 Comparison of Conventional CMOS Ring Oscillator, CMOS Thyristor Element and CMOS Thyristor with Footer for Ring Oscillator Design

S.No	Parameter	Fig 1	Fig 3	Fig 5
1	Supply Voltage	1.8 V	1.8 V	1.8 V
2	Vmin	0 V	0 V	0 V
3	Vmax	1.8 V	1.8 V	1.8 V
4	TP	59.20 NS	18.64 MS	18.69 MS
5	Frequency	16.89 MHZ	53.64 HZ	53.50 HZ
6	Average Power	185 µW	5.52 µW	0.151 µW

Table -2 Comparison of Different CMOS Thyristor Based techniques for Ring Oscillator Design

S.No	Parameter	Fig 6	Fig 7	Fig 8	Fig 9
1	Supply Voltage	1.8 V	1.8 V	1.8 V	2.5 V
2	Vmin	0 V	210 mV	566.10 mV	942.46 mV
3	Vmax	1.72 V	1.7 V	1.4 V	1.62 V
4	TP	26.91 ms	117.43 ms	963.14 ms	3.30 s
5	Frequency	37.16 Hz	8.51 Hz	1.038 Hz	0.303 Hz
6	Average Power	1.77 nw	1.39 nw	2.56 nw	6.62 nw

Table -3 Effect of Voltage Variations on The Time Periods of Output Waveforms of Different CMOS Thyristor Based Techniques for Ring Oscillator Design

S.No.	Voltage	Fig 6	Fig 7	Fig 8	Fig 9
1	1.8 V	26.91 ms	117.43 ms	963.14 ms	-
2	2 V	23.11 ms	100.20 ms	758.60 ms	-
3	2.5 V	16.30 ms	69.30 ms	455.70 ms	3.30 s
4	3 V	12.00 ms	50.70 ms	304.20 ms	2.65 s
5	3.5 V	8.87 Ms	37.10 ms	215.30 ms	1.81 s

CONCLUSION

CMOS thyristor based cascode current mirror and CMOS thyristor based triple cascode current mirror are the proposed structures for generating low frequency signals. The CMOS thyristor based triple cascode current mirror is generating the frequency of 0.303Hz. The CMOS thyristor with triple cascode current mirror has small votage swing thus the minimum voltage of this circuit is large when compared to other circuits and consumes more average power than the CMOS thyristor with cascode current mirror. The CMOS thyristor based cascode current mirror is generating the frequency of 1.038Hz and consumes less average power than the conventional CMOS ring oscillator circuit. For low frequency application, CMOS thyristor based triple cascode current mirror circuit is better than the CMOS thyristor based cascode current mirror and consumes less average power than the conventional CMOS ring oscillator. From Table III, while increasing the supply voltage, the time periods of the circuits are decreased hence frequency is increased. It is clearly concluded that low supply voltage is preferred than higher supply voltage.

REFERENCES

[1] Shruti Suman, Monika Bhardwaj and BP Singh, An Improved Performance Ring Oscillator Design, *IEEE Second International Conference on Advanced Computing & Communication Technologies (ACCT)*, **2012**, 236-239.
[2] B Razavi, A Study of Phase Noise of in CMOS Oscillator, *IEEE Solid-State Circuits*, **1996**, 31, 331–343.
[3] YA Eken and JP Uyemura, A 5.9 GHz Voltage Controlled Ring Oscillator, *IEEE Solid-State Circuits*, **2004**, 39, 230–233.
[4] Gyudong Kim, Min Kyu Kim, Byoung Soo and Wonchan Kim, A Low Voltage, Low Power CMOS Delay Element, *IEEE Solid State Circuits*, **1996**, 31, 966–971.
[5] Piyush Keshri and Biplab Deka, *CMOS Thyristor Based Low Frequency Ring Oscillator*, Indian Institute of Technology, Kanpur, India.
[6] Ajay Kumar Mahato, *Ultra Low Frequency CMOS Ring Oscillator Design*, National Institute of Technology, Sikkim, India, **2014**.