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ANALYSIS OF CMOS BASED FULL ADDERS FOR MOBILE COMMUNICATIONS

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Abstract:

As technology scales into the nanometer regime leakage power and noise immunity are becoming important metric of comparable importance to active power, delay and area for the analysis and design of complex arithmetic and logic circuits. In this project, low leakage 1 -bit full adder cells are proposed for mobile applications. For the most recent CMOS feature sizes (e.g., 180nm), leakage power dissipation has become an overriding concern for VLSI circuit designers. The main goal is to reduce leakage power. Therefore a new transistor resizing approach is used for 1-bit Full Adder cells. The simulation results depicts that the proposed design also leads to efficient 1-bit full adder cells in terms of standby leakage power. In order to verify the leakage power, various designs of full adder circuits are simulated using DSCH, Micro wind and Virtuoso (Cadence).

Keywords **— CMOS, 1-bit Full Adder, leakage power, noise immunity.**

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I. INTRODUCTION

In recent years, several variants of different logic styles have been proposed to implement 1-bit adder cells. These adder cells commonly aimed to reduce power consumption and increase speed. These studies have also investigated different approaches realizing adders using CMOS technology. For mobile applications, designers have to work within a very tight leakage power specification in order to meet product battery life and package cost objectives. The designer's concern for the level of leakage current is not related to ensuring correct circuit operation, but is related to minimize power dissipation.

An When an electronic device such as a mobile phone is in standby mode, certain portions of the circuitry within the electronic device, which are active when the phone is in talk mode, are shut down. These circuits, however, still have leakage currents running through them. The leakage current depletes the battery charge over the relatively long standby time, whereas the operating current during talk time only depletes the battery charge over the relatively short talk time.

As a result, the leakage current has a disproportional effect on total battery life. This is why building low leakage adder cells for mobile applications are of great interest.

Shortening the gate length of a transistor increases its power consumption due to the increased leakage current between the transistors source and drain when no signal voltage is applied at the gate. The leakage power is expected to reach more than 50% of total power in sub 100nm technology generation. The main reason is that leakage current increases exponentially as the feature size shrinks. Techniques for leakage power reduction can be grouped in two categories: state-preserving techniques where circuit state (present value) is retained and state-destructive techniques where the current Boolean output value of the circuit might be lost. A state-preserving technique the circuitry can resume operation at a point much later in time without having to somehow regenerate state. Our new design technique, which we call the “sleepy stack” technique, retains data during sleep

mode while providing reduced leakage power consumption at a cost of slightly increased delay. Furthermore, the sleepy stack approach can be applicable to single- and dual-threshold voltage technologies.

A. *Design considerations in Integrated Circuits*

A circuit is specified to operate at a particular dissipation; area of implementation and reliability issues are subjects which designer must take into account**.** However, reducing interconnect capacitance, which is another way to lower delay, reduces both power and delay. Generally, great power savings can be achieved if delay is not an issue, but optimizing power without delay consideration is insignificant delay, otherwise the entire system may not work.

B. *Why low power?*

With the continuous increase of the density and performance of integrated circuits due to the scaling down of the CMOS technology, reducing power dissipation becomes a serious problem that every circuit designer has to face.

Power dissipation limitations come in two ways. The first is related to cooling considerations when implementing high performance systems.

The second failure of high-power circuits relates to the increasing popularity of portable electronic devices. In today's technology, the main contributer to static power consumption of a CMOS circuit is subthreshold leakage. The subthreshold leakage current can be expressed as follows:

$$I_{sub} = K_1 W e^{-V_{th}/nV_\theta}(1 - e^{-V/N_\theta})$$

Where K1 and n are experimental values, W is the width of the transistor, Vth is the threshold voltage and Vθ is the thermal voltage.

C. *What is ground bounce noise?*

As signal rise times continue to increase, a phenomenon called "ground bounce" begins to be an issue. It is a source of circuit noise and signal distortion that occurs inside an IC package. How much current flows depends on, among other things, how many devices (loads) are connected to the output. The loads tend to be capacitive, so the initial current spike is not negligible. The output voltage (Vout) is measured between the output pin of the device and Ref B, which is at ground.

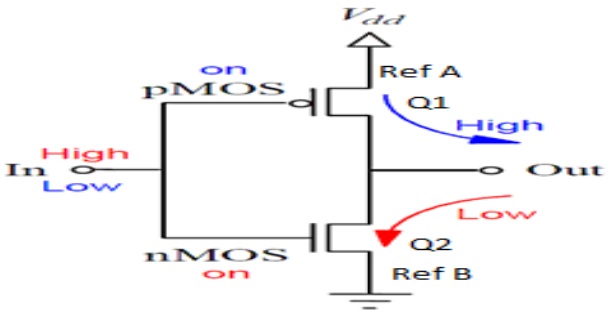

Fig1 A CMOS Inverter

II. TECHNIQUES FOR LOW POWER DESIGN

D. *Components of power consumption*

Power consumption in a static CMOS circuit basically comprises three components: dynamic switching power, short circuit power and static power. Compared to the other two components, short circuit power normally can be ignored in submicron technology.

Dynamic power is due to charging and discharging the loading capacitances. It can be expressed by the following equation

$$P_{dyn} = \frac{1}{2} C_L V_{dd}^{\ 2} . A . F$$

E. *Leakage Power*

The leakage current of a transistor is mainly the result of reverse-biased PN junction leakage, sub- threshold leakage and gate leakage as illustrated in Figure 2.

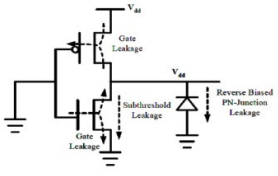

Fig2 Leakage currents in an inverter.

In submicron Technology, the reverse-

biased PN junction leakage is much smaller than sub-threshold and gate leakage and hence can be ignored. The sub-threshold leakage is the weak inversion current between source and drain of an MOS transistor when the gate voltage is less than the threshold voltage. It is given by:

$$\mathbf{I_{sub} = \mu_0 C_{ox} (W/L_{eff}) V_T^2 e^{1.8} exp ((V_{gs}-V_{th}) / nV_T) (1-exp (-V_{ds} / V_T))}$$

Due to the exponential relation between Isub and Vth, an increase in Vth sharply reduces the sub-threshold current.

Gate leakage is the oxide tunnelings current due to the low oxide thickness and the high electric field which increases the possibility that carriers tunnel through the gate oxide.

$$I_{gate} = W_{eff} L_{eff} A \left(\frac{V_{ox}}{T_{ox}}\right)^2 exp\left[\frac{-B\left(1-\left(1-\frac{V_{ox}}{\emptyset_{ox}}\right)^{\frac{3}{2}}\right)}{\frac{V_{ox}}{\emptyset_{ox}}}\right] \quad (2.3)$$

Where Vox is the potential drop across the thin oxide, Φox is the barrier height for the tunneling particle (electron or hole), and Tox is the oxide thickness. A and B are physical parameters given by,

$$A = \frac{q^3}{16\pi^2 h \emptyset_{ox}} \quad and \quad B = \frac{4\sqrt{2m}\emptyset_{ox}^{\frac{3}{2}}}{3hq}$$

Where m is the effective mass of the tunnelling particle, q is the electronic charge, and h is the reduced Plank's constant. The oxide thickness Tox decreases with the technology scaling to avoid the short channel effects.

F. Techniques for Leakage Reduction

Leakage is becoming comparable to dynamic switching power with the continuous scaling down of CMOS technology. To reduce leakage power, many techniques have been proposed, including dual-Vth, multi-Vth, body bias, transistor stacking and optimal standby input vector selection.

1) Dual-Vth Assignment

Dual-Vth assignment is an efficient technique for leakage reduction. In this method, each cell in the standard cell library has two versions, low Vth and high Vth. Gates with low Vth are fast but have high subthreshold leakage, whereas gates with high Vth are slower but have much reduced subthreshold leakage. Author affiliation must be in 10 pt Italic. Email address must be in 9 pt Courier Regular font.

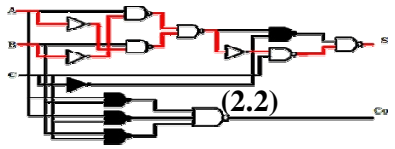

Fig3 an example dual-Vth circuit.

G. Multi-Threshold-Voltage CMOS

A Multi-Threshold-Voltage CMOS (MTCMOS) circuit is implemented by inserting high Vth transistors between the power supply voltage and the original transistors of the circuit. Figure 4 shows a schematic of a MTCMOS NAND gate. The original transistors are assigned low Vth to enhance the performance while high-Vth transistors are use d as sleep controllers.

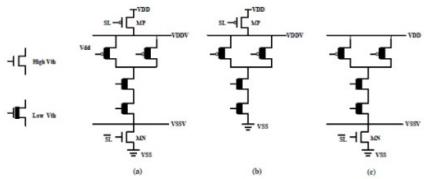

Fig4 Schematic of MTCMOS, (a) original MTCMOS, (b) PMOS Insertion MTCMOS, (c) NMOS insertion MTCMOS.

To reduce the area, power and speed overhead contributed by the sleep control high-Vth transistors, only one high-Vth transistor is needed.

2) Adaptive Body Bias

The threshold voltage of a short-channel NMOSFET can be expressed by the following equation

$$V_{th} = V_{th0} + \gamma\left(\sqrt{\emptyset_s - V_{bs}} - \sqrt{\emptyset_s}\right) - \theta_{DIBL} V_{dd} + \Delta V_{NW}$$

Equation shows that a reverse body bias leads to an increase of the threshold voltage and a forward body bias decreases the threshold voltage.

Leakage power reduction can be achieved by dynamic ally adjusting the threshold voltage

through adaptive body bias according to the different operation modes.

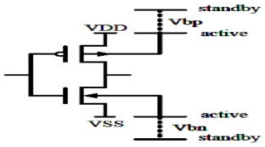

Fig5 Scheme of an adaptive body biased inverter.

3) *Transistor Stacking*

The two serially-connected devices in the off state have significantly lower leakage current than a single off device. This is called the stacking effect.

With transistor stacking, by replacing one single off transistor with a stack of serially-connected off transistors, leakage can be significantly reduced. Such a stack of transistors causes either performance degradation or more dynamic power consumption.

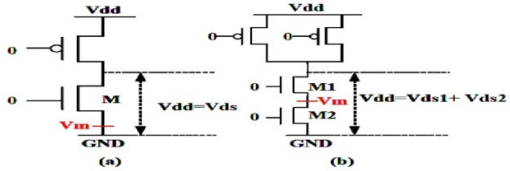

Fig6 Comparison of leakage for (a) one single off transistor in an inverter (b)Two serially-connected off transistors in a 2-input NAND gate.

III. DESIGN OF CMOS FULL ADDER CIRCUIT

H. *Conventional CMOS full adder*

A binary full adder is a three-input and two-output combinational circuit. Considering that A and B are the input bits to be added, C is the carry input, SUM is the sum output and CARRY is the carry output, the truth table of the full-adder cell is shown in Table 1. Following Boolean functions that the full-adder circuit is to perform can be figured out from Table 1.

$$SUM = A \oplus B \oplus C$$

$$= ABC + A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C}$$

$$CARRY = AB + AC + BC$$

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table1. Truth table for full adder circuit

Recently, power dissipation has become an important concern and considerable emphasis is placed on understanding the sources of power and approaches to dealing with power dissipation.

The following figure shows the conventional CMOS 28 transistor adder. This is considered as a Base case throughout this paper. All comparisons are done with Base case. The CMOS structure combines PMOS pull up and NMOS pull down networks to produce considered outputs.

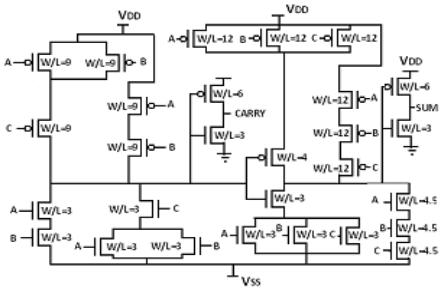

Fig7 Conventional CMOS full adder

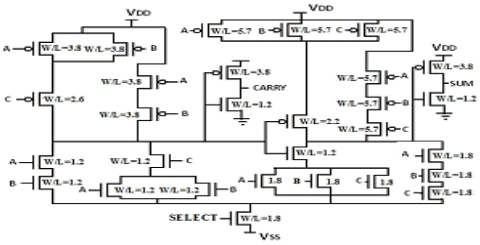

Fig8 Full adder (Design1) circuit with sleep transistor.

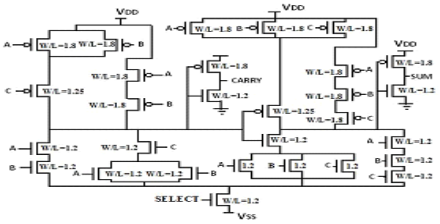

Fig9 full adder (design2) circuit using sleep transistor

Since addition forms the basis of many binary operations, adder circuits are of great interest in digital design. As the most frequently used block in the overall design is full-adder, now we turn our attention to build an efficient full-adder circuit using various techniques like Sleep method and Dual stack method. The simulated results of full adder circuit using sleep method and full adder circuit using dual stack method show that these methods are able to reduce the power dissipation more effectively when compared with the basic full adder circuit and design-1 and design-2 full adder circuits. Since, each circuit has got its own advantage and disadvantage in power dissipation and area depending up on the requirement of the designer either of the methods is used.

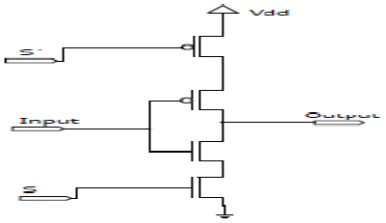

Fig10 Basic Inverter circuit using Sleep Method

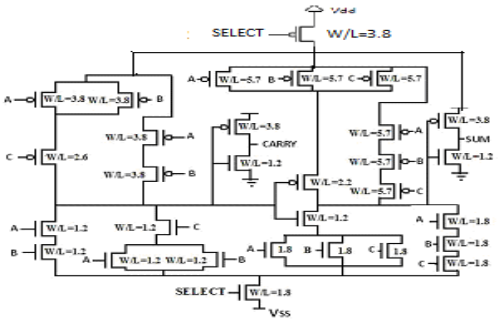

Fig11 Full Adder circuit using sleep method

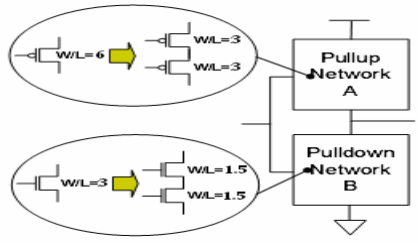

Fig12 Stack approach

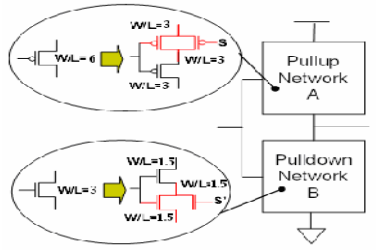

Fig 13 Sleepy Stack approach

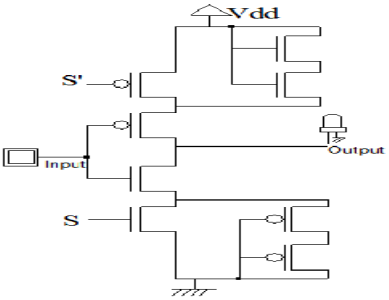

Fig14 Dual Stack approach

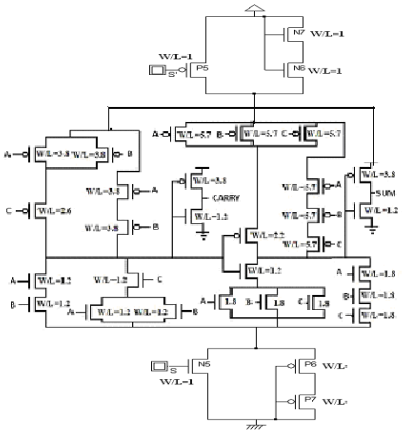

Fig15 Full adder circuit using Dual stack approach

IV. SCHEMATIC DESIGN AND SIMULATION RESULTS OF FULL ADDER CIRCUIT

I. Schematic design for Basic full adder circuit

A schematic view of a basic 1-bit full adder is shown in the figure 16. The layout and simulated input and output waveforms are shown in the figure 17 and 18 respectively.

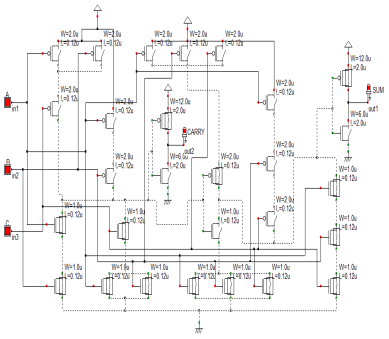

Fig16 Digital schematic design for basic full adder circuit

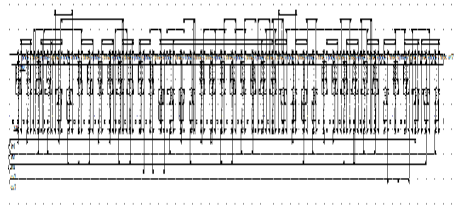

Fig17 Layout for basic full adder circuit

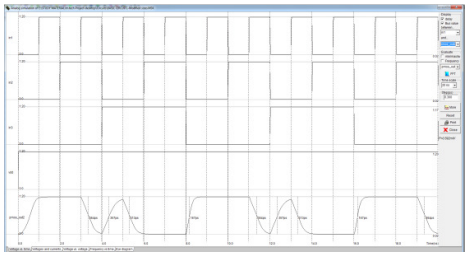

Fig18 Simulation results for basic full adder circuit

J. *Schematic design for Design-1 circuit*

A schematic view of a design-1 full adder is shown in the figure 19. The layout and simulated input and output waveforms are shown in the figure 20 and 21 respectively.

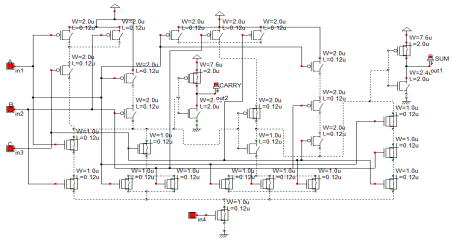

Fig19 Digital schematic design for design-1 full adder circuit

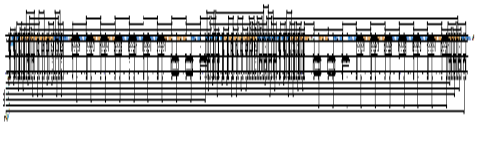

Fig20 Layout for design-1 full adder circuit

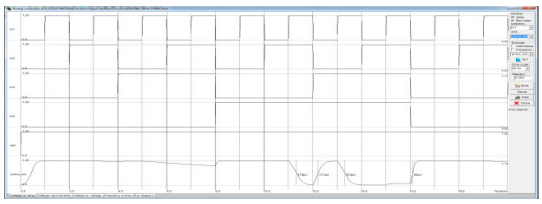

Fig21Simulation results for design-1 full adder circuit

K. *Schematic design for Design-2 circuit*

A schematic view of a design-2 full adder is shown in the figure 22. The layout and simulated input and output waveforms are shown in the figure 23 and 24 respectively.

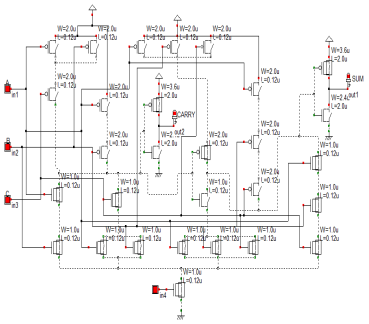

Fig22 Digital schematic design for design-2 full adder circuit

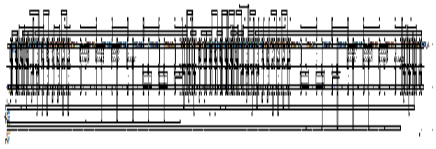

Fig23 Layout for design-2 full adder circuit

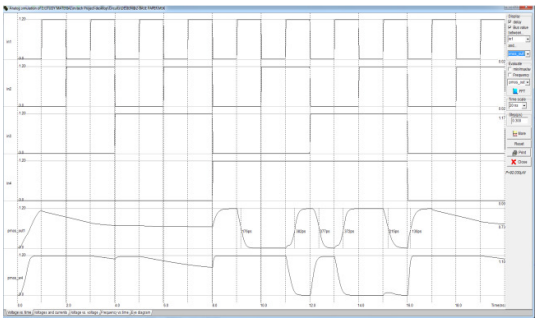

Fig24 Simulation results for design-2 full adder circuit

L. *Schematic design for Sleep method circuit*

A schematic view of a full adder circuit using sleep method is shown in the figure 25.The

layout and simulated input and output waveforms are shown in the figure 26 and 27 respectively.

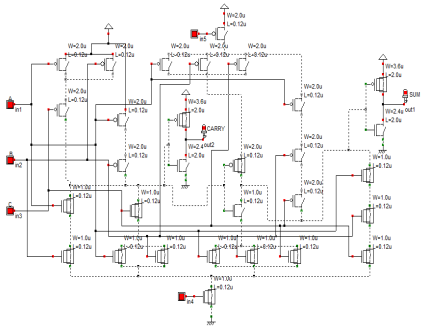

Fig25 Digital schematic design for full adder circuit using sleep method

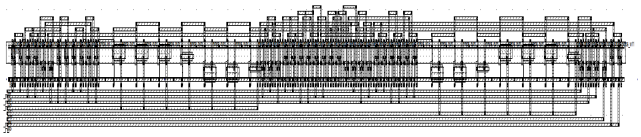

Fig26 Layout for full adder circuit using sleep method

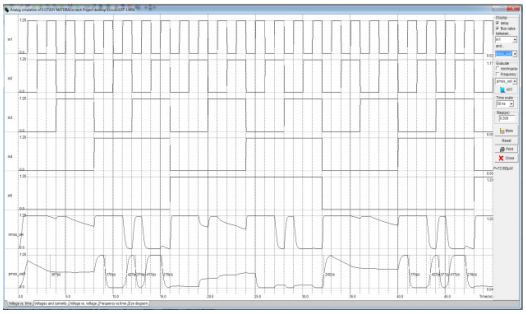

Fig27 Simulation results for full adder circuit using sleep method

M. Schematic design for Dual-Stack method circuit

A schematic view of a full adder circuit using dual-stack method is shown in the figure28.

The layout and simulated input and output waveforms are shown in figure 29 and 30 respectively.

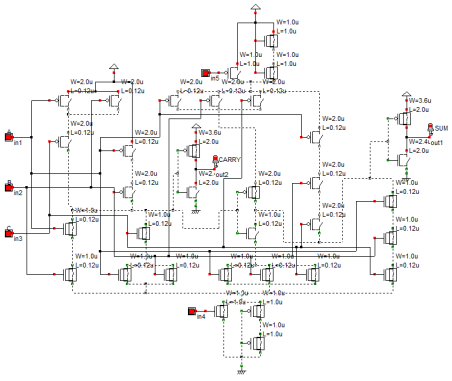

Fig28 Digital schematic design for full adder circuit using dual-stack method

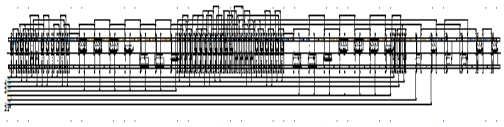

Fig29 Layout for full adder circuit using dual-stack method

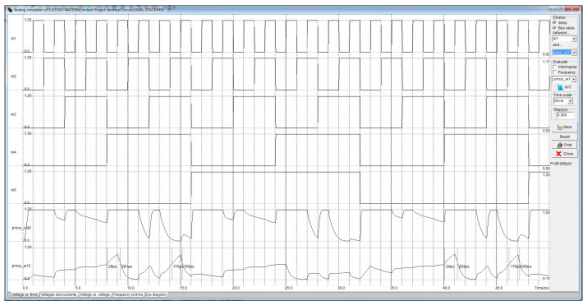

Fig30 Simulation results for full adder circuit using dual-stack method

V.CONCLUSION

In this thesis, low leakage 1 bit full adder cells are proposed for mobile applications with low leakage power. By using the proposed technique leakage power is reduced by 33% (Design1), 46% (Design2) in comparison to the conventional adder cell (Base case). By using the novel techniques of sleep method and dual-stack method leakage power is further reduced when compared with the basic circuit, design-1 and design-2 circuits. In this thesis, we have presented different ways to reduce the leakage power of one-bit full adder circuits.

One-bit full adder circuit is considered as two cascaded blocks i.e. carry generation block and sum generation block. Separate sleep transistors are added at the bottom of the blocks.

To summarize, since full adder circuits are designed in five different methods, each with its own advantages and disadvantages of power, area, etc,. can be used depending up on the requirement of the designer.

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