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# DESIGN OF LOW POWER DIGITALLY OPERATED VOLTAGE REGULATOR BY USING CMOS TECHNOLOGY

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**Abstract**.- As portable electronic devices become a part of daily life, it creates a huge market for electronic components for those battery driven devices. Low-power digitally operated (LPDO) voltage regulator is an important part that provides steady DC supplies for other components. Low power, low noise and high stability are the desired features of a regulator.
Here, A Low-Power Digitally Operated (LPDO) Voltage Regulator that can operate with a very small Input-output Differential Voltage with 32nm CMOS technology has been proposed. It increases the Packing Density and provides the new approach towards power management.
A voltage regulator is capable of providing 0.8V output under the supply voltage of 1.2V and the output voltage level is controlled externally by means of 2 1-bit control signals.

***Keywords***: Low Drop-Out, Voltage Regulator, Power management, Reduction in chip Area.

## 1. INTRODUCTION

A programmable Low power digitally operated voltage regulator has become an essential part of portable electronic devices that provide steady DC supplies for other components. LPDO operates over a very small input output differential voltage. In this, voltage regulator capable of providing 0.8v output has been proposed. where low power dissipation, low noise and high efficiency are the desired characteristics.

Voltage regulators can be divided into two main categories: Linear Voltage Regulators (LVR) and Switching Mode Power Converters (SMPC). SMPC is restricted in the use of portable electronic devices, because of its high cost, high output voltage ripple and noise. whereas, LVR shows the characteristics of very small output voltage ripple, compactness, and low output noise. Low power digitally operated Voltage (LPDO) Regulator presents the lowest dropout voltage and highest power efficiency. However, frequency response of the LPDO system highly depends on load conditions.

Low power digitally operated voltage regulators are the circuit, design to provide a specified stable DC voltage, with low input to output voltage difference. Dropout voltage of regulator is the value of differential voltage at which regulation provided by control loop stops. Minimization of dropout voltages is essential for maximizing dynamic range of PMOS circuit. The low drop out voltage regulator is programmable and offers a range of four different voltages by means of two binary input control signals at its input. The entire circuit has been design by using 32nm CMOS technology by using the Microwind 3.1 tool.

## SCOPE OF WORK

The objective of this project is to enhance performance of low power digitally operated voltage regulators for battery powered electronics. a low power digitally operated (LPDO) voltage regulator can operate with a very small input–output differential voltage with 32nm CMOS technology. It provides new approach towards power management.

## I. LOW POWER DIGITALLY OPERATED VOLTAGE REGULATOR

The supply voltage of a system-on-chip (SOC) is generally generated from an external supply voltage. In this block diagram, the external supply voltage level is converted to another level with a switching DC-DC converter to obtain a high power efficiency. But at the output of DC-DC convertor we get large ripple. Hence to avoid this ripple noise LDO regulator is inserted in the circuit and output of LDO regulator is given to the load.

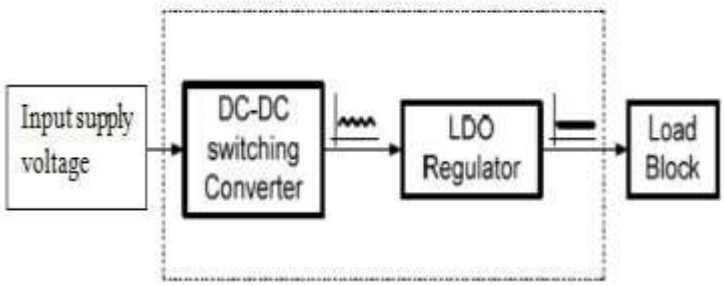


**Fig. 1: General block diagram of a LDO with a load**

## II. SPECIFICATIONS OF LPDO VOLTAGE

### 1. REGULATION

Low power digitally operated (LPDO) voltage regulators work in the same way as all linear voltage regulators. The main difference between LPDO and non-LPDO regulators is their schematic topology. Instead of an emitter follower topology, a low-dropout regulator uses open collector or open drain topology. This enables transistor into saturation region. If a bipolar transistor is used, additional power may be lost to control it, whereas non-LPDO regulators take that power from voltage drop itself. Power FETs may be preferable to reduce power consumption, but this FET's may give problems when the regulator is used for low input voltage, as FETs generally require 5 to 10V to close completely. And It can also increase the cost of a design.

### 2. PROPOSED REGULATOR ARCHITECTURE

In this, we are proposing LPDO voltage regulator which will be as compact as possible. The 32nm CMOS technology will provide new approach towards power management. In our architecture, a current-sourcing PMOS in the output stage has been introduced. It is required that the PMOS get pulled to ground so as it get further biased into saturation region. For this reason, the present topology is modified and a common source stage is added. The common-source stage is responsible for enhancing signal swing and boosting. The two gate inputs provided to the proposed LPDO architecture will make the device programmable. Two bit binary values are given to the gate inputs. The variation of the output with respect to these inputs will be as depicted in the following table.

| BINARY INPUT | OUTPUT VOLTAGE (V) |
|---|---|
| 00 | 0.7V to 0.8V |
| 01 | 0.6V to 0.7V |
| 10 | 0.6V to 0.7V |
| 11 | 0.8V |

Table 1: Variation in input and output

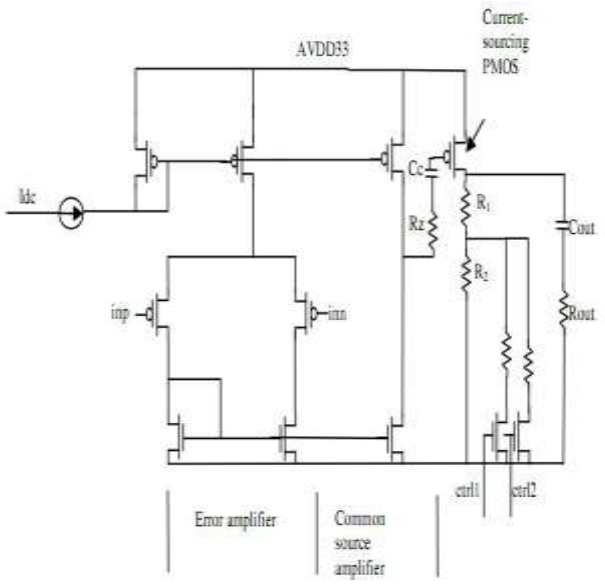


Fig 2: Circuit diagram of proposed regulator

The proposed architecture divided in three different stages:

1. Error Amplifier

2. Common Source Amplifier

3. Current-sourcing PMOS

**1. ERROR AMPLIFIER**

In this, A high gain operational amplifier is used as the error amplifier, with a stable voltage reference is given as a input to the amplifier. The voltage reference is usually obtained from a band gap reference circuit. It provides load which has the advantage of providing high output impedance and consequently high gain.

**2. COMMON-SOURCE AMPLIFIER**

In general, a source follower is used as the buffer stage in most LPDO's. The source follower has asymmetric current driving capability, and it provides gain less than one. Hence a common-source amplifier is used, which has a small signal gain equal to

$$Av=gm(ro1||\ ro2)$$

where gm is the transconductance of the amplifying device, ro1 and ro2 are the output resistances of the load and the amplifying device.

**3. CURRENT-SOURCING PMOS**

The current-sourcing PMOS is responsible for quick
charging and discharging of output node. In this, PMOS with high thresholds voltage is used. Because, low-voltage threashold FET's are known to contribute to leakage currents, and increases the power dissipiation in the device.
The schematic view of proposed regulator architecture is given below.

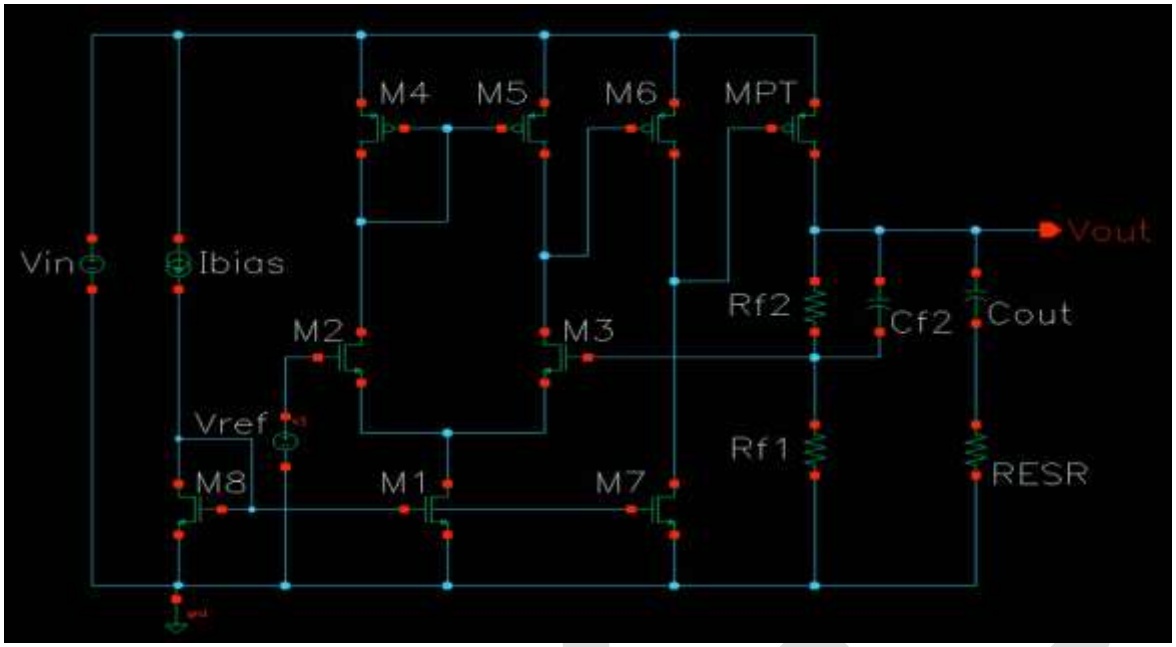


Fig. Schematic views of proposed LPDO regulator

On the basis of this schematic view of LPDO voltage regulator, the proposed regulator is designed by using 32nm technology in vlsi. this design is given as below.

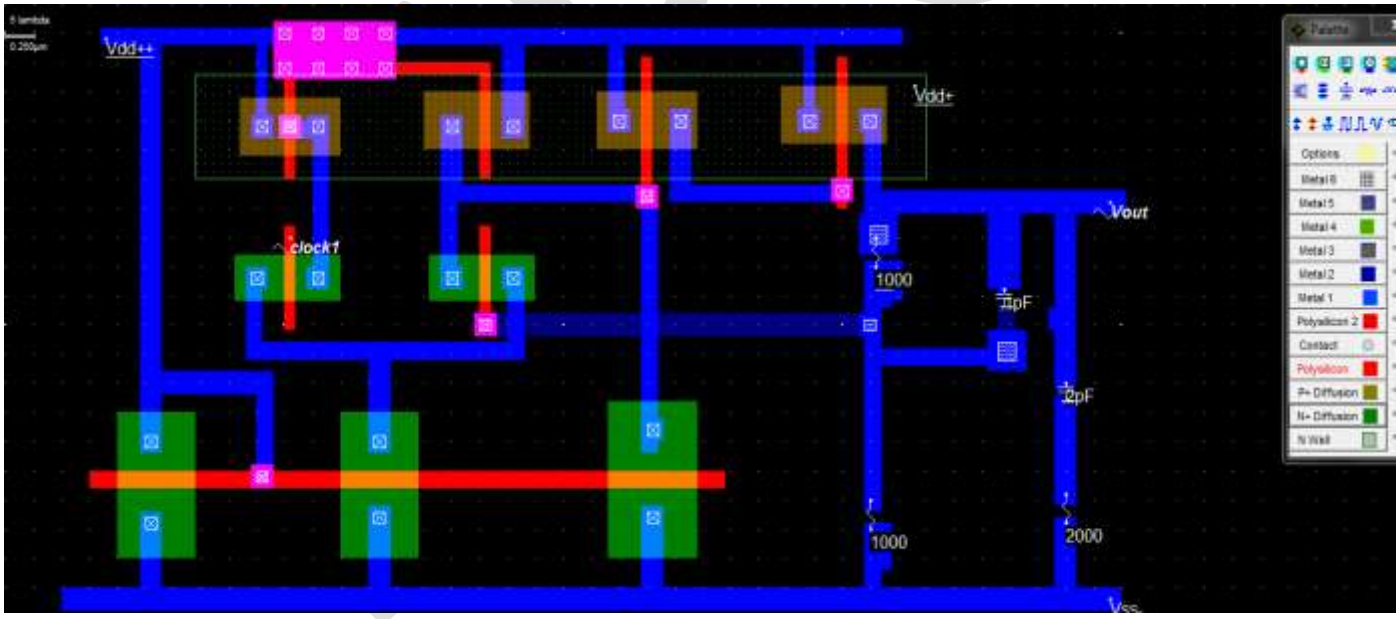


Fig. VLSI design of proposed LPDO regulator.

The design specification of that proposed LPDO is:

| | |
|---|---|
| CMOS Technology | 32nm |
| Power supply voltage | 0.35v,1.20v |

| | |
|---|---|
| Area of complete chip | 8.2um2 |
| Width of complete layout | 4.4um |
| Height of Layout | 2.0um |
| No of PMOS | 3 |
| No of NMOS | 5 |

After simulation of that LPDO design, we get the voltage waveform which is as follows.

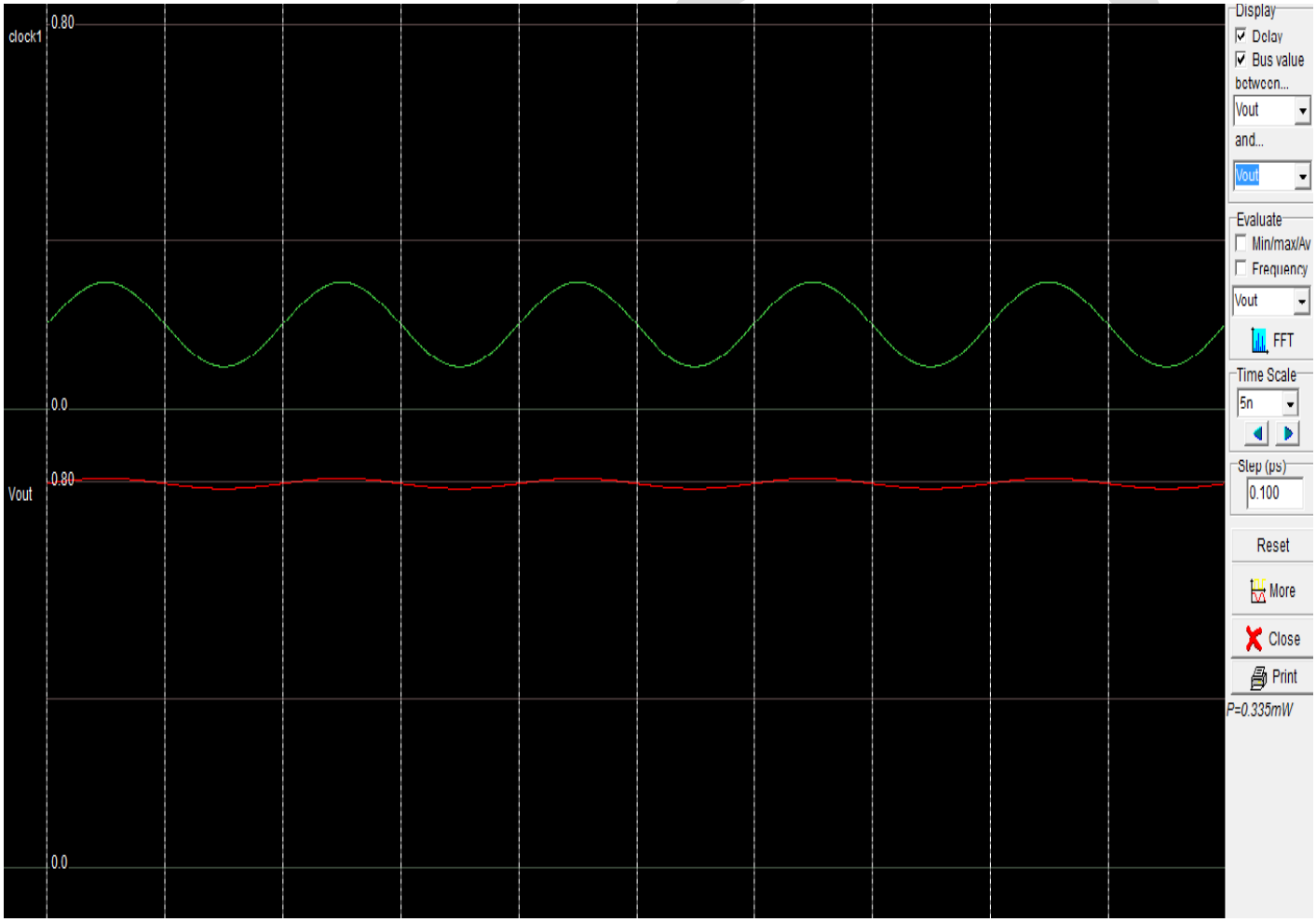


Fig. Output waveform of LPDO regulator

As shown in above waveform, we get the 0.8v voltage at the output end for the given input of 1.2v.

As, different devices required different voltage levels .for that reason, we decide to make our device programmable at the output. In that case, the output voltage level is control externally by using 2 1-bit control signals and we will get 4 different voltage levels.

## 2. LITERATURE REVIEW

From the rigorous review of related work and published literature, it is observed that many researchers have designed Low Power Digitally Operated Voltage Regulator by applying different techniques.

Gabriel Alfonso Rincon-Mora and Philip E. Allen,[1] was studied and designed a low drop out voltage regulators, and published a paper, which discusses thoroughly the important issues relevant to the design of a LDO circuits. The paper further illustrates the design criteria corresponding analysis relevant to LDOs.

R. Jacob Baker, Stuart K. Tewksbury and Joe E. Brewer,[2] had worked on CMOS Circuit Design, Layout and Simulation.

Vincent Lixiang Bu[3] had worked and studied the CMOS Capacitor less Low Drop-Out Voltage Regulator. In this paper, a 3-5V 50mA CMOS low Drop-out (LDO) linear regulator with a single capacitor of 1pF is presented.

Robert J. Milliken, Jose Silva-Martínez,[4] had studied and presented a paper on Full On-Chip CMOS Low Drop Voltage Regulator. This paper proposes a solution to the bulky external capacitor low-dropout (LDO) voltage regulators with an external capacitor less LDO architecture.

Xinquan Lai And Donglai Xu[5] had studied An Improved CMOS Error Amplifier Design for LDO Regulators in Communication Applications. In this paper, A new CMOS error amplifier, which is primarily used in LDO regulators for communication applications, was presented.

## 4. PROBLEM DEFINATION

### CONVENTIONAL LDO BLOCK DIAGRAM

Low-drop out regulators is one of the most conventional applications of operational amplifiers. Figure3 shows the basic topology. A voltage reference is used with the op-amp to generate a regulated voltage Vreg. and the variation in the gain is desensitized using feedback and makes the regulated voltage stable. The ideal voltage regulator is as shown below.

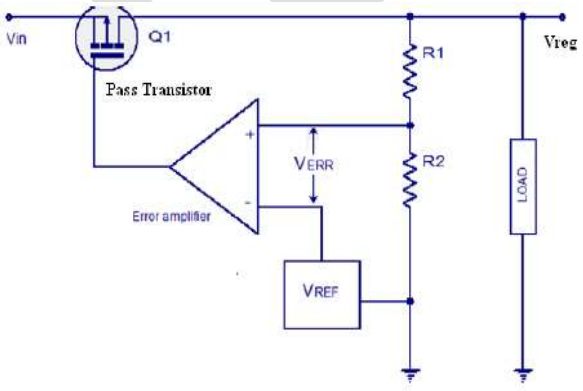


Fig. 3: Conventional LDO

## 4. RESEARCH METHODOLOGY

To achieve the low drop out regulator, different methodology and techniques can be used for design. The program MICROWIND3.1 allows designing and simulating an integrated circuit at physical description level. It contains a library of analog ICs, metals and different logic to view and simulate the circuit. MICROWIND 3.1 includes all the commands as well as required tools which never present before in a single module. We can simulate the circuit only by pressing single key. The simulation of circuit is automatically performed and it produces voltage and current curves immediately. considering the advancement of future technology and the advantage of 32nm technologies over 90 and 65nm technology, the proposed project has been decided to do with the selection of lower order of nm technology. The proposed LPDO is designed using 32 nm CMOS/VLSI technology in MICROWIND 3.1.

32 nm CMOS technology has advantages as:

- Increase in switching performance
- Reduction in power management
- It gives 2 times higher density
- Reduction in leakage current
- Minimize the area of a chip

## 5. IMPLICATIONS

We have designed a low power digitally operated voltage regulator that is capable of providing a very small output of 0.8v. this is the 50% of our total work. now, further we will make this voltage regulator programmable..The design provides a 30 dB gain. In this, input is given nearly 1.2v and the output we get 0.8v. total circuit is design by using MICROWIND 3.1 CMOS technology.

## REFERENCES:

[1] “Study and Design of Low Drop-Out Regulators” by Gabriel Alfonso Rincon- Mora and Philip E. Allen, Department of Electrical and Computer Engineering, Georgia Institute of Technology.

[2] “CMOS Circuit Design, Layout and Simulation” by R. Jacob Baker, *IEEE Press Series on Microelectronic Systems*, Stuart K. Tewksbury and Joe E. Brewer, Series Editors.

[3] “A CMOS Capacitorless Low Drop-Out Voltage Regulator” by Vincent Lixiang Bu, Department of Electrical and Computer Engineering, Tufts University.

[4] “Full On-Chip CMOS Low Drop Voltage Regulator” by Robert J. Milliken, Jose Silva-Martínez, Senior Member, *IEEE, and Edgar Sánchez-Sinencio, Fellow, IEEE.*

[5] “An Improved CMOS Error Amplifier Design for LDO Regulators in Communication Applications” by Xinquan Lai, Institute of Electronic CAD and Donglai Xu, School of Science and Technology.

[6] “Design of Analog CMOS Integrated Circuits” by Behzad Razavi