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Power Reduction in Row Address Circuitry of SRAM Design

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Abstract— SRAM memories are used in high speed computers and embedded applications. They are used as register and cache memory of processor. SRAMs operating frequency is compatible with modern processor speed because they are fabricated in CMOS technology. So demand of SRAM memory will remain high in coming years. So there efficient design and fabrication has large scope in current and near future market. The sources of SRAM power are the sum of the power consumed by decoders, memory array, write drivers, Sense amplifiers, and I/O line drivers. This paper is mainly focuses on the development of power efficient SRAM structure. The paper describes the comparison of different decoder circuitries and optimized design of decoder with word line driver while driving large capacitive loads for minimizing power dissipation across load. The comparison has been designed and simulated using Cadence Virtuoso Spectre in 180 nm technology.

Keywords— SRAM, CMOS taper buffer, Decoders, Leakage power, Power dissipation, Tapering factor, SRAM Peripheral circuit

INTRODUCTION

In computers data (information) and program (sequence of commands) are store in some physical devices on permanent or temporary basis. This stored content is used in other computing or on time computing depends on the application. For large data which may need to access in future on permanent basis for that magnetic storage is used. Run time data is stored in semiconductor memories. Computer memories are mainly divided into two parts: Primary memory and Secondary Memory. Semiconductor memories come under primary storage. SRAM is random access memory that means its content can be access from anywhere of storage memory. Data are stored in cells and to access data randomly, fix address is assign to all locations of storage cell. SRAMs are volatile in nature that means their storage data will loss after power shutdown. Therefore they can be used to store run time data in computer systems. SRAM is used as register and cache memory to make faster program execution in computer system. SRAMs are made by using same sources as for process made therefore they are compatible with processor in all extent and their speed is matched with current processor speed. SRAM cell are made up with cross couple inverter latch having positive feedback loop therefore during write operation it store data rapidly.

CMOS technology scaling has been a primary driving force to increase the processor performance. A drawback of this trend lies in a continuing increase in leakage power dissipation .Recent results have shown that leakage in SRAM peripheral circuits, such as word line drivers as well as input and output drivers are now the main sources of leakage[1]. A CMOS Tapered buffer is used to increase the driving ability of the logic circuitry; it is connected with large capacitive load. These are used between logic gate and large capacitive load to increase its drain current strength. These circuits are required which can drive the load at high speed while not degrading the performance of previous stages in the chain of inverters [2].These buffers are used in the memory access path as word line drivers, which is place in the output stage of decoder section.

In brief, two main reasons explain this difference in leakage.

- Memory cells are designed with minimum-sized transistors mainly for area considerations. Unlike memory cells, periphery circuits use larger, faster and accordingly, more leaky transistors so as to satisfy timing requirements
- Memory cells use high threshold voltage transistors, which have a significantly lower leakage reduction compared with typical threshold voltage transistors used in peripheral circuits.

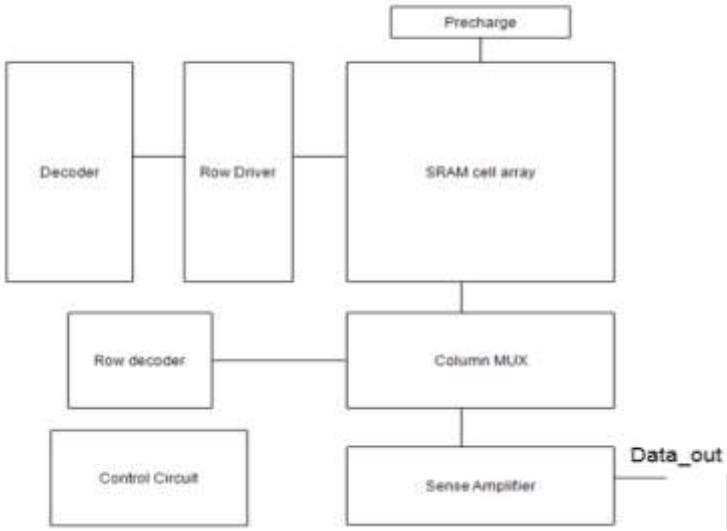

Fig 1: Block diagram of SRAM memory array

Address Decoder is an important digital block in SRAM which takes up to 50% of the total chip access time and notable amount of the total SRAM power in normal read/write cycle. Due to large amount of storage cells in memories it can be found various solutions of address decoder designs leading to power consumption reduction and performance improvement.
The focus of this paper is, therefore, reduction of power dissipation across load of SRAM memory array. This paper explores the comparison of different decoder circuits. And also compares the combination of decoder section with word line driver which act as buffers while driving large capacitive load.

Results from the literature survey

TABLE 1: COMPARISON OF DECODER CIRCUITS

Type of decoder	**Average power(µW)**
Conventional 2:4 decoder	39.22
Dynamic NAND 2:4 decoder	15.53

Topology's	**Technology**	**Power dissipation(Watts)**	**Propagation delay**
Conventional static CMOS inverter[3]	180-nm	14.44uw	-
Sleepy inverter chain[4]	180-nm	151.03nw	-
Sleepy inverter chain with state retention buffer[4]	180-nm	150.12nw	-
Zig zag sleep buffer[5]	180-nm	7.088µw	-
Two stage taper buffer with feedback network[6]	180-nm	15.97% ↓	4.703% ↑
Four stage Tapered Vth (constant) CMOS inverter buffer[7]	65-nm ,1.08V	39% ↓	4% ↑
1. Four stage Tapered Vth(varying) CMOS inverter buffer[8]	45-nm ,1-V	61% ↓	10% ↑
Four stage taper buffer with feedback network[6]	180-nm	13.11% ↓	7.213% ↑
Four stage Taper buffer with bypass [9]	65-nm	19.02% ↓	6.63% ↓

TABLE 2: COMPARISON OF EXISTING BUFFER TOPOLOGIES

From the survey we can see that, taper buffer with bypass circuits have low power and lower propagation delay compared to all other topologies. By combining best word line driver with power efficient decoder circuit which is dynamic NAND while driving large capacitive load.

DESIGN METHODOLOGY

TABLE 3: WORD LINE DRIVERS DESIGN REQUIREMENTS

Technology	180nm
V_{DD}	3.3V
Tapering factor	4.55
No: of stages	4
Capacitive load	295.8

CIRCUIT DIAGRAMS

Figure below shows the combination of dynamic NAND decoder with conventional taper buffer and the transient analysis

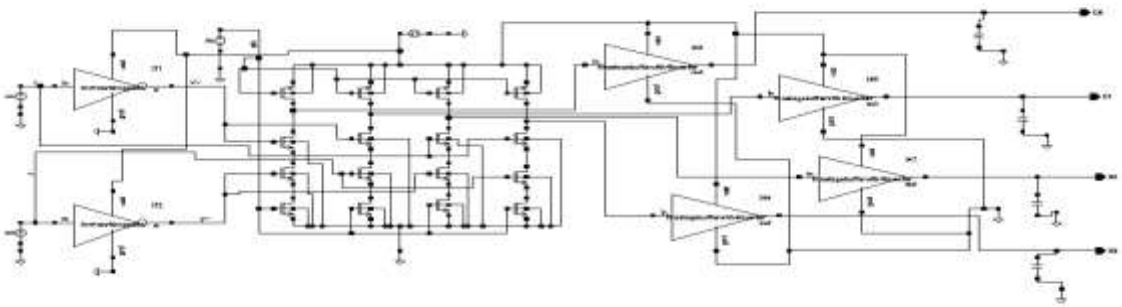

Fig 2: Integration of Dynamic NAND 2:4 decoder with conventional four stage taper buffer circuit

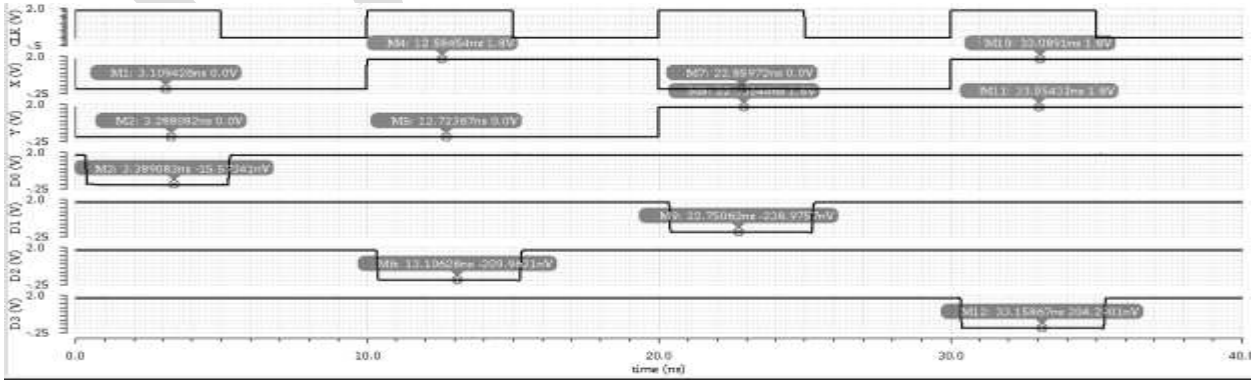

Fig 3: Transient analysis for dynamic NAND 2:4 decoder with conventional four stage taper buffer

Figure below shows the combination of dynamic NAND decoder with bypass buffer and the transient analysis

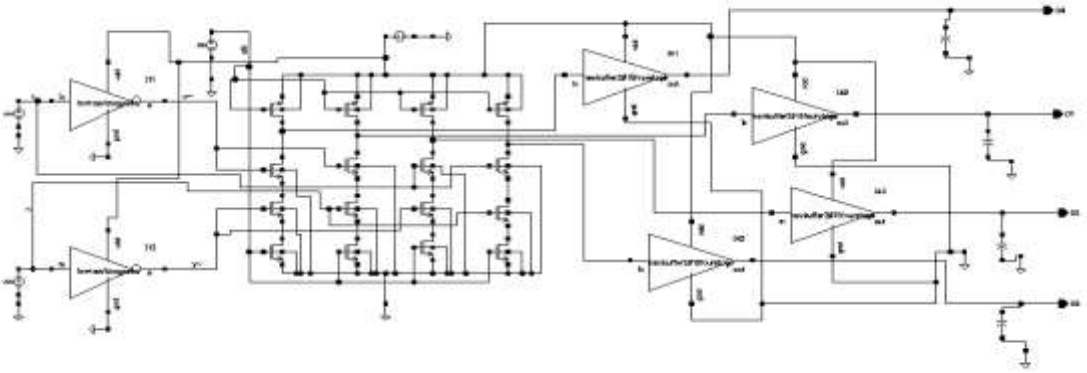

Fig 4: Integration of dynamic NAND 2:4 decoder with four stage CMOS taper with bypass buffer

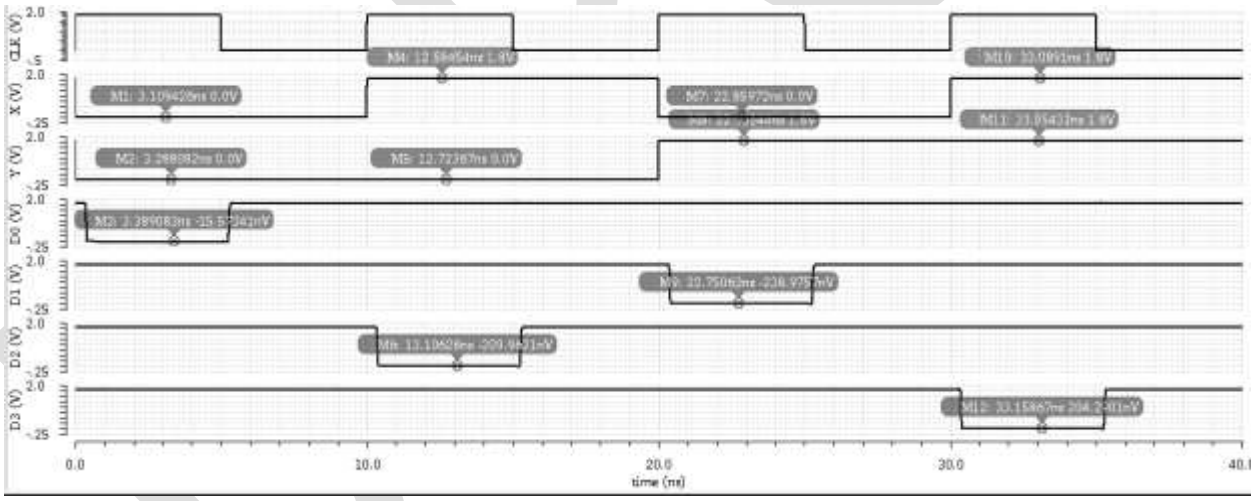

Fig 5: Transient analysis for dynamic NAND 2:4 decoder with four stage CMOS taper bypass buffer

EXPERIMENTAL RESULTS

TABLE 4: COMPARISON RESULTS

TOPOLOGYS	POWER DISSIPATION ACROSS LOAD (nW) 00	01	10	11
Dynamic NAND 2:4 decoder with conventional four stage buffer	C1=287.1	C2=224.1	C3=244.7	C4=179.2
Dynamic NAND 2:4 decoder with four stage CMOS tapper bypass buffer	C1=107.2	C2=139.4	C3=221.7	C4=124.5

From the experimental results it can be concluded that, the power dissipation across load while selecting the address of particular SRAM array location is reduced when using the combination of bypass circuit buffer and dynamic NAND decoder.

CONCLUSION

Periphery circuits are important components of SRAM memory and the performance of SRAM depends on these components. Leakage power dissipation of on-chip SRAM constitutes a significant amount of the total chip power consumption in microprocessors and System on chips. In this paper two types of decoders are designed and analyzed for optimum power dissipation across load during the design of SRAM memory architecture. The power dissipation across load can be reduced by combining dynamic decoder circuits with bypass buffer. The comparison has been designed and simulated using Cadence Virtuoso Spectre in 180 nm technology.

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