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Short Channel Effects in Conventional MOSFETs and their Suppression

Anu Tonk
Ph.D Student, Department of Electronics and Communication Engineering,
F/O Engineering and Technology
Jamia Millia Islamia, New Delhi
tonkanu.saroha@gmail.com

Abstract— The paper discusses short channel effects (SCEs), a major issue faced by the nano-scale devices and as a result of which the device performance degrades. As indicated by the Moore's law the number of transistors inside the chip doubles every two years mainly attributed to downscaling of the MOSFET size. As the channel length is reduced, departures from the long channel behavior occur. These departures, which are called Short Channel Effects, arise as the results of a two-dimensional potential distribution and high electric fields in the channel region. The phenomenon of Charge sharing, Sub-surface punch through and DIBL in conventional MOSFETs along with some important remedies have been discussed in the paper.

Keywords— Charge Sharing, Sub-Surface Punchthrough , DIBL, High-K dielectrics, Pocket Implants, SOI

INTRODUCTION

For a given channel doping concentration when the channel length is reduced the depletion layer widths of source and drain junctions become comparable to channel length. The potential distribution in the channel now depends on both the transverse field Ex (controlled by the gate voltage and back-surface bias) and the longitudinal field Ey (controlled by the drain bias). In other words, the potential distribution becomes two dimensional, and the gradual channel approximation (i.e. Ex >> Ey) is no longer valid.

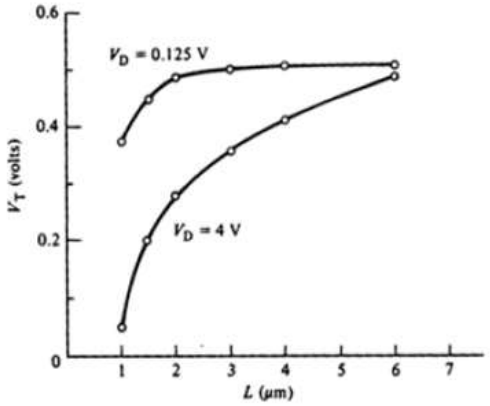

Fig 1: Threshold voltage (V_T) decreases with the decrease in channel length (L) [1]

This two dimensional potential results in degradation of the threshold behavior and dependence of threshold voltage on the channel length & biasing voltages. This can be understood with the help of Fig 1. The threshold voltage decreases with the decrease in the technology [2] (L: channel length) or scaling [8]. This is highly undesirable because circuit designers would like V_T to be invariant with transistor dimensions and biasing conditions [9].

SHORT CHANNEL EFFECTS: The short-channel effects are attributed to two physical phenomena:

- The limitation imposed on electron drift characteristics in the channel,
- The modification of the threshold voltage due to the shortening channel length.

Following are some distinguished SCEs:

1. Charge sharing: In Long channel devices, the influence of source-drain regions is negligible since the source and drain regions form small fraction of the channel region [5]-[7]. For small channel devices, the source-drain ends up taking a

large portion of the depletion region and consequently shares a major portion of this body effect. We therefore usually identify this effect as "charge sharing". In charge sharing, the area and charge under the gate is reduced and hence the threshold voltage.

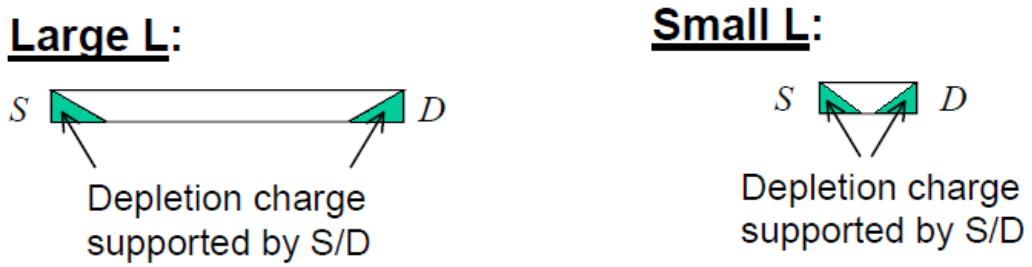

Fig 2: Charge Sharing in long channel and short channel MOSFETs.

2. Sub-Surface Punchthrough

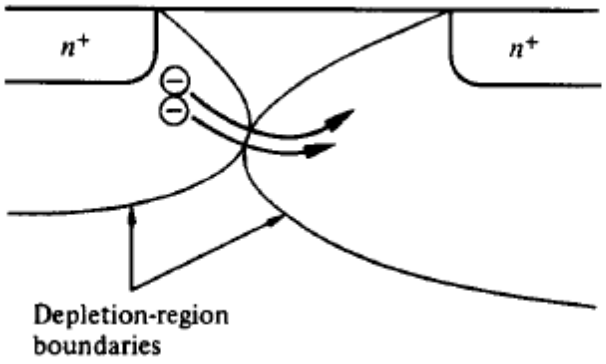

Fig 3: Sub-surface punchthrough

When the drain is at high enough voltage with respect to the source, the depletion region around the drain may extend to the source, causing current to flow irrespective of gate voltage (i.e. even if gate voltage is zero). This is known as Sub-surface Punchthrough as it takes place away from the gate oxide and substrate interface. So when channel length L decreases (i.e. short channel length case), punch through voltage rapidly decreases. In short-channel devices, due to the proximity of the drain and the source, the depletion regions at the drain-substrate and source-substrate junctions extend into the channel. As the channel length is reduced, if the doping is kept constant, the separation between the depletion region boundaries decreases. An increase in the reverse bias across the junctions also pushes the junctions nearer to each other. When the combination of channel length and reverse bias leads to the merging of the depletion regions, punchthrough is said to have occurred.

3. DIBL: There exists a potential barrier between source and drain which is to be lowered by applying gate voltage. In short channel devices in addition to the gate voltage, drain voltage also has a significant effect on reducing this barrier. As

the source & drain get closer, they become electrostatically coupled, so that the drain bias can affect the potential barrier to carrier flow at the source junction. As a result, subthreshold current increases. As the drain depletion region continues to increase with the bias, it can actually interact with the source to channel junction and hence lowers the potential barrier. This problem is known as Drain Induced Barrier Lowering (DIBL) [10]. When the source junction barrier is reduced, electrons are easily injected into the channel and the gate voltage has no longer any control over the drain current. In long-channel devices, the source and drain are separated far enough that their depletion regions have no effect on the potential or field pattern in most part of the device. Hence, for such devices, the threshold voltage is virtually independent of the channel length and drain bias. DIBL is enhanced at high drain voltages and shorter channel lengths.

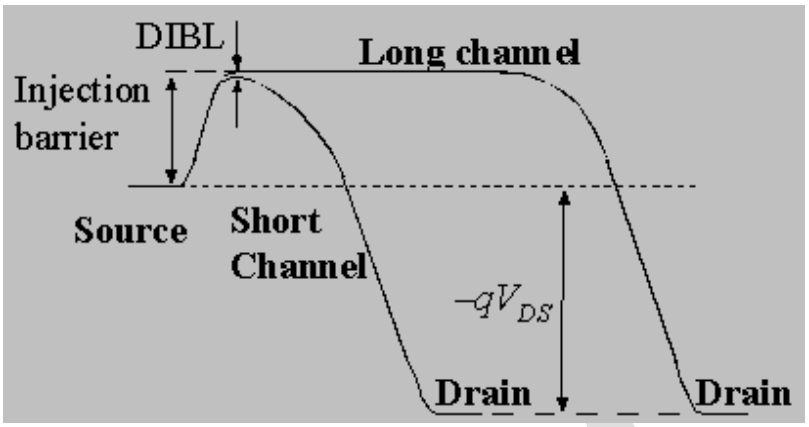

Fig 4: Drain-Induced Barrier Lowering (DIBL)

Remedies [4]:

1. High K dielectric [12]: "High-k" stands for high dielectric constant, a measure of how much charge a material can hold. Different materials similarly have different abilities to hold charge. The higher "K" increases the transistor capacitance so that the transistor can switch properly between "ON" and "OFF" states, with very low current when OFF yet very high current when ON. Because high-k gate dielectrics can be several times thicker, they reduce gate leakage by over 100 times. As a result, these devices run cooler. Replacing the silicon dioxide gate dielectric with a high-k material allows increased gate capacitance without the increasing leakage effects.

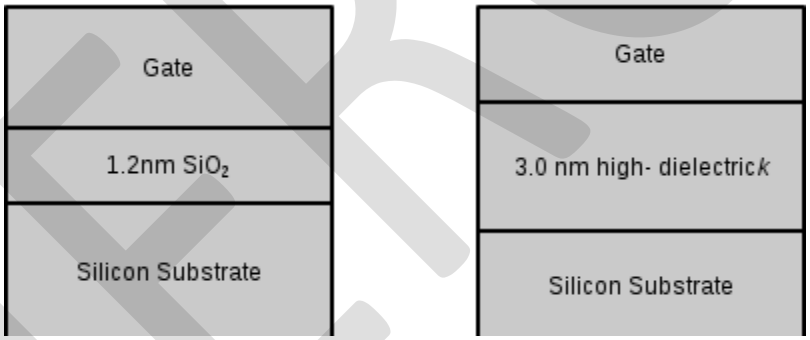

Fig 5: High-K dielectrics

2. Pocket Implants: In submicrometer MOSFETs, an adjust implant is used to have a higher doping at the surface than that in the bulk. This causes a greater expansion of the depletion region below the surface (due to smaller doping there) as compared to the surface.

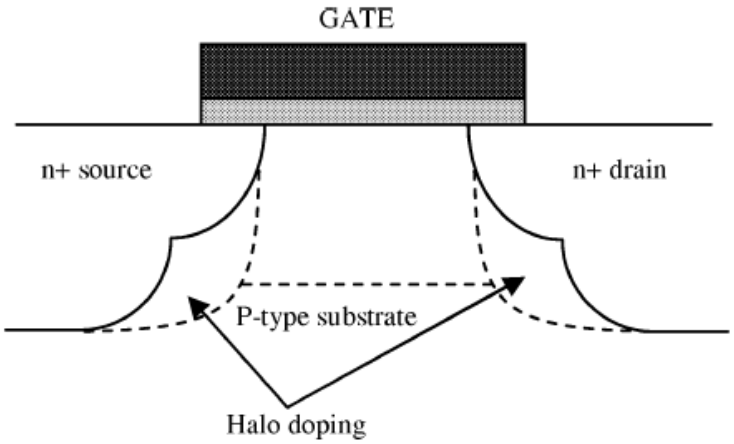

Fig 6: Pocket Implants: Halo Doping

Halo doping [1] or non uniform channel profile in a lateral direction was introduced below 0.25- m technology node to provide another way to control the dependence of threshold voltage on channel length. For n-channel MOSFETs, more highly p-type doped regions are introduced near the two ends of the channel. Under the edges of the gate, in the vicinity of what will eventually become the end of the channel, point defects are injected during sidewall oxidation. These point defects gather doping impurities from the substrate, thereby increasing the doping concentration near the source and drain end of the channel. More highly doped p-type substrate near the edges of the channel reduces the charge-sharing effects from the source and drain fields, thus reducing the width of the depletion region in the drain-substrate and source-substrate regions [11]. As the channel length is reduced, these highly doped regions consume a larger fraction of the total channel. Reduction of charge-sharing effects reduces the threshold voltage degradation due to channel length reduction. Thus, threshold voltage dependence on channel length becomes more flat. With the reduction in drain and source junction depletion region width also reduces the barrier lowering in the channel, thus reducing DIBL.

3. Shallow source and drain

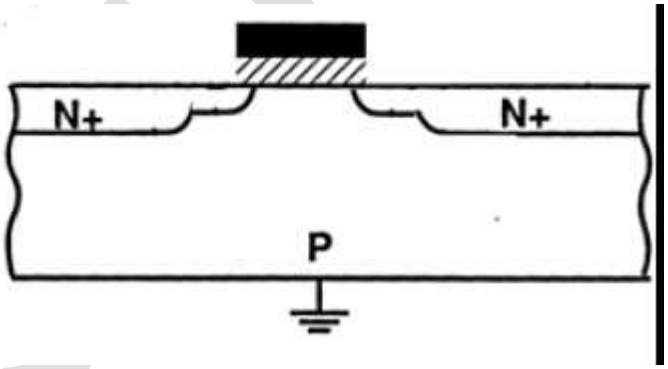

Fig 7: Shallow source and drain regions

- To minimize SCE, we want shallow (small junction resistance *r*j) S/D regions but the parasitic resistance of these regions will increase when *r*j is reduced.
- Shallow S/D "extensions" may be used to effectively reduce *r*j without increasing the S/D sheet resistance too much. Higher surface and channel doping and shallow source/drain junction depths reduce the DIBL effect on the subthreshold leakage current.

4. SOI (Silicon on Insulator) **: SOI** technology [3] refers to the use of a layered silicon–insulator–silicon substrate in place of conventional silicon substrates in semiconductor manufacturing, especially microelectronics, to reduce parasitic device capacitance, thereby improving performance.

- The fully depleted thin film SOI transistors are considered to have smaller SCEs.
- Today we are settling everything in small area .When scaling down the device dimensions the doping densities must be increased to maintain proper device behavior which is hard to manage when the device dimensions reach 50 nm and below. However, for thin film devices, such as fully depleted SOI, the doping densities required are lower. This is one reason for why SOI may be more suitable for the future processes in comparison to bulk CMOS.
- Speed in bulk devices is much determined by the relative magnitude of the parasitic drain and source junction capacitances compared with the gate capacitance, which is increasing as the devices are scaled down and doping levels are increased. Parasitic capacitances of the devices are thereby much smaller in SOI technologies than in bulk technologies.
- The active volume of silicon is smaller in SOI devices than in bulk technology. The SOI devices are therefore less sensitive to high energy particles and make them suitable for use in radiation hard applications.
- The increases of battery powered equipment strongly increase the demand for integrated circuits operating at a low supply voltage and with minimum power consumption .This is also a reason for choosing SOI instead of bulk in the future, since it is more suited to low voltage applications.
- In addition, the current drive capability of SOI devices is higher than for bulk devices, which increases the speed of the device. It also makes it possible to trade speed/power, to get a device with the same speed performance as the bulk device, but at lower power consumption.
- In SOI MOSFETS to enhance the immunity against short channel effects, a number of solutions have been proposed in literature such as (i) thin body SOI with raised source and rain, (ii) buried insulator engineering, (iii) graded channel SOI, (iv) halo doped SOI, (v) ground plane SOI, and (vi) multiple gate SOI.

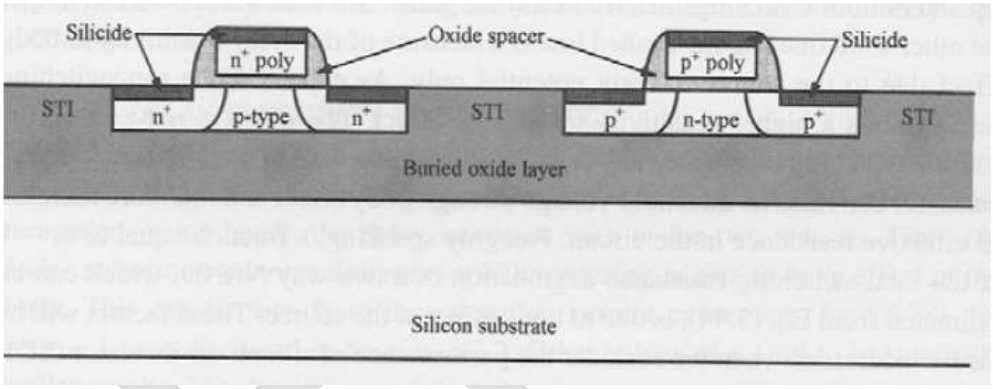

Fig 8: SOI Device

CONCLUSION

When the gate directly couples with the drain or source rather than the channel, it losses some control over the charge in the channel and SCEs are said to have occurred. Better reduction of SCEs and an improvement in the device reliability have been observed with techniques like using properly designed high k material stacks, pocket implants, channel engineering, creating shallow source and drain junctions and SOI technique.

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