

Design and Implementation of Pseudo-carry Compensation Truncation (PCT) Multiplier

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Abstract — The paper is about the implementation of pseudo-carry compensation truncation (PCT) multiplier, which is derived for the multiplexer based array multiplier. Multiplication is a computation intensive and core operation in many algorithms used in scientific computations. Designing an eminence multiplier is always a need to electronics industry. Multiplier is an important element from the point of power consumption and area in the system. Multiplication using truncated scheme provides an efficient method for reducing the power and area as compared to that of full-width multipliers. There are many schemes for truncation in multiplier among them an adaptive pseudo-carry compensation truncation (PCT) scheme gives result with low error. The designed truncated multipliers occupy about 50% less area compared to that of full width multiplier. The designed 64x64bit PCT multiplier occupies same area with approximately 8% less power consumption with low error probability.

Keywords — Xilinx ISE Design Suite 14.5, Verilog, Multiplier, PCT Multiplier, Truncated Multiplier. CCT, VCT, Braun, Vedic

INTRODUCTION

Multiplier is a device which is used to perform the multiplication operation. An eminence multiplier is always being a need of electronics industry for applications in DSP, image processing. A system's performance is generally depending on the performance of the multiplier because the multiplier operation is time consuming which makes it slowest element in the system and it is generally the large area consuming. So optimizing both the speed and area of the multiplier is a key design issue.

The problem of more area and power consumption with fast operation can be overcome using truncation schemes for multiplier. Truncation means cut short. In Mathematics, truncation is to shorten (a number) by dropping a digit or digits. Use of truncation schemes gives significant reduction in complexities of design. Truncation is best suited where exact result is not always required and a rounded product is used for further computation. Multiplication using truncated scheme provides an efficient method for reducing the power and area as compared to that of full width multipliers.

Truncated Multiplier is an array multiplier. A truncated multiplier is a $p \times p$ multiplier with p bits output. In a truncated multiplier the p less significant bits of the full-width product are discarded and to compensate it some of the partial products are removed and replaced by a suitable compensation function, to trade-off accuracy with hardware cost.

Many truncation schemes for array multipliers

- Constant Correction Truncation (CCT)
- Variable Correction Truncation (VCT)
- Pseudo-carry Compensation Truncation (PCT)

In constant correction truncation (CCT) the correction constant is fixed for specific values of n and k regardless of the value of the multiplicand and multiplier. A non-zero DC component of the resulting product is incurred by this fixed correction constant. A non-zero dc component is added based on specific values of n and k to Columns $(n-1)$ to $(k-1)$ of the pp matrix.

To adapt the correction to the input values, a variable correction truncation (VCT) scheme was proposed. A data-dependent variable correction truncation scheme (VCT) is proposed where the most significant pp bits from the $(n-k-1)$ th column are stacked over the $(n-k)$ th column and a constant bias of 'C' is added in Columns $(n-1)$ to $(n-k)$.

The PCT technique takes account of correction to the input values and carries generated in each stage. This scheme is suitable to array multiplier. In this paper pseudo-carry compensation truncation (PCT) scheme is used and the architecture of a multiplier is designed in Verilog HDL language and simulated on Xilinx.

FULL WIDTH MULTIPLIERS

Full width multiplier is a $p \times p$ multiplier with $2p$ bits output. Some examples of full width multipliers are Braun and Vedic multipliers.

Braun Multiplier: It is a simple parallel multiplier generally called as carry save array multiplier. It has been restricted to perform signed bits. The structure consists of array of AND gates and adders arranged in the iterative manner and no need of logic registers. This can be called as non-additive multipliers. An $n \times n$ bit Braun multiplier is constructed with $n(n-1)$ adders and n^2 AND gates as shown in the fig.1. In this paper, designed for 8×8 bit and 64×64 bit Braun multiplier.

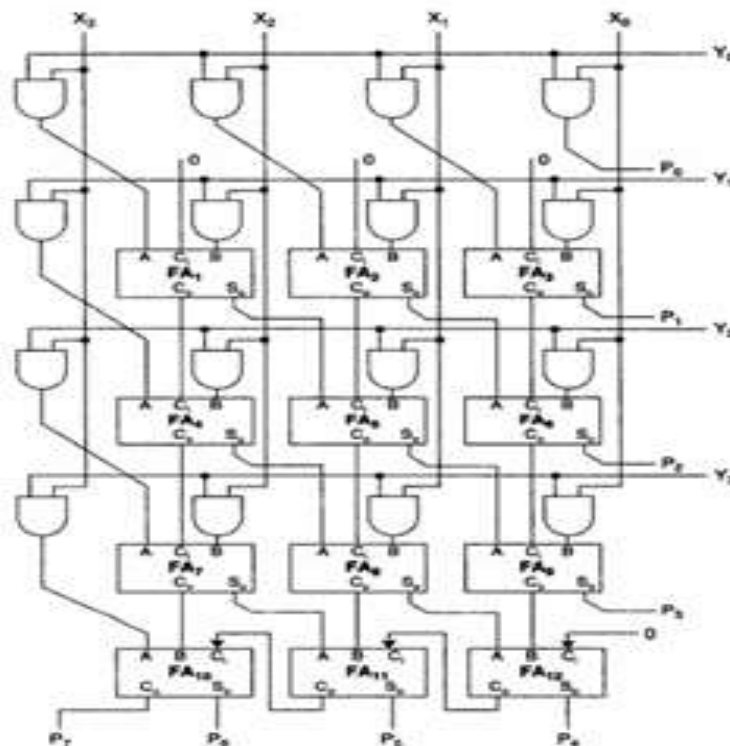


fig.1 Braun Multiplier

Vedic Multiplier: Vedic mathematics is the name given to the ancient system of mathematics. The use of Vedic mathematics lies in the fact that it reduces the typical calculations in conventional mathematics to very simple one. The proposed Vedic multiplier is based on the "Urdhva Tiryagbhyam" sutra (algorithm). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. It is a general multiplication formula applicable to all cases of multiplication. It

literally means “Vertically and Crosswise”. The beauty of Vedic multiplier is that here partial product generation and additions are done concurrently. Hence, it is well adapted to parallel processing. The feature makes it more attractive for binary multiplications. This in turn reduces delay.

The 2X2 Vedic multiplier module is implemented using four input AND gates & two half-adders which is displayed in its block diagram in fig 2.

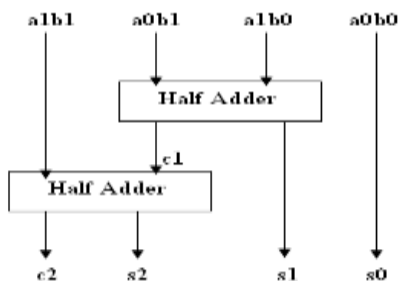


Fig 2: Block diagram of 2x2 Vedic multiplier

The implementation of 4x4 bit Vedic multiplier which uses the 2x2 bit multiplier as a basic building block. The same method can be extended for input bits 4 & 8. In this paper designed for 8x8 bit and 64x64 bit Vedic multiplier.

TRUNCATED MULTIPLIERS

Use of truncations schemes gives significant reduction in complexities of design. Truncation is best suited where exact result is not always required and a rounded product is used for further computation.

Truncated Multiplier: The truncated multiplier is an array multiplier, whose design is based on multiplexer.

The product of two n-bit positive integers $X = x_{n-1}, x_{n-2}, \dots$

, x_1, x_0 And $Y = y_{n-1}, y_{n-2}, \dots, y_1, y_0$ is a 2n-bit product $P = XY$. The numbers are assumed to be fractional in their error analysis and the inputs and output are scaled by a factor of 2^{-n} and 2^{-2n} , respectively.

$$P = \{X_{n-1} + 2^{n-1} x_{n-1}\} \{Y_{n-1} + 2^{n-1} y_{n-1}\}$$

$$P = \sum_{i=0}^{n-1} (x_i \cdot y_i) 2^{2i} + \sum_{i=1}^{n-1} M_i 2^{2i}$$

Where $M_i = X_i \cdot y_i + x_i \cdot Y_i$, M_i can be implemented as a multiplexer With x_i and y_i as select signals. $M_i = 0, X_i, Y_i$ and $X_i + Y_i$ when $x_i, y_i = 00, 01, 10$ and 11 , respectively. Without loss of generality, our proposed truncated scheme can be explained with the help of a truncated multiplexer matrix of Fig. 1 with $n = 8$ and $k = 2$, where k is the number of partial product (pp) columns to be kept beyond the width, n of the truncated product.

The architecture of truncated multiplier is shown in fig 3. It consists of AND gates and two types of fixed input multiplexers. One is with inputs 0, 0, 0, C_i , where C_i is carry bit input of multiplexer which will take care of carry generated in the previous column in architecture or from inputs by ANDing them and other with 0, x_i, y_i, s_i where x_i, y_i are the input bits of 8 bit numbers and s_i is the sum bit taking summation result coming from the previous column of multiplexer. In this paper, designed for 8x8 bit and 64x64 bit truncated multiplier.

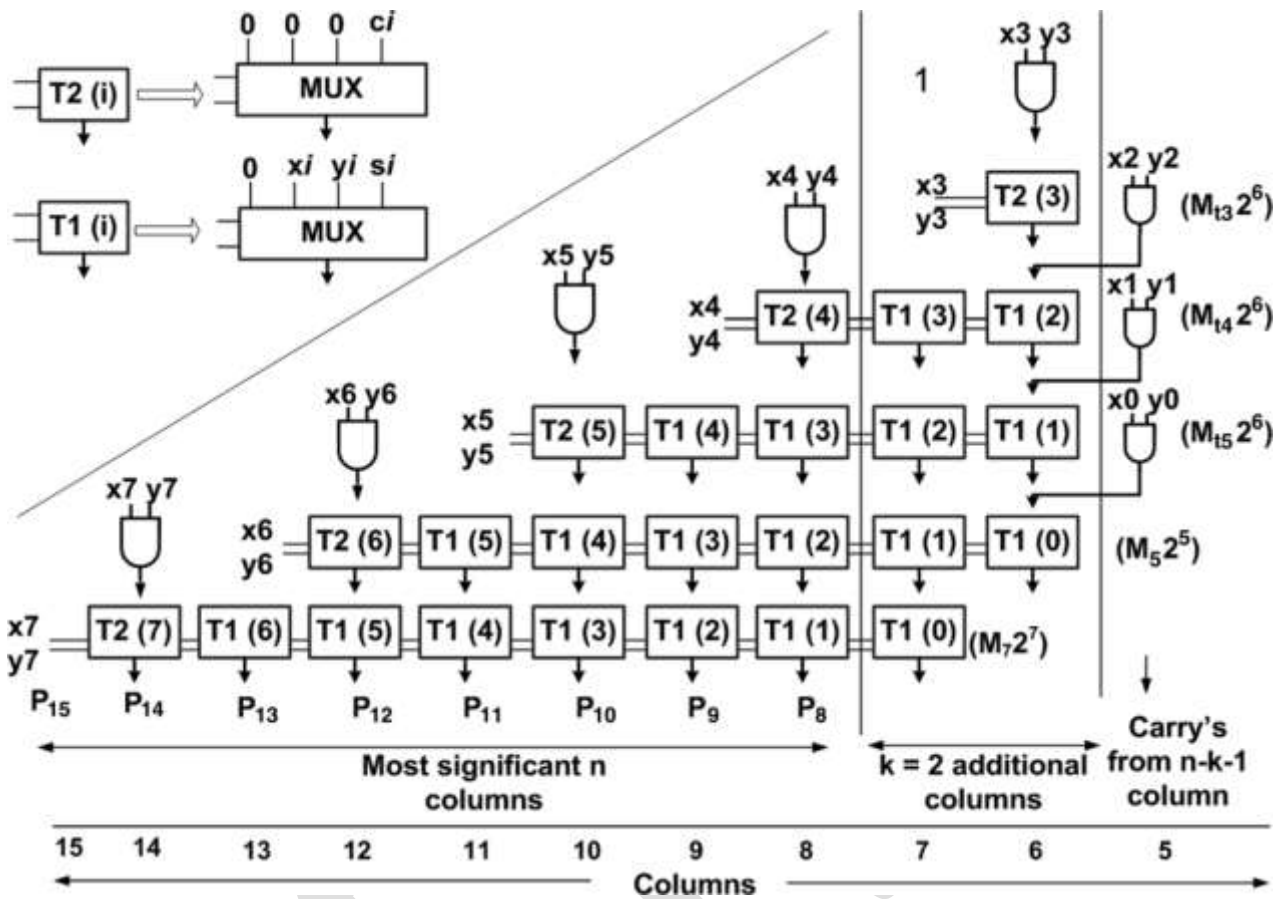


Fig 3: Truncated multiplexer matrix multiplier for an 8*8 bit multiplier; n=8 most significant columns and k=2 additional columns of multiplexers.

Pseudo-carry Compensation Truncation (PCT) Multiplier: By exploiting the symmetry of the multiplexer based array multiplier, the partial product bits generated by the multiplexers in our truncated multiplier can be accumulated in a carry-save format to further reduce the area and improve the speed over other truncated array multipliers.

To minimize the truncation error for an unsigned integer multiplication, a new pseudo-carry compensated truncation (PCT) scheme consisting of an adaptive compensation circuit and a fixed bias is proposed.

The architecture consists of two main blocks. First block is designed with full adder and AND gates which produces two outputs, one for sum and other for carry. Second block is designed using two 4-to-1 multiplexers, in which one multiplexer to generate sum output and other multiplexer to generate carry output. These two blocks are arranged in such a fashion as shown in figure 4.2 to get the final 8 bit truncated product. The first block cells are placed in boundary and the second block cells are placed in the interior of the carry- save architecture, because they receive an additional sum signal from the preceding block.

The adaptive error compensation is realized by the AND cells on the top right, and the fixed correction bias is realized with an input "1" placed on the leftmost first block in the first row. The ripple carry adders (RCA) are used at the bottom of the array to add the

outputs and to get the final product bit. In this project, 8x8 bit and 64x64 bit Pseudo-carry Compensation Truncation (PCT) multiplier are designed.

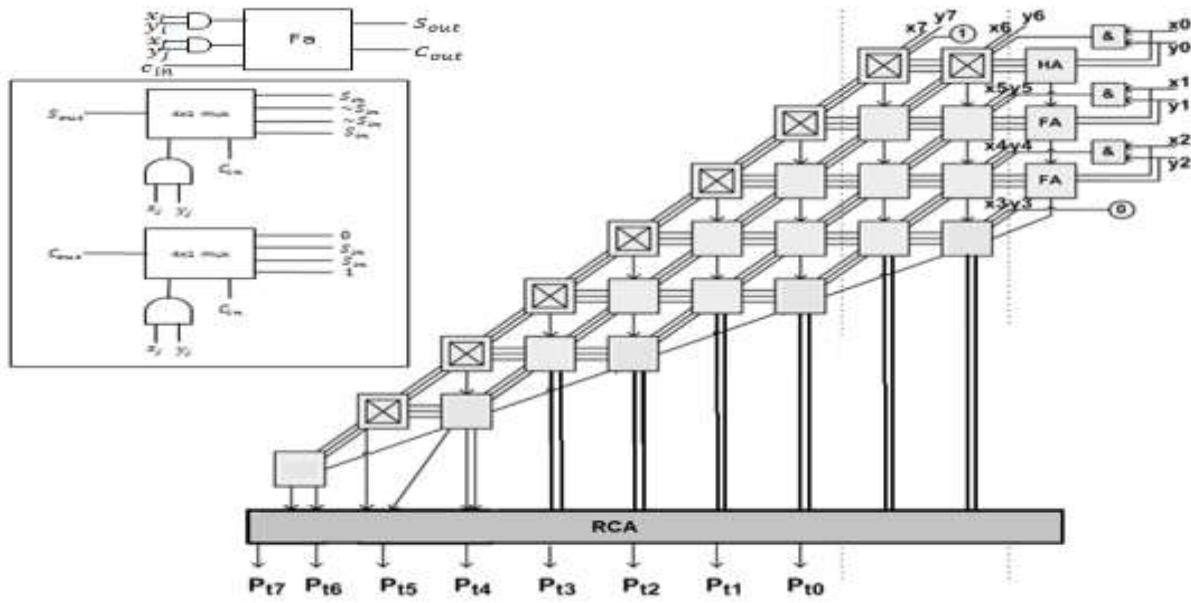


Fig 4: PCT multiplier architecture for n = 8 and k =2

RESULTS

SIMULATION RESULTS:

In this work, the Xilinx ISE is used. Here shows the outputs taken after the simulation and synthesis.



Fig 5: 8x8 Braun multiplier

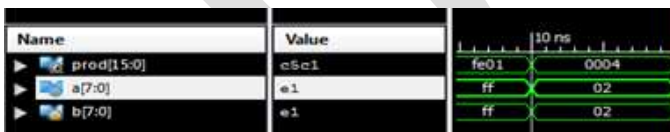


Fig 6: 8x8 Vedic multiplier



Fig 7: 8x8 Truncated multiplier



Fig 8: 8x8 PCT multiplier

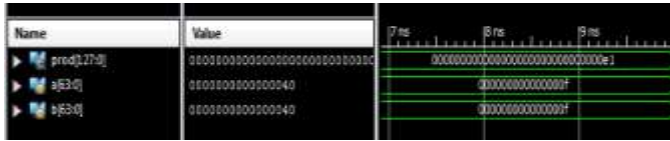


Fig 9: 64x64 Braun multiplier

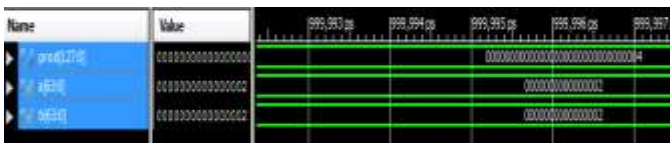


Fig 10: 64x64 Vedic multiplier

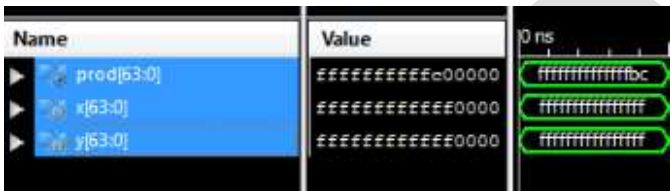


Fig 11: 64x64 Truncated multiplier



Fig 12: 64x64 PCT multiplier

Synthesis Output:

	Available	Full Width Multipliers		Truncated Multipliers	
		Braun	Vedic	CCT	PCT
No. of slices occupied	4656	65	108	43	43
% Area	100%	1%	2%	0%	0%

Table 1: Area Comparison of 8x8 bit

Synthesis Output:

	Available	Full Width Multipliers		Truncated Multipliers	
		Braun	Vedic	CCT	PCT
No. of slices occupied	13132	4672	7588	2427	2427
% Area	100%	35%	57%	18%	18%

Table 2: Area Comparison of 64x64 bit

	Truncated	PCT
Power (W)	0.150	0.138

TABLE 3: POWER CONSUMPTION

CONCLUSION

A conclusion from the results obtained clearly shows that Truncated multipliers occupy very less area compared to full width multipliers. Among truncated multipliers, PCT multiplier is occupying same area, provides low error rate, and power consumption is less. The future work on this is to implement this multiplier for the application of image compression.

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