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High Speed Data Transfer Using FPGA

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Abstract— Field-programmable gate arrays (FPGAs) are reprogrammable silicon chips. Reprogrammable silicon also has the same flexibility of software running on a processor based system, but it is not limited by the number of processing cores available. Unlike processors, FPGAs are truly parallel in nature, so different processing operations do not have to compete for the same resources. With its highly reconfigurable logic they can be used to implement a real time Ethernet communication system using the existing backbone. This project is aimed to study and implement data transmission and reception using the embedded processor in FPGA. The Xilinx Evaluation Board ML505 is used for the purpose. The embedded processor like MicroBlaze is to be configured and accessed through FPGA. The OS intended to be used is Xilkernel. DDR and MAC are configured as the peripherals for the MicroBlaze. A block of data is received, modified and transmitted using the embedded processor in FPGA. The data extracted can then be interfaced to peripherals such as LCD. After realization of the functions on the Xilinx Evaluation Board it can be extended to custom hardware for specific application.

Keywords— FPGA, MicroBlaze, Virtex-5, EDK, SDK, XPS, Xilkernel.

INTRODUCTION

FPGAs are programmable semiconductor devices that are based around a matrix of Configurable Logic Blocks (CLBs) connected through programmable interconnects. That is, any portion of the system can be reconfigured at any time while the rest of the design is still working. With the advancement of Field Programmable Gate Arrays (FPGAs) a new trend of implementing the microprocessors on the FPGAs has emerged in the design community [2]. Nowadays FPGA Boards are connected to PC for function offloading. This can speed up the execution of scientific code for instance.

In Ethernet communication data is transmitted in the form of frames. It contains a header part and after that the data is placed, so that we can retrieve actual data from the Ethernet data. If a processor is used, this can be done easily. The ML505 board supports the embedded processor MicroBlaze, which is a soft processor. By configuring the MicroBlaze, it is able to achieve reception, modification and transmission of GbE packets with a speed of 1Gbps. For better performance MicroBlaze is loaded with Xilkernel as the Operating System (OS).

This paper describes how the GbE transmission and reception are achieved on the Virtex-5 FPGA using MicroBlaze with Xilkernel as OS.

DESIGN APPROACH

A) Why FPGA?

Due to the difference in the arrival time of the data packets there will be gap between the packets. This gap is called Jitter. The jitter must be of the order of few microseconds for the proper functioning of the system. This becomes a huge burden for the ordinary used processor where the entire network stack is implemented in software. FPGA is a better solution for this problem. With its highly reconfigurable logic they can be used to implement a real time Ethernet communication system using the existing backbone [1].

B) Xilkernel

Typical embedded control applications are comprised of various tasks that need to be completed in a particular schedule. As the number of tasks increases it is very hard to manually organize the tasks. Thus the responsiveness and the capability of the application decrease with the complexity. So breaking down the tasks into simple applications and it can be implemented on an OS. Xilkernel is a small, robust and modular kernel. It is highly integrated with platform studio framework and is free software library that is available with Xilinx EDK kit [11]. The main advantage of Xilkernel OS is multithreading functionality.

RELATED WORKS DONE

Gigabit data transmission and reception can be done using the Trimode Ethernet wrapper modules which can be instantiated using the core generator tool available in the Xilinx ISE. It is a prameterizable core ideally suited for use in networking equipment such as routers. It is suited for high density Gigabit Ethernet communication and storage equipment. It works on 10Mbps, 100Mbps and 1000Mbps speed. During the instantiation of the TEMAC, an example design is automatically generated

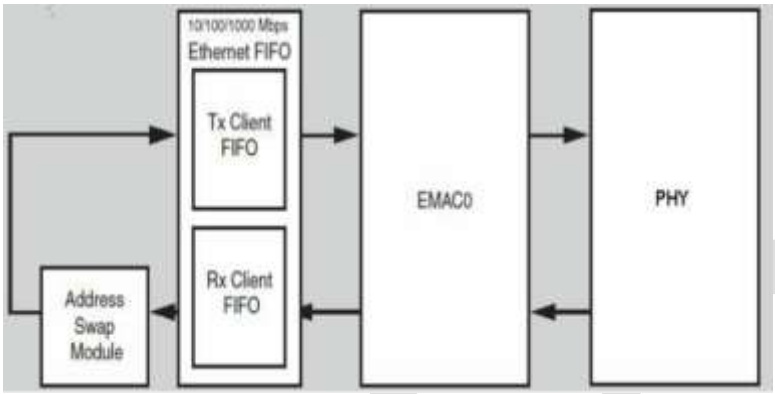

Figure 1 : Example design generated[10]

Here the data is received through the PHY interface .the data is passed through EMAC module and then through the Ethernet FIFO. The EMAC module forms the data link layer for data transmission. Ethernet FIFO is a 4Kb RAM which stores the data.The address swap module will swap the source and destination addresses and it is transmitted through the PHY interface.

The address swap module can be modified such that it can receive a block of data, modify the received data and then it can be transmitted to other location for further processing. Here data is transmitted or received using certain timing diagram.

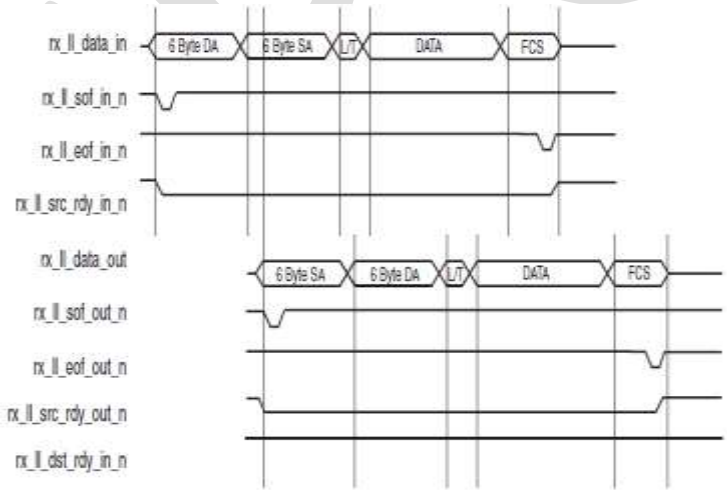

Figure 2: Timing Diagram [10]

DATA IS RECEIVED OR TRANSMITTED ONLY WHEN THE FALLING EDGE OF START OF FRAME (RX_LL_SOF_IN_N) AND FALLING EDGE OF SOURCE READY (RX_LL_SRC_RDY_IN_N). SIMILARLY DATA RECEPTION AND TRANSMISSION STOPS ON THE RISING EDGE OF END OF FRAME (RX_LL_EOF_IN_N) AND RISING EDGE OF SOURCE READY(RX_LL_SRC_RDY_IN_N). SYSTEM DESIGN

A) Hardware Design

The embedded hardware is developed in the BSB (Base System Builder) Wizard inside Xilinx Platform Studio (XPS) by instantiating the embedded processor MicroBlaze soft processor that is supported on the ML505 board with peripherals GPIO LEDs, SDRAM, UART, Ethernet and timer. The MicroBlaze processor accesses its peripherals using Processor Local Bus (PLB) and is selected with clock of 125MHz and local memory of 64KB. UART and Ethernet are the Human Machine Interfaces. The Ethernet which is selected

here is hard Ethernet MAC which supports a speed range of 10mbps to 1000mbps and it is configured in SGMII mode. A block RAM is instantiated using the core generator tool which is available in the Xilinx ISE kit is used as the memory block for storing data packets. The Bock RAM has 32 bit width and 1024 bit depth. The control signals are first written into the bock RAM and then it is transmitted as per the use.

B) Software Design

The software part is designed using the Xilinx SDK tool. The embedded hardware with bit file is exported to the SDK for embedded programming. Here Board Support Package is available. The BSP is changed such that the MicroBlaze processor is loaded with Xilkernel as Operating System. For that standalone mode is changed to Xilkernel 5.01.a and selected lwip 130 and xilflash such that the Ethernet MAC inside the ML505 board can receive and transmit UDP packets.

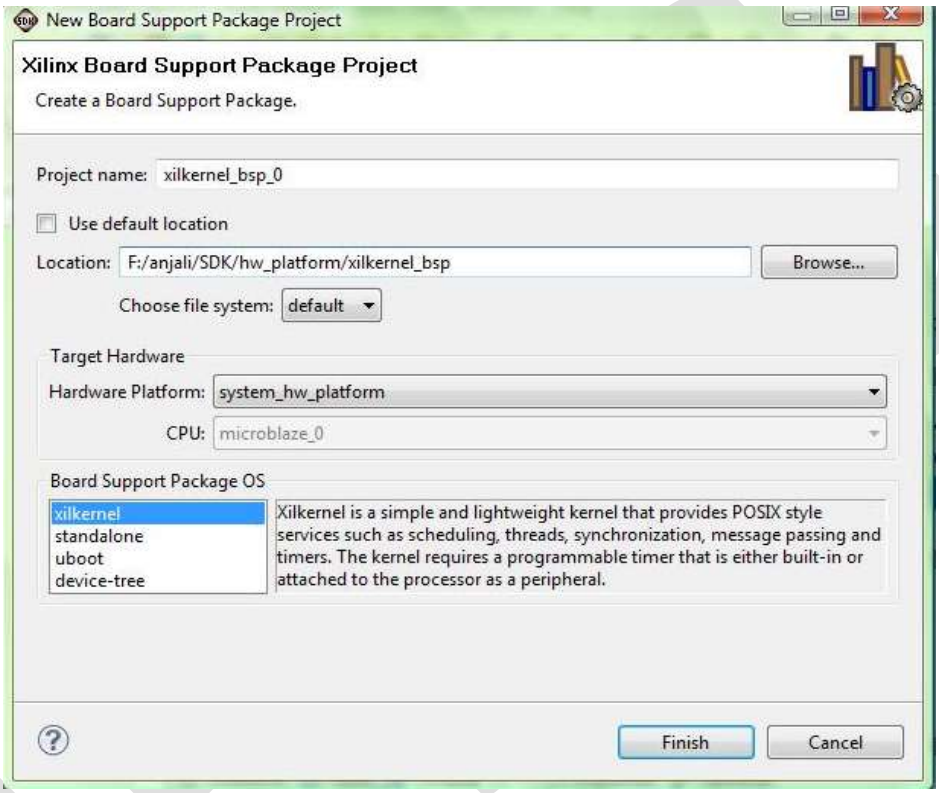

Figure 3: Selecting Xilkernel as OS

After configuring the Xilkernel select the Xilinx c project. There will be a number of project templates provided by the Xilinx SDK tool. Here lwip is configured in socket mode. So select the empty application template and write the client-server C- program for UDP packet reception and transmission. After developing this, debug the program and bit file is generated. Then that bit stream is downloaded to FPGA.

Figure 4 shows the embedded design flow that is the hardware and software design flow.

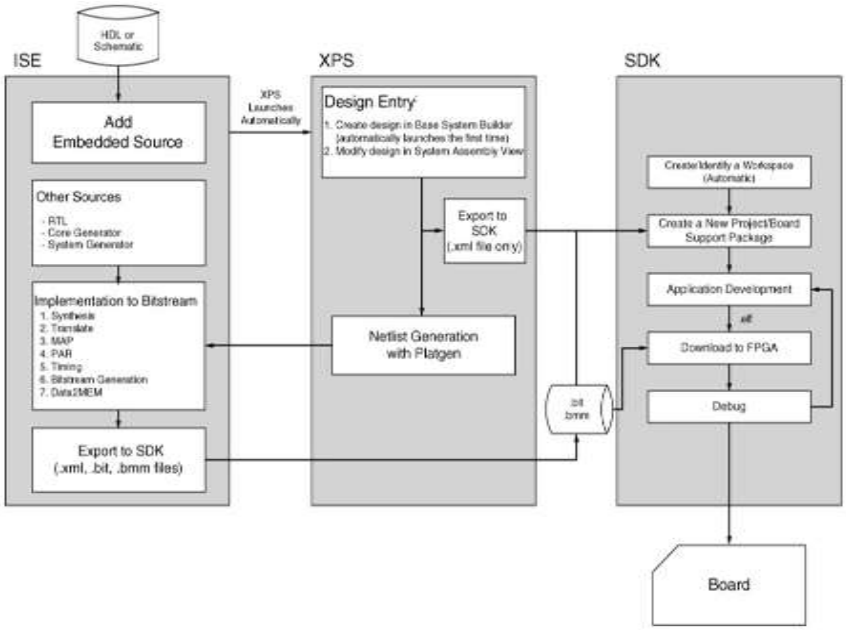

Figure 4: Embedded Design flow [4]

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IMPLEMENTATION

The FPGA board is connected to a computer using Ethernet cable, RS232 and JTAG cable. Then IP address is assigned to the Ethernet interface of the computer. The IP address of the FPGA board and the computer must be in the same subnet. In the application program the board IP address is set to 192.168.1.100. Now the IP address of the computer is changed in the adapter settings to 192.168.1.1.

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CONFIGURATION DETAILS

Board IP: 192.168.1.100
Netmask : 255.255.255.0
Gateway : 192.168.1.1
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Figure 5: Output at serial port

The C-program which is written in the software design is compiled and an executable file is generated and it is downloaded to the FPGA. We use a LABVIEW program which can transmit UDP packets to FPGA board with IP 192.168.1.100. After running the LABVIEW program the Ethernet connection LED, transmit LED, receive LED and Ethernet speed indicating LED with 1Gbps speed lights up showing that reception and transmission are in progress. GPIO LEDs are connected so that received data can be shown in LED.

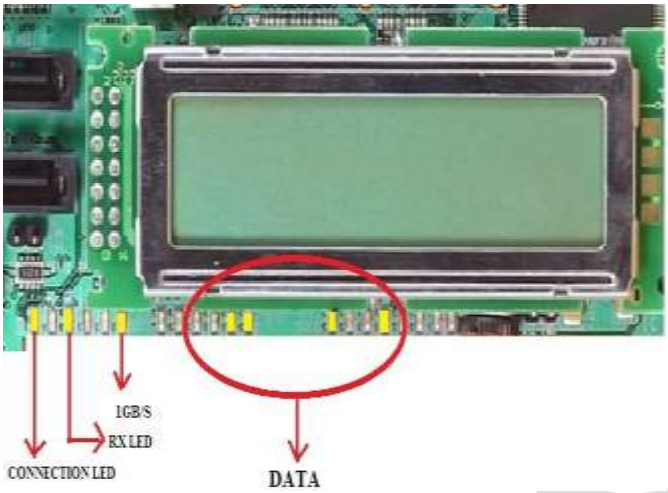

Figure 6: Interfacing with LED

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The data that is transmitted using LABVIEW is received at the board. In figure5, '9' is received and the ASCII value corresponding to '9' ie '39' is shown on the data LEDS. Similarly a 20 byte data is transmitted using the LABVIEW and it is received at the board. Then the received data is modified and then it is transmitted from the FPGA board. The data which is transmitted is 1, 2, 3, 4, 0, 0 corresponding ASCII values are also shown in the figure. This data is received and modified by adding a constant '56' and the result is 1, 2, 3, 4, 5, 6 and then it is transmitted. These can be analyzed by capturing these packets in Wireshark.

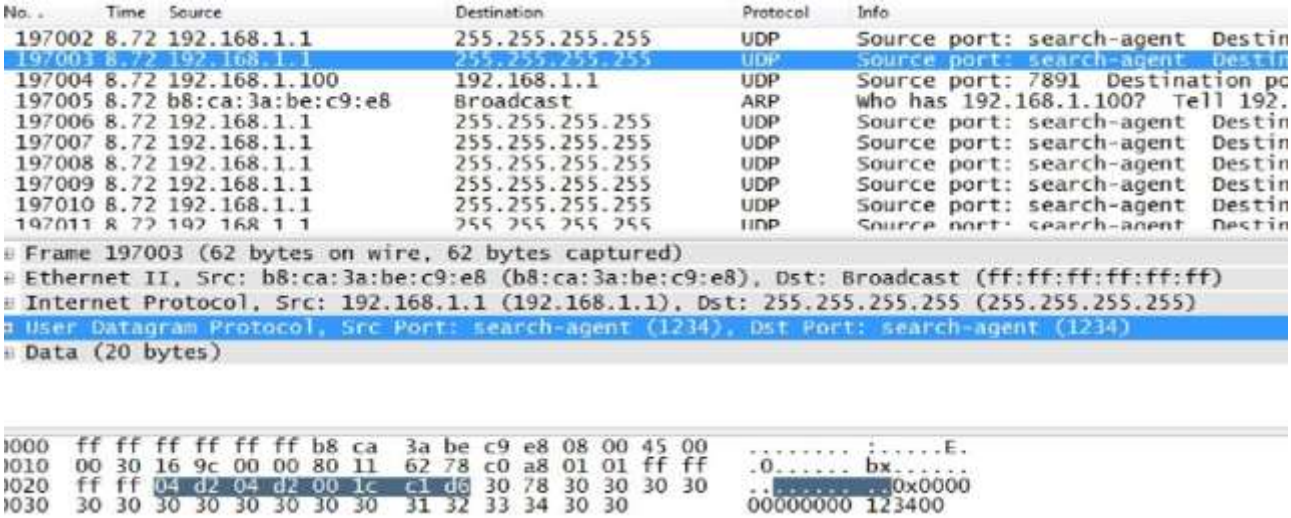

Figure 7: Received frames captured in Wireshark

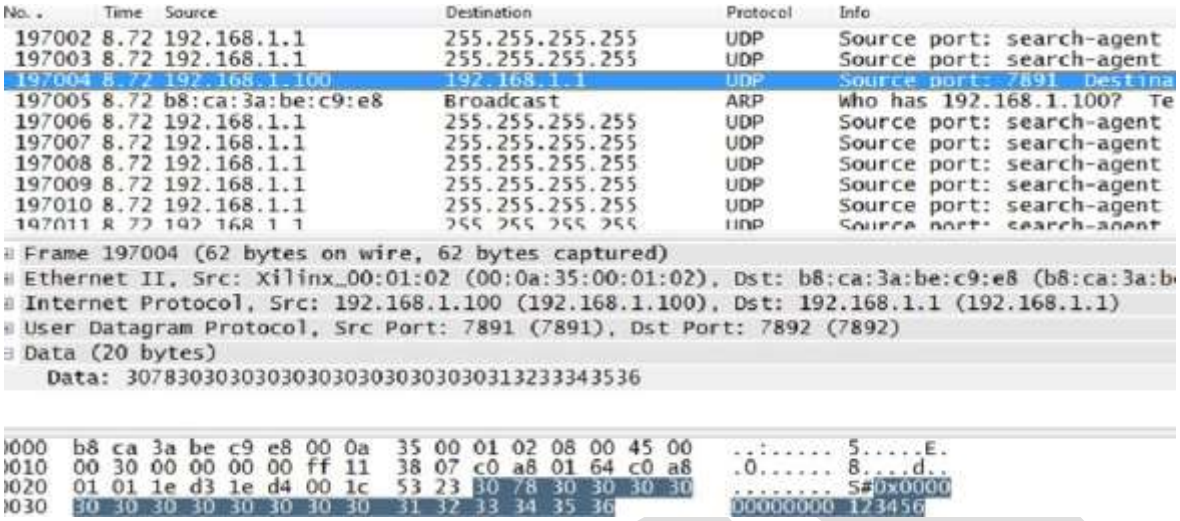

Figure 8: Modified frame which is transmitted is captured

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CONCLUSION

MicroBlaze soft processor with Hard Ethernet MAC was configured using the EDK tool. Using SDK, Xilkernel was loaded inside the processor as the Operating System. This configuration is capable of receiving packets sent to the board's IP address. Then processor will modify the data accordingly and will display it on the data LEDs. Then the modified data is transmitted to other locations for further processing

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