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Modelling and Simulation of Unipolar HVDC Link

Assistant Professor Karan Gupta[1], Shubham Abrol[2], Suvan Sharma[3], Chahat Bakshi, Vikram Singh

Department of Electrical Engineering, GCET Jammu

Email address: [1]karan74_gupta@yahoo.com, [2]sabrol538@gmail.com, [3]suvansharma01@gmail.com

Abstract—The use of high voltage AC transmission of bulk power over long distance invite the attention of transmission of high voltage DC for long lengths of line. HVDC systems suffer relatively lower electrical losses and require relatively lower economic expenditure, for long distance transmission. In this paper we simulate a unipolar HVDC transmission link using twelve pulse thyristor convertors. The changes in output waveforms are noted for change in firing angles and DC fault conditions.
Keywords—*HVDC, Unipoar, Rectifier, Inverter, Three Phase AC, Firing angle and DC fault.*

INTRODUCTION

Voltage conversion in an AC system is simple as high power levels and high insulation levels are allowed by an AC transformer in one unit, and also losses are low. Its simplicity and superiority of a three phase synchronous generator over DC generator led and encouraged the introduction of AC technology in the development of electrical power systems. But, disadvantages linking to AC transmission like limits on transmission capacity due to inductive and capacitive elements of overhead lines, impossibility of direct connection between two AC systems with different frequencies and system instability caused by direct connection between two AC systems with the same frequency compelled and engaged engineers over ages in substituting AC transmission by DC transmission. With the invention of mercury arc rectifiers in the 20th century, line commutated current sourced converter could be designed. Next major development occurred when thyristor valves replaced mercury arc valves. The need for parallel connection and large number of series connected thyristors per valve has been extinguished by the development of thyristors with high current and voltage rating. Innovations and appreciable development in areas of HVDC have increased reliability of HVDC systems significantly.

METHODOLOGY

General Overview

In this paper we have illustrated the modelling of a unipolar HVDC link using 12 pulse thyristor converters and perturbations are applied to examine performance of the transmission system. A 1000 MW (500kV, 2KA) DC unipolar link is used to transmit power from a 500kV, 5000 MVA, 50Hz system to a 345 kV, 10000 MVA, 50Hz system. The AC systems are represented by an emf source in series with inductance and damped L-R equivalents.

Circuit Block Diagram

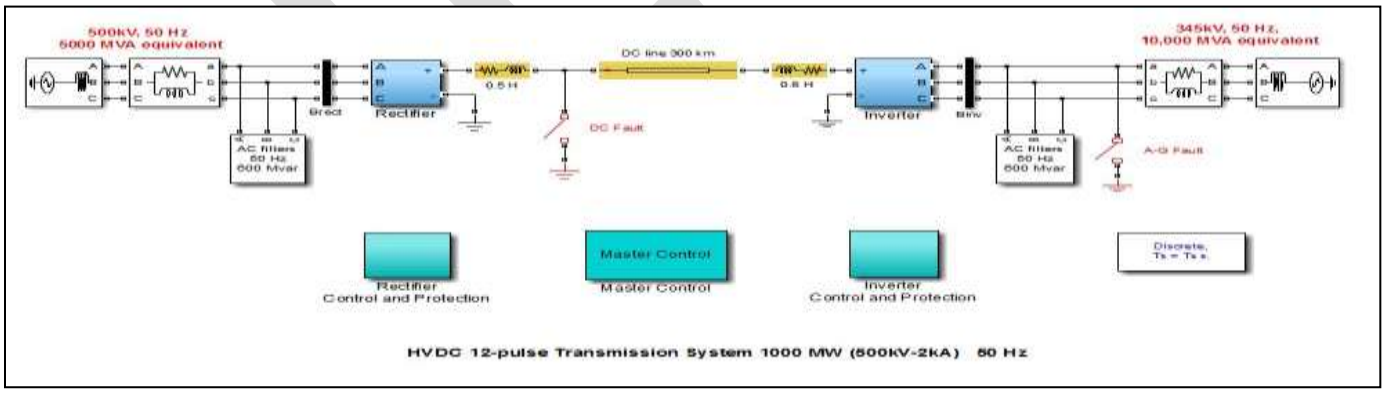

Fig. 1: Circuit Block Diagram

The rectifier and inverter are 12-pulse bridge converters using two Universal Bridge blocks. These two Universal Bridge blocks are connected in series. A 300 km line is used to interconnect the converters. 0.5H smoothing reactors are used on both sides. The Three Phase Three Winding blocks are used as the converter transformers blocks. These are Wye grounded on primary side, Wye connected on secondary side and Delta on tertiary side. The tap changing of the transformer is not simulated and hence the tap positions are fixed and determined by a multiplication factor of 0.9 for the rectifier and 0.96 for inverter which applied to the primary voltage of the three

phase three winding transformers. The HVDC converter acts as a source of harmonic currents for the AC side. and harmonic voltages for the DC side. The order of the ac harmonic is one less than or greater than the intergral multiple of number of pulses and that of dc harmonic is integral multiple of number of pulses.

$n = kp \pm 1$ (for AC current)

$n = kp$ (for direct voltage);

k being an integer and p being number of pulses,

Since we have used 12 pulse circuit, hence the harmonics on AC side are of the order 11,13,23,25 and so on and that on DC side is of order 24,36 and so on.

AC filters are used to control the spreading out of the odd harmonic currents on the AC system and high passes damped filters are used to control even harmonics. The filters are grouped into two subsystems. These filter subsystem also contains a capacitor bank which is used to provide reactive power compensation to the circuit. This reactive power compensation is required because of the different firing angle of the thyristors in the converter circuit. The series RLC filter is used to eliminate the 11^{th} and 13^{th} harmonic and high pass damped filter is used to eliminate 24^{th} harmonic.

The breaker block applies faults on the reactifier DC side to check for the stability of the system during fault. The sample time of Ts=50µs with the disrete steps are used for both the HVDC system and the rectifier and inverter control and protection subsystems. These control susbsystems are basically the PI controllers which takes the error inputs and based on those inputs generate the output current reference for both the rectifier and inverter and helps in the starting and stopping of the HVDC power transmission. The protection systems can be switched ON and OFF.

SIMULATIONS

In the first case the circuit is run and output waveforms are analyzed. In second case the firing angle is changed and circuit is simulated. In the third and final case DC fault condition is simulated and output waveforms analyzed accordingly.

Case 1

The simulation of unipolar HVDC link is run with the inverter firing angle between 92^o and 166^o. The simulation is started, current is first ramped up to the steady state, then negative current step is added, after some time positive voltage step is added and the current is ramped down at the time of stopping of the system. The different waveforms are studied in the rectifier and inverter scope. The waveforms reproduced are as follows:-

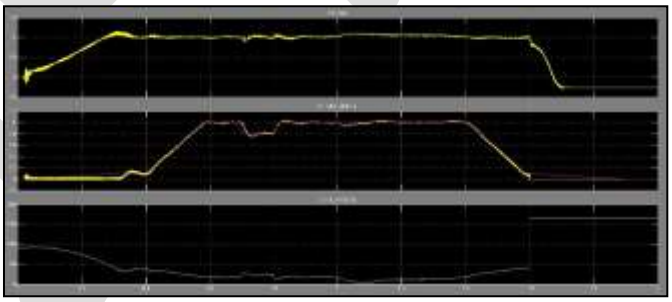

Fig. 2: V_{dL}, I_d and alpha_order v/s time waveforms across Rectifier

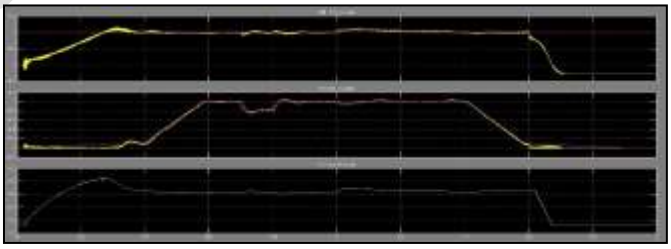

Fig. 3: V_{dL}, I_d and alpha_order v/s time waveforms across Inverter

At the start of simulation the converters pulse generators in the master control are deblocked and the power transmission started by ramping the reference current at t=20ms and triggering the 12 pulse rectifier and inverter circuit with firing angle of 92^o and 102^o respectively. At t=0.3s, the reference current reaches a value of 0.1pu, the DC current starts to build, the inverter firing angle α reaches the maximum value of 166^o and the voltage V_{dL} across rectifier and inverter crosses the reference voltage 1pu and makes an overshoot to 1.2pu meanwhile the current I_d takes an overshoot and reaches the value around 0.1pu. At t=0.4s, the reference current is ramped from 0.1 to 1 pu (5kA) in 0.18s (5pu/s) and the dc current I_d increases with the reference current keeping V_{dL} constant and then the dc current shifts from transient to steady state at t=0.58s. The trace 1 of rectifier and inverter scope shows the DC line voltage (1pu=200 kV), trace 2 shows the reference current and the measured I_d current (1pu=5 kA) and trace 3 shows the firing angle of both the rectifier and inverter. The rectifier and inverter are current and voltage controlled device resp. but during ramp both controls current. At t=0.7s, a -0.2pu step is applied during 0.1s to the reference current, hence the current I_d decreases with the step but the slight decrease in voltage seen keeping it constant. At t=1.0s, a 0.1pu step is applied during 0.2s at the inverter reference voltage. The voltage takes the shoot to 1.1pu mean while current decreases to 0.9 and becomes constant after which voltage regulator regulates the voltage and the voltage and current reaches the value of 1pu. The firing angle α of rectifier and inverter are around 16.5 degree and 143 degree respectively at t=1.35s. At t=1.4s the controller stops the simulation by ramping down the current to min value of 0.1pu keeping the voltage constant. At t=1.6s the firing angle alpha is forced to 166 deg at the rectifier and to 92 deg at the inverter which extinguishes the current and brings down the DC voltage due to the trapped charge in the line capacitance. At t=1.7s the pulses are blocked in both converters.

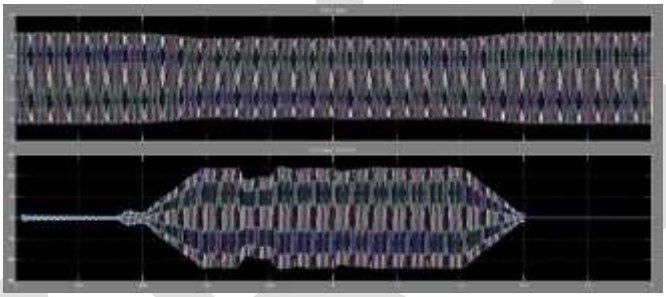

Fig. 4: AC voltage and current v/s time On Rectifier Side

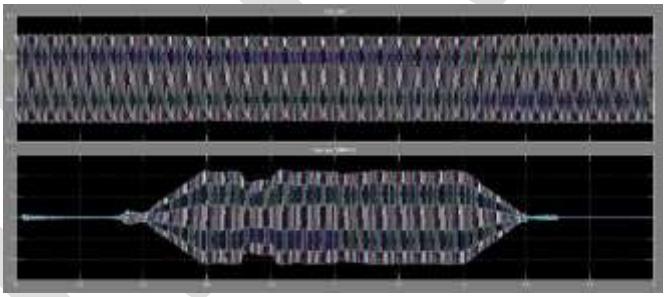

Fig. 5: AC voltage and current v/s time On Inverter Side

At t = 0 s, V_{abc_r} is around 1.1 pu and V_{abc_i} is around 1.06 pu but the I_{abc_r} and the I_{abc_i} are 0 pu/100 MVA. Then At t = 0.3 s, I_{abc_r} and I_{abc_i} increases to 2 pu/100 MVA and 1.6 pu/100 MVA resp. meanwhile V_{abc_r} and V_{abc_i} decreases to 1.08 pu and 1.05pu resp. At t = 0.4 s, V_{abc_r} decreases from 1.08 pu to 0.9 pu and V_{abc_i} decreases from 1.05 pu to 1 pu and the I_{abc_r} increases from 1.5 pu/100 MVA to 12 pu/100 MVA and I_{abc_i} increases from 1 pu/100 MVA to 11 pu/100 MVA. At t=0.7s, V_{abc_r} and V_{abc_i} increases to 1pu and I_{abc_r} and I_{abc_i} decreases to 9 pu/100 MVA and 8.2 pu/100 MVA. At t=0.8s, V_{abc_r} and V_{abc_i} continue to remain same and I_{abc_r} and I_{abc_i} increases to 12pu/100 MVA and 11.2pu/100MVA. At t=1.4s, V_{abc_r} starts increasing to 1.1 pu but V_{abc_i} is same and I_{abc_r} and I_{abc_i} drops from 12 to 1.1pu/100 MVA and 11 to 1 pu/100 MVA respectively. At t=1.6s, V_{abc_r} and V_{abc_r} are same and I_{abc_r} and I_{abc_i} finally attains a value of 0.1pu/100 MVA.

Case 2

The simulation of unipolar HVDC link is run with the change in inverter firing angle between 105^o and 142^o. This is because whenever there is change in load in the inverter end (the load can be inductive, capacitive or anything), the required current changes or

the reactive power compensation is required hence the firing angle of the inverter is changed manually. The simulation is started, current is first ramped up to the steady state, then negative current step is added, after some time positive voltage step is added and the current is ramped down at the time of stopping of the system. The different waveforms are studied in the rectifier and inverter scope. The waveforms reproduced are as follows:-

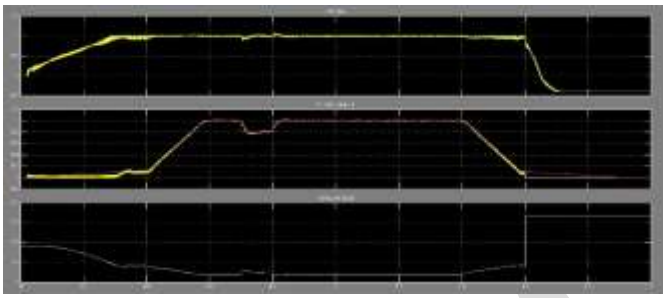

Fig. 6: V_{dL}, I_d and alpha_order v/s time waveforms across Rectifier

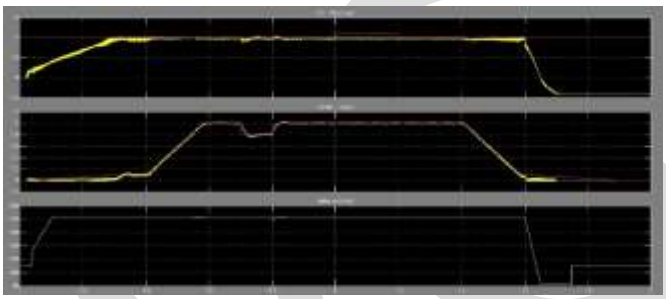

Fig. 7: V_{dL}, I_d and alpha_order v/s time waveforms across Inverter

At the start of simulation the converters pulse generators in the master control are deblocked and the power transmission started by ramping the reference current at t=20 ms and triggering the 12 pulse rectifier and inverter circuit with firing angle of 92^o and 117^o. At t=0.3 s, the reference current reaches a value of 0.1 pu, the DC current starts to build, the inverter firing angle α reaches the maximum value of 142^o and the voltage V_{dL} across rectifier and inverter takes an shoot to 1 pu and then reaches the steady state 1 pu value, meanwhile the current I_d increases from 0 pu and reaches the value around 0.1 pu. At t=0.4s, the reference current is ramped from 0.1 to 1 pu (2 kA) in 0.18 s (5 pu/s) and the dc current I_d increases with the reference current keeping V_{dL} constant and then the DC current shifts from transient to steady state at t=0.58 s. The trace 1 of rectifier and inverter scope shows the DC line voltage (1 pu=200kV), trace 2 shows the reference current and the measured I_d current (1pu=5kA) and trace 3 shows the firing angle of both the rectifier and inverter. The rectifier and inverter are current and voltage controlled device resp. but during ramp both controls current. At t=0.7s, a -0.2 pu step is applied during 0.1 s to the reference current, hence the current I_d decreases with the step and the rectifier voltage decreases to 0.9 pu and then increases to 1.1 pu at the end of step but the slight decrease in inverter voltage seen keeping it constant. At t=1.0s, a 0.1 pu step is applied during 0.2 s at the inverter reference voltage. The voltage and current remains constant. The firing angle α of rectifier and inverter are around 18.5 degrees and 142 degrees respectively at t=1.35s. At t=1.4s the controller stops the simulation by ramping down the current to min value of 0.1pu keeping the voltage constant. At t=1.6s the firing angle alpha is forced to 166 deg at the rectifier and to 92 deg at the inverter which extinguishes the current and brings down the DC voltage due to the trapped charge in the line capacitance. At t=1.7s the pulses are blocked in both converters.

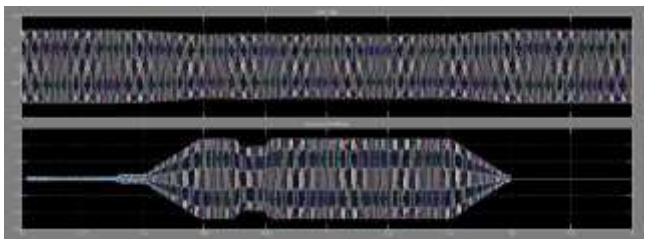

Fig.8: AC voltage and current v/s time on Rectifier Side

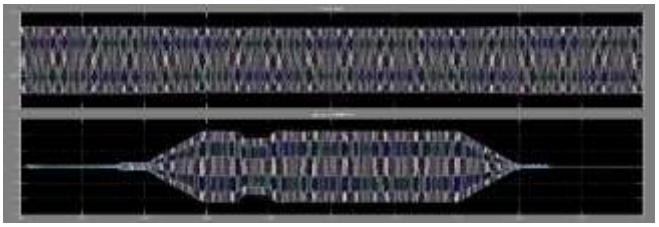

Fig.9: AC voltage and current v/s time on Inverter Side

At t=0s, V_{abc_r} and V_{abc_i} are around 1.1pu and 1.06pu respectively but both the I_{abc_r} and I_{abc_i} are 0 pu/100 MVA. Then at t=0.3s, I_{abc_r} and I_{abc_i} increases to 1.5 pu/100 MVA and 1.3 pu/100 MVA respectively but V_{abc_r} decreases to 1.08 pu keeping V_{abc_i} constant. At t = 0.4 s, V_{abc_r} and V_{abc_i} decreases to 0.9 pu and 1.06pu but the I_{abc_r} increases from 1.35 pu/100 MVA to 11.8 pu/100 MVA and I_{abc_i} from 1.2 pu/100 MVA to 11.1 pu/100 MVA. At t=0.7s, V_{abc_r} and V_{abc_i} increases to 0.98 pu and 1.01pu but I_{abc_r} and I_{abc_i} decreases to 9.2 pu/100 MVA and 8.6 pu/100 MVA. At t=0.8s, both V_{abc_r} and V_{abc_i} continue to remain same and I_{abc_r} increases to 12pu/100 MVA and I_{abc_i} to 11.2pu/100 MVA. At t=1.4s, V_{abc_r} increases to 1.1 pu keeping V_{abc_i} constant but I_{abc_r} drops from 12 to 1.1pu/100 MVA and I_{abc_i} from 11.1 to 1.5 pu/100 MVA. At t=1.6s, both V_{abc_r} and V_{abc_i} are same and both I_{abc_r} and I_{abc_i} finally attains a value of 0.05 pu/100 MVA.

Case 3

The simulation of unipolar HVDC link is run with inverter firing angle between 92^o and 166^o with the dc fault. The DC fault is mainly the line to ground fault of the DC line. DC fault is applied by deactivating the steps applied on the current reference and on the voltage reference in the Master Control and in the Inverter Control and Protection respectively by setting the switches in lower position. The simulation is started, current is first ramped up to the steady state, then the dc fault is applied and then the current is ramped down at the time of stopping of the system. The different waveforms are studied in the rectifier and inverter scope. The waveforms reproduced are as follows:-

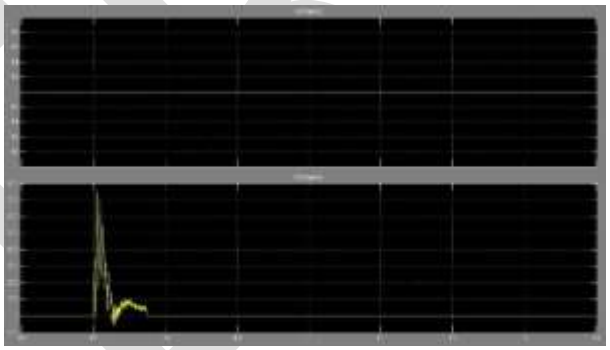

Fig 10: AC and DC Fault Current v/s time

At t=0.7s dc fault is applied and the fault current increases to 7500A with the transient reaching 0A at t=0.725s and then slightly increases to 1000A and then extinguishes at t=0.75s. The ac fault current remains 0A.

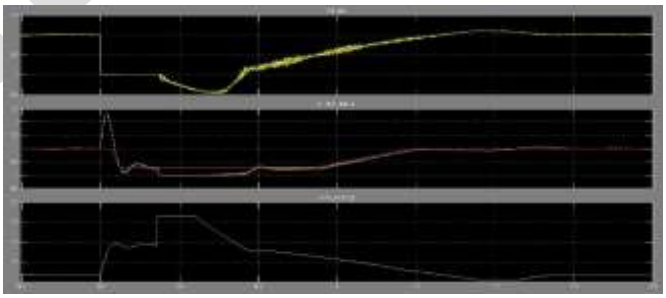

Fig. 11: V_{dL}, I_d and alpha_order v/s time waveforms for Rectifier

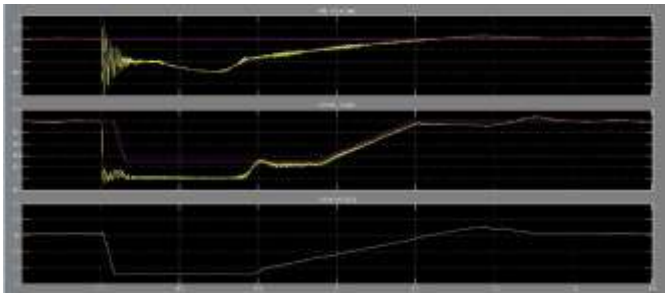

Fig. 12: V_{dL}, I_d and alpha_order v/s time waveforms for Inverter

At t = 0.7 s, the dc fault is applied and the dc current at rectifier increases to 2.2 pu and at inverter drops to zero but the dc voltage at rectifier and inverter falls to zero. This Voltage Dependent Current Order Limiter (VDCOL) and the DC Fault protection detects the DC voltage drop and hence reduces the reference current at both the rectifier and inverter to 0.3 pu. A DC current flows between the line to ground fault. Then, at t = 0.77 s, a low DC voltage is detected by the DC fault protection circuit which forces the rectifier and inverter firing angles α to 166 and 92 degrees respectively. The rectifier then operates in inverter mode and inverter in rectifier mode due to which the energy stored in the lie is returned to the ac system which forces the dc fault to extinguish also the line voltage becomes negative and reaches the maximum value of -0.5 pu. Then at t=0.82s the firing angle of rectifier decreases and that of inverter increases due to which dc current increases to 0.3pu with voltage crossing 0pu. Then at t=0.9s the current reference is then ramped and reaches the value of 1pu and the dc current and voltages increases with the ramp. Now the dc voltage and dc current takes a shoot to 1.1 pu then reaches the value of 1 pu between 1.18 s and 1.25 s in both rectifier and inverter.

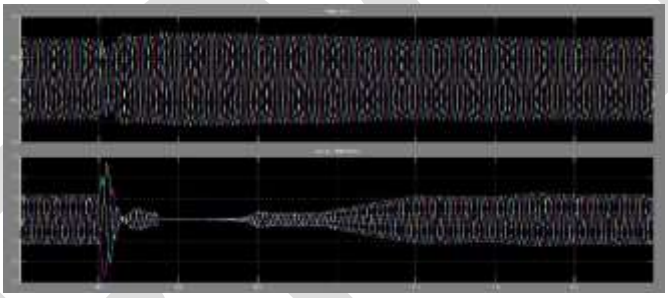

Fig.13: AC voltage and inverter v/s time on Rectifier Side

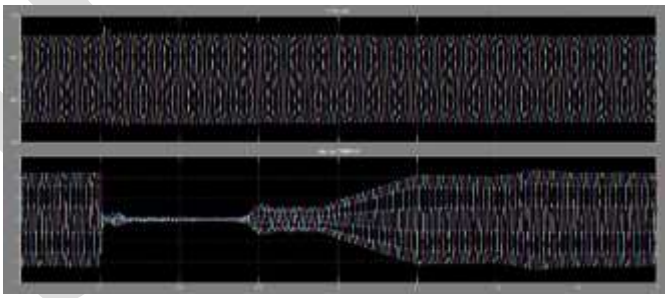

Fig.14: AC voltage and current v/s time on Inverter Side

At t=0.7s, V_{abc_r} decreases to 0.7 pu and V_{abc_i} increases to 1.3pu but I_{abc_r} increases to 25 pu/100 MVA and I_{abc_i} decreases to 1pi/100MVA. Then at t=0.73s, V_{abc_r} increases to 1.1pu and V_{abc_i} decreases to 1.1pu and I_{abc_r} decreases to 2 pu/100 MVA and I_{abc_i} increases to 2 pu/100 MVA. At t=0.75s, both V_{abc_r} and V_{abc_i} remains same and I_{abc_r} increases to 5 pu/100 MVA and I_{abc_i} decreases to 0.5 pu/100 MVA. At t=0.85s, V_{abc_r} and V_{abc_i} decreases to 0.95pu and 1.05pu respectively and I_{abc_r} and I_{abc_i} increases to 10pu/100 MVA and 4 pu/100 MVA respectively. At t=1.2s, both V_{abc_r} and V_{abc_i} increases to 1 pu and I_{abc_r} and I_{abc_i} increases to 13 pu/100 MVA.

CONCLUSION

This paper concludes with the observation that whenever the system is simulated, the controller increases the reference current slowly with the ramp so that transient surges are prevented from occurring so that the dc current and voltage increases with the reference current and becomes constant at the steady state. Also if any fault occurs in the HVDC system the system detects the fault and extinguishes the fault automatically without changing the system parameters making the system stable.

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