

# DESIGN OF RECONFIGURABLE SYSTEM ON CHIP BASED HIGH SPEED DATA ACQUISITION SYSTEM FOR MARINE APPLICATION

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**Abstract --** The main aim to propose a processor for the data acquisition by sensors, which can be monitored and transmitted. A flexible and reconfigurable SoC is developed. A NIOS II based system on chip is used for the SOPC creation. The Altera Quartus tool with the SOPC builder used for building the hardware part of the processor and the NIOS II IDE used for the building of software part of the processor. A pressure signal can be acquired by the pressure transducers (PTX 1830/1840) from the source side and converted into pressure signal and then transmitted to the destination. Transmission can be done by using ZigBee protocol. Then those signals can be compared with the data sheets and warning can be given.

**Keywords –** NIOS, SoPC, Altera FPGA, Pressure Transducer, ZigBee.

## I. INTRODUCTION

To design a reconfigurable processor with the high speed data acquisition from the sensor, the processor is designed by the NIOS II software with the help of system on chip (SoC) concept to build the software part of the system with the requirements of external hardware components for the processor. Then the reconfigurable processor the developed with the basic ALU unit, memory unit, and control unit. The ALU unit performs basic arithmetic and logical operations. The memory unit will stores the output data in the external data card (SDRAM).then the control unit controls all other unit in the processor. So the software part of the system is design with the NIOS II processor and the hardware part is done with the Altera Cyclone IV, DE-0 Nano board for the data acquisition from the sensor, a flexible and reconfigurable SoC is developed for the efficient data acquisition. The data acquisition by the sensor which converts any measurement parameters to an electrical signal which can be monitored displayed and transmitted to an control room. The external SDRAM card is used for the memory purpose and the transmission is done through the wired/wireless medium to the control room.

This project describes the Nios II processor from a high-level conceptual description to the low-level details of implementation. The primary reference for the Nios II family of embedded processors and is part of a larger collection of documents covering the Nios II processor and its usage that you can find on the page of the Altera website

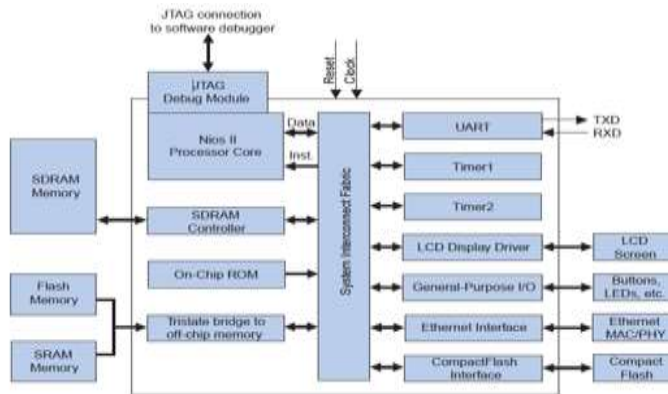
### 1.1 Nios II Processor System:

The Nios II processor is a general-purpose RISC processor with the following features:

- Full 32-bit instruction set, data path, and address space
- 32 general-purpose registers.
- Optional shadow register sets.
- 32 interrupt sources.
- External interrupt controller interface for more interrupt sources.
- Single-instruction  $32 \times 32$  multiply and divide producing a 32-bit result.
- Dedicated instructions for computing 64-bit and 128-bit products of multiplication.
- Floating-point instructions for single-precision floating-point operations.
- Single-instruction barrel shifter.
- Access to a variety of on-chip peripherals, and interfaces to off-chip memories and peripherals.
- Hardware-assisted debug module enabling processor start, stop, step, and trace under control of the Nios II software development tools.
- Optional memory management unit to support operating systems that require MMUs.
- Optional memory protection unit (MPU).
- Software development environment based on the GNU C/C++ tool chain and the Nios II Software Build Tools (SBT) for Eclipse.

- Integration with Altera's SignalTap II Embedded Logic Analyzer, enabling real-time analysis of instructions and data along with other signals in the FPGA design.
- Instruction Set Architecture (ISA) compatible across all Nios II processor systems.
- Performance up to 250 DMIPS.

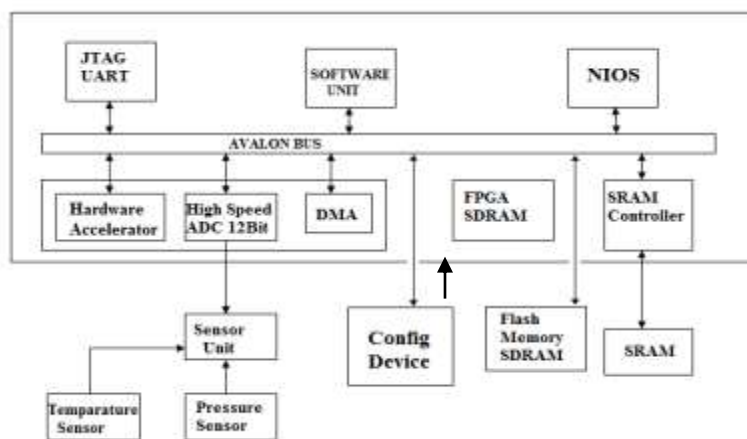
A Nios II processor system is equivalent to a microcontroller or “computer on a chip” that includes a processor and a combination of peripherals and memory on a single chip. A Nios II processor system consists of a Nios II processor core, a set of on-chip peripherals, on-chip memory, and interfaces to off-chip memory, all implemented on a single Altera device. Like a microcontroller family, all Nios II processor systems use a consistent instruction set and programming model.



**Fig 1.1.** Example of a Nios II Processor System

Using the Nios II hardware reference designs included in an Altera development kit, you can prototype an application running on a board before building a custom hardware platform. Figure 1–1 shows an example of a Nios II processor reference design available in an Altera development kit. If the prototype system adequately meets design requirements using an Altera-provided reference design, you can copy the reference design and use it without modification in the final hardware platform. Otherwise, you can customize the Nios II processor system until it meets cost or performance requirement.

**1.2. Design of Reconfigurable system:**



**Fig 1.2** Block Diagram of the Reconfigurable System

Avalon Bus:

- It is a communication protocol.
- It establishes the communication between NIOS processor and overall system component.
- It uses two Avalon bus interface named as (i) MM (ii) ST

Jtag Uart:

- It is used for debugging purpose while run time.
- It is also used for serial data transmission between hardware and PC.

It is used to insert hardware break points in the run time and used for efficient

debugging.

Baud rate for this Jtag Uart is 9600bps and default is 115200bps.

Software Unit:

It denotes the coding part.

This unit is user interface to the hardware.

It is written in Embedded C and it also can be done by assembly language.

System.h header file defines the H/W Abstraction Layer (HAL) of overall system.

A main.c is added to accumulate all the top level system access.

Hardware Accelerator:

A H/W accelerator is developed to access high speed 12bit ADC data from ADC 128S022 lower power 8 channel CMOS 12 bit A/D convertor.

It uses SPI controller to acquire data.

On SPI master/slave protocol is designed as Verilog module to access data.

DMA:

It is used as a separate buffer unit to hold the ADC data temporarily.

External interface to ADC is given through GPI02.

Config Device:

SRAM object file is loaded in config device after overall H/W development is finished.

SRAM Controller:

Used for internal data/register storage for the processor.

FPGA SDRAM:

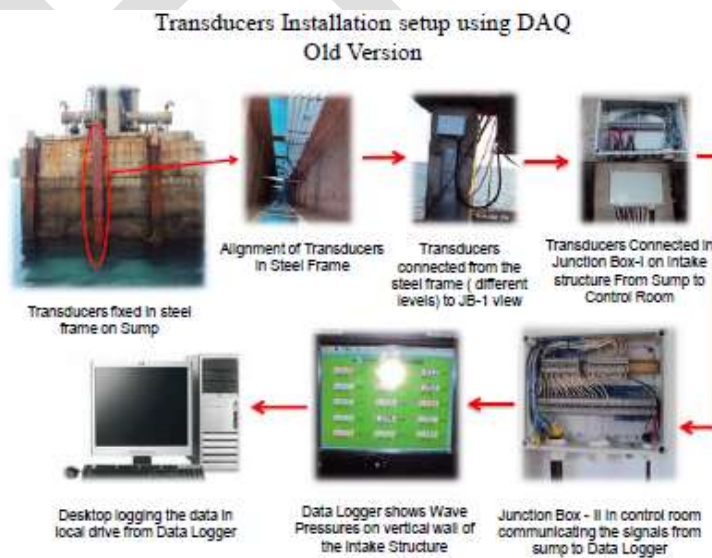
NIOS II will boot by this SDRAM only.

32MB SDRAM starts the NIOS core.

A special/dedicated SDRAM controller IP is developed for the memory access in processor.

## II. PROPOSED & EXISTING SYSTEM

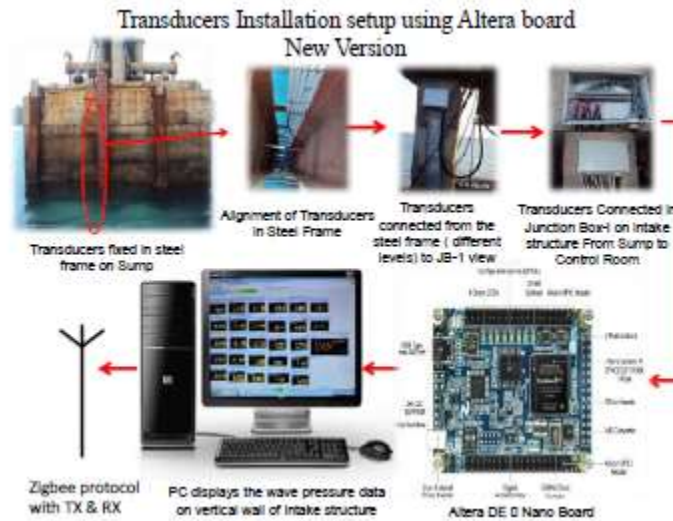
### 2.1. Existing system:



**Fig 2.1. Model of the existing system**

The data from the pressure transducer can be acquired in the array of transducers and combined into a single data and given into a junction box. Then the data can be sent to the data logger unit for splitting the data and stored in a memory unit. Then the data is taken in a memory card and sent to the control room through a wired medium.

## 2.2. Proposed System:



**Fig 2.2. Model of the proposed system**

Here the data acquisition can be done in similar way as existing one. The usage of the data logger unit is replaced by the altera FPGA board. The acquired data has been displayed in the system as continuously. Then those signals are transmitted to the control room through wireless protocol ZigBee.

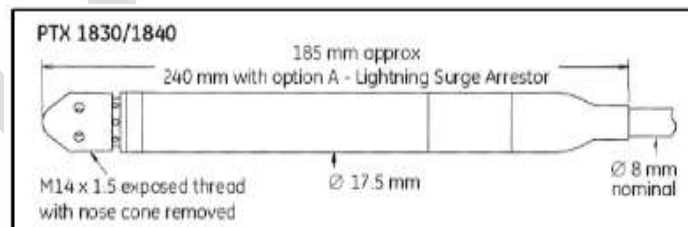
## III. INSTRUMENTATION USED FOR SYSTEM

The major instruments was used in the present study

- Pressure transducers
- Altera DE-0 Nano Board
- ZigBee protocol(TX & RX)

### 3.1. Pressure transducers

Pressure transducer of 15 No's used for measurement of waver pressures on the vertical wall. The time history of dynamic pressures will be measured by using GE Druck make (PTX 1830/1840) diaphragm type pressure transducers. The capacities of the pressure transducers are 0 -5 bar. The instantaneous change in the displacement of the diaphragm due to the action of external pressure is proportional to the instantaneous change in the applied pressure. Figure shows installation drawing of PTX 1830/1840 pressures transducer & Figure actual view of PTX 1830/1840 pressures transducer used in the present study. Displacement transducers will be fixed on the wall, sense the displacement of the diaphragm accurately. The real time histories of the proposed measured pressures are arrived by using the calibration coefficients of the pressure transducers. Table 1 shows technical specification of the pressure transducers.



**Fig 3.1. Installation drawing of PTX 1830/1840 pressures transducer**



Fig 3.2 Actual view of PTX 1830/1840 pressures transducer

Table 1-Technical specification of Pressure Transducer

S.No	Description	Value
1.	Range	0-5 bar
2.	Accuracy	± 0.1% F S
3.	Type	2 wire
4.	Output current	4 to 20 mA
5.	Application	Sea water
6.	Material	Titanium / SS 316L
7.	Process connection	1/2" NPT
8.	Protection	IP 68 / submersible in Marine Environment
9.	Operation Temperature	0-50° C
10.	Frequency	2000 Hz

3.2. Altera DE-0 Nano Board:

Layout and Components:

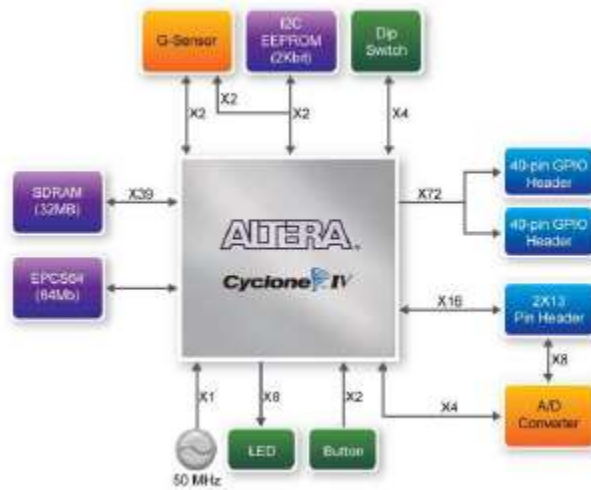
The picture of the DE0-Nano board depicts the layout of the board and indicates the locations of the connectors and key components.



Fig-3.3. The DE0-Nano Board PCB and component diagram (top & bottom view)

Block Diagram of the DE0-Nano Board:

The block diagram of the DE0-Nano board is to provide maximum flexibility for the user all connections are made through the Cyclone IV FPGA device. Thus, the user can configure the FPGA to implement any system design.



**Fig-3.4. Block diagram of DE0-Nano Board**

#### IV. RESULTS AND DISCUSSION

##### 4.1. Calibration of Pressure Transducers

The static calibration of pressure transducers was done using the conventional method by lowering and raising the pressure transducer to known depth of immersion and registering the changes in the corresponding currents and pressure using multimeter and data logger. The calibration charts for all the pressure transducers used in the present investigation.

**Table 2 shows the sample calculation of calibration constant for pressure transducer.**

Sl. No	Water Depth in m	Measured Current In mA		Average in mA	Difference in mA
		Low ring	Lifting		
1	0	3.99	3.99	3.99	
2	1	4.31	4.31	4.31	0.32
3	2	4.62	4.62	4.62	0.31
4	3	4.93	4.93	4.93	0.31
5	4	5.24	5.24	5.24	0.31
6	5	5.56	5.56	5.56	0.32
7	6	5.88	5.88	5.88	0.32
				<b>Average</b>	<b>0.32</b>

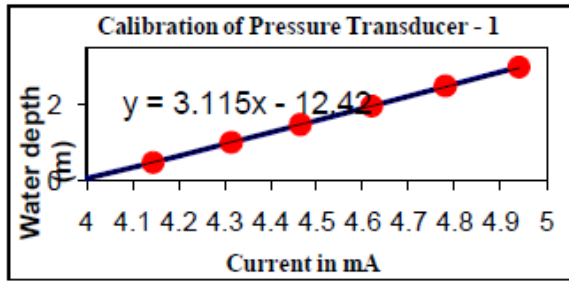


Figure 4.1 Calibration chart for pressure transducer-1

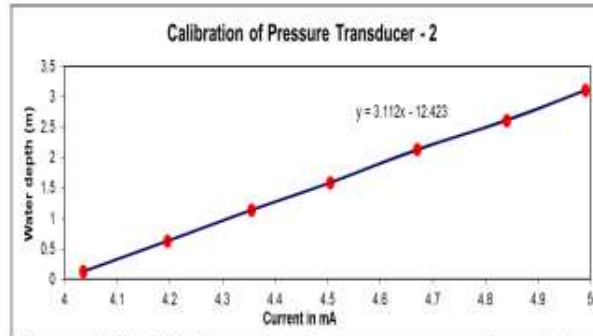


Figure 4.2 Calibration chart for pressure transducer-2

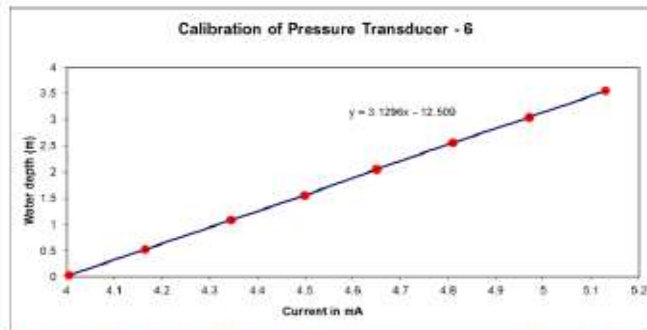


Figure 4.6 Calibration chart for pressure transducer-6

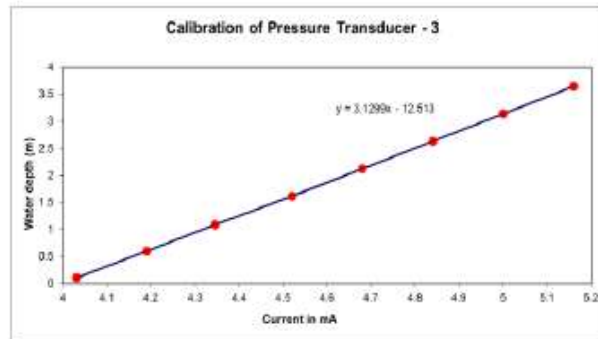


Figure 4.3 Calibration chart for pressure transducer-3

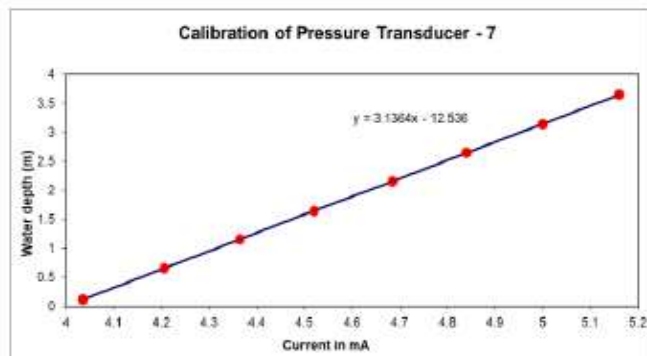


Figure 4.7 Calibration chart for pressure transducer-7

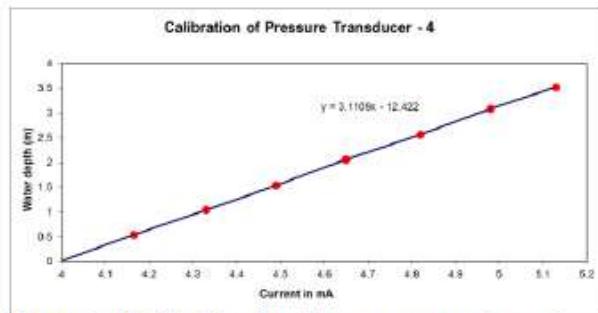


Figure 4.4 Calibration chart for pressure transducer-4

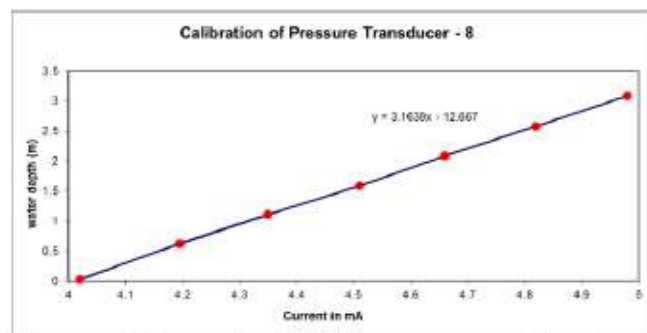


Figure 4.8 Calibration chart for pressure transducer-8

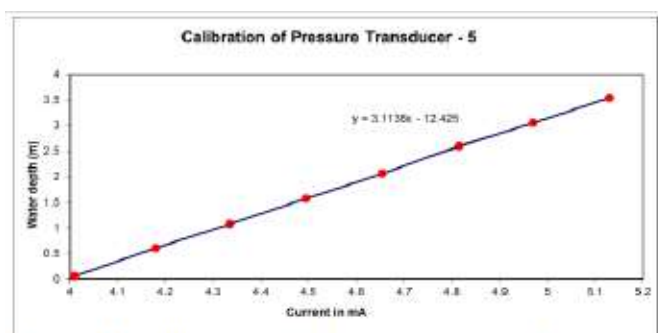


Figure 4.5 Calibration chart for pressure transducer-5

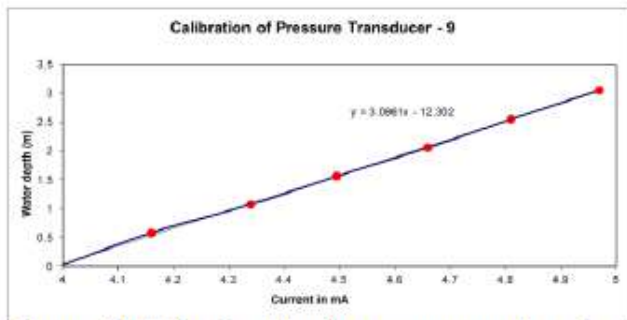


Figure 4.9 Calibration chart for pressure transducer-9

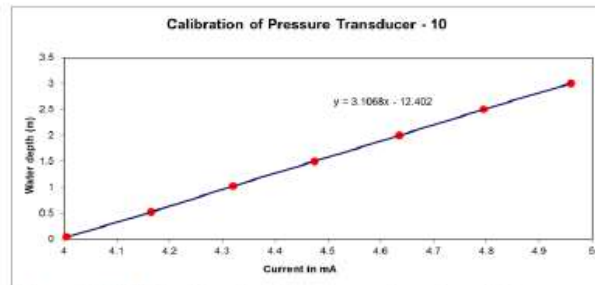


Figure 4.10 Calibration chart for pressure transducer-10

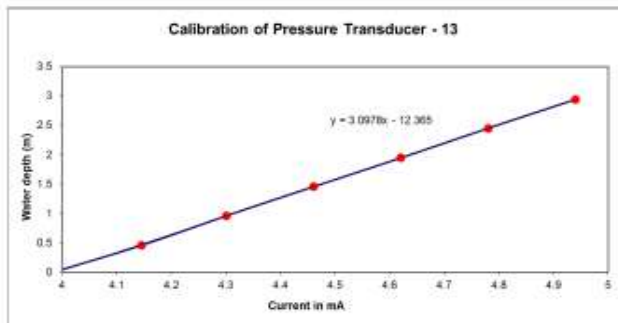


Figure 4.13 Calibration chart for pressure transducer-13

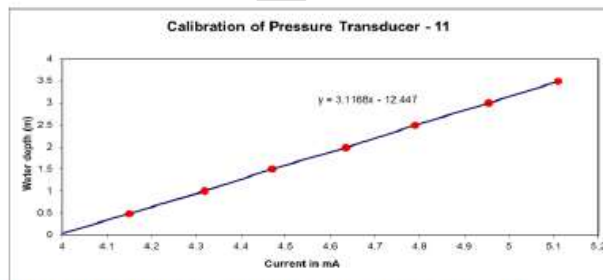


Figure 4.11 Calibration chart for pressure transducer-11

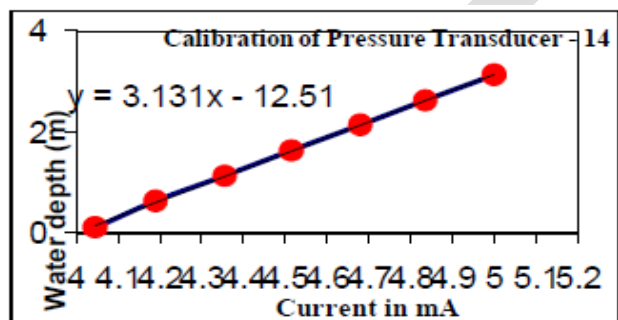


Figure 4.14 Calibration chart for pressure transducer-14

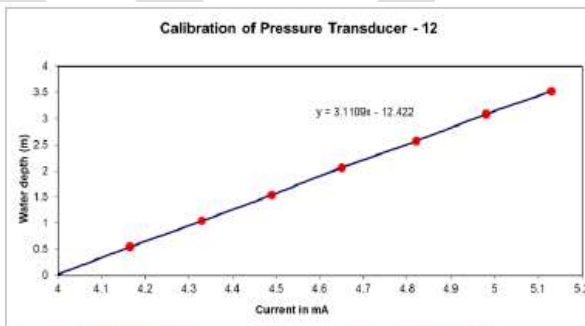


Figure 4.12 Calibration chart for pressure transducer-12

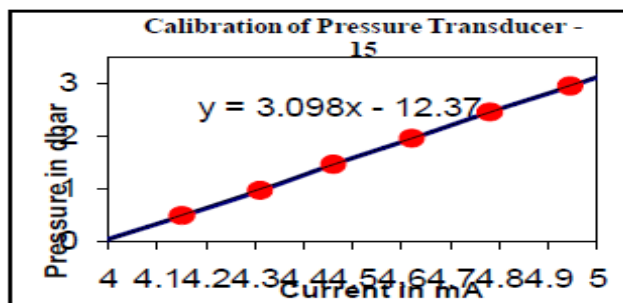


Figure 4.15 Calibration chart for pressure transducer-15

## V. CONCLUSION AND FUTURE WORK

### 5.1. Conclusion:

Thus the data acquisition for a marine application using a reconfigurable system on chip concepts was concluded that the acquired pressure data from the transducer by the Altera DE-0 Nano Board will be monitored by the system, and the data was transmitted to the control room by ZigBee wireless protocol with a distance of 40-50 meters. Based on the resulting values the corresponding warning signals like tsunami, cyclone etc., will be announced to the people by the scientist from the control room.



## 5.2. Future Work:

The acquired data can be transmitted to the destination by the same wireless protocol with a distance of 1000's of meters and the warning signals will be given to the people by automatically using some software through online.

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