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Fully Reconfigured VLSI architecture of FM0, Manchester and Miller Encoder for DSRC Applications

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Abstract- Intelligent transportation system (ITS) aim to provide innovative services at different modes of transport and traffic management. Dedicated short range communication (DSRC) is a new technique to promote the intelligent transportation into our daily life. DSRC standard generally use FM0 and Manchester codes for encoding. These codes enhance the signal reliability with dc balance. The coding diversity between FM0 and Manchester codes limits the potential to design a fully reused VLSI architecture for both codes. This project proposes a fully reused VLSI architecture design by using SOLS (similarity oriented logic simplification) technique. This technique overcome the coding diversity between FM0 and Manchester and Miller encoding for DSRC application. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce the number of transistors. This project is mainly motivated by the desire to implement the intelligent transportation system concept to the real world because of the key benefits in safety and travelling ease in a low cost manner. Here in this project we are using FM0, Manchester and Miller encoding techniques to reach dc balance and enhancing the signal reliability. The SOLS technique improves the hardware utilization rate to 100%. The encoding capability of this paper fully support the DSRC standards of America, Europe, and Japan. This paper not only develops a fully reconfigured VLSI architecture, but also exhibits a competitive performance compared with the existing works. All the codes for the processor design are written in Verilog HDL.

Keywords: Dedicated short-range communication (DSRC), FM0 encoder, Manchester encoder, Miller encoder, SOLS technique, VLSI, FPGA

1. INTRODUCTION

Today, automobile industries are paving a way for intelligent transportation. Google driverless cars are the state of art in this direction. DSRC system plays an important role in modern automobile industry. DSRC is an emerging technique, it is one way or two way short to medium range wireless communication. It enables different users to be better informed, make safer, more coordinated and advanced use of transportation networks. The DSRC standards have been established by several organisation in different countries.

DSRC can be classified into two categories. These are automobile to automobile and automobile to roadside. In automobile to automobile, the DSRC provides the message sending and broadcasting for safety issues public information announcement. It mainly deals with the collision alarms, hard break warnings etc. In automobile to roadside, the DSRC enables the intelligent transportation services such as ETC (Electronic Toll Collection), highway rail intersection warning, in vehicle signing etc.

System architecture of DSRC transceiver consists of three modules namely; base band processors, RF front end and the microprocessors. The microprocessor is used to transfer the instruction to the baseband processing and RF frontend. The RF frontend is used to transmit and receive the wireless signals using the antenna. The baseband processing is responsible for modulation, error correction, encoding and synchronization.

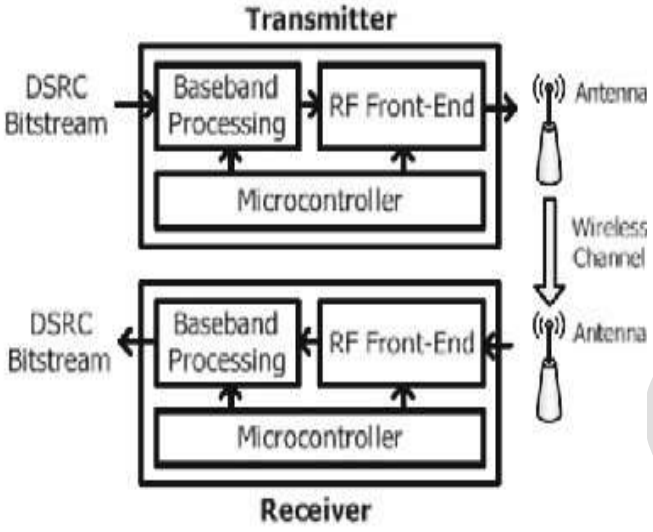

Fig. 1. System architecture of DSRC transceiver

2. LITERATURE REVIEW

An accountable work is being done in this field of intelligent transportation and modern automobile industries are devoting considerable amount of resources for research in this field. Because in day to day life the intelligent transportation system has its own advantages like smooth traffic control, vehicular safety etc. The following section will point out the evolution of the proposed project's work and research till date.

P. Benabes, A. Gauthier, and J. Oksman implemented a Manchester code generator running at 1 GHz. This literature [4] proposed a VLSI architecture of Manchester encoder for the use of optical communication. This design used the CMOS inverter and the gated inverter as the switch for the construction of Manchester encoder. It was executed by 0.35-μm CMOS technology and its operation frequency is 1 GHz .(P. Benabes, A. Gauthier, and J. Oksman 2003)

M. A. Khan, M. Sharma, and P. R. Brahmanandha presented FSM based Manchester encoder for UHF RFID tag emulator. This literature [5] also proposed a Manchester encoding architecture for ultrahigh frequency (UHF) RFID tag emulator. This hardware architecture is operated by the FSM (finite state machine) of Manchester code, and is performed by FPGA (field-programmable gate array) prototyping system. The maximum operation frequency of this architecture is about 256 MHz. (M. A. Khan, M. Sharma, and P. R. Brahmanandha 2008)

Karagounis, A. Polyzos, B. Kotsos, and N. Assimakis implemented a 90nm Manchester code generator with CMOS switches running at 2.4 GHz and 5 GHz. This literature [3] later replaced the architecture of switch in [5] by the NMOS device. It is performed in 90nm CMOS technology, and the maximum operation frequency is higher than 5 GHz. (A. Karagounis, A. Polyzos, B. Kotsos, and N. Assimakis 2009)

Y.C. Hung, M. M. Kuo, C.-K.Tung, and S.H. Shieh presented a High-speed CMOS chip design for Manchester and Miller encoder. This literature [2] evolved a high-speed VLSI architecture relatively fully reused with Manchester and Miller encodings for RFID applications. This architecture was performed in 0.35-μm CMOS technology and the maximum operation frequency is 200 MHz. (Y.C. Hung, M.M. Kuo, C.K. Tung, and S.H. Shieh 2009)

The new methodology presented by Yu Hsuan Lee and Cheng Wei Pan. They implemented a fully reused VLSI Architecture of FM0/Manchester encoding using SOLS technique for DSRC applications. This paper [1] is the inspiration for this project. It proposed a promising solution for high performance fully reused VLSI architecture of FM0/Manchester encoding using similarity oriented logic simplification (SOLS) technique for dedicated short range communication. The SOLS technique improves the hardware utilization rate from 57.14% to 100% for both FM0 and Manchester encodings. (Yu-Hsuan Lee and Cheng-Wei Pan 2014)

3. CODING PRINCIPLES OF FM0, MANCHESTER AND MILLER ENCODER

3.1. FM0 ENCODING

For each input data, the FM0 code consists of two parts: one for former half cycle of clock signal, A, and the other one for later half cycle of clock signal, B. The coding principle of FM0 encoder is given below:

1) If input data is logic-0, the FM0 code must show a transition between A and B.
2) If input data is logic-1, no transition is allowed between A and B.
3) There is a transition is allocated among each FM0 code no matter what the X is.

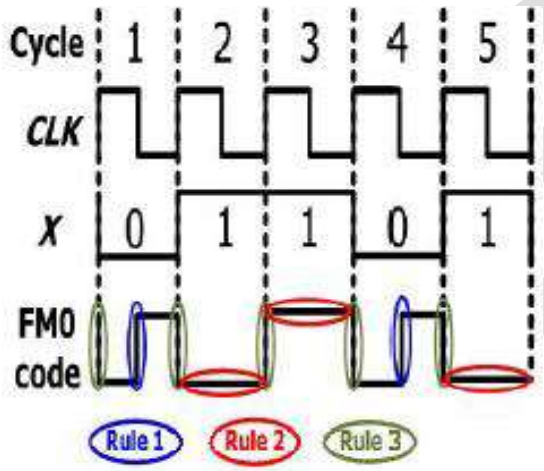

Fig.2. Example for FM0 coding

3.2. MANCHESTER ENCODING

The Manchester encoding is realized with XOR operation between clock and input signal. Manchester encoder always produces a transition between the center of each cycle. The Manchester coding example is shown in Figure. 3.

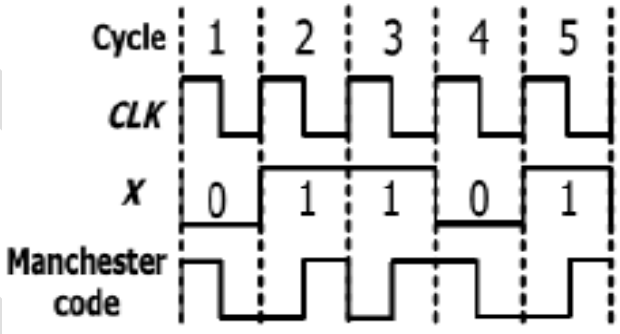

Fig. 3. Example for Manchester encoding

3.3. MILLER ENCODER

Miller encoding is also known as delay encoding. It can be used for higher operating frequency and it is similar to Manchester encoding except that the transition occurs in the middle of an interval when the bit is 1. While using the Miller delay, noise interference can be reduced.

The block diagram of Miller encoder consists of a D flip flop, T flip flop, NOT gate and XOR gate. Here the input is A and CLK. For example, if the input is 0 and the clock, given the XOR operation has done in between A and CLK, therefore 0 plus a positive edge

clock produces the output as 0. Given it to D flip flop, the clock has inverted, and after that output is given to T flip which is 0. Then the TFF is toggle FF, which produces the Miller output as 1.

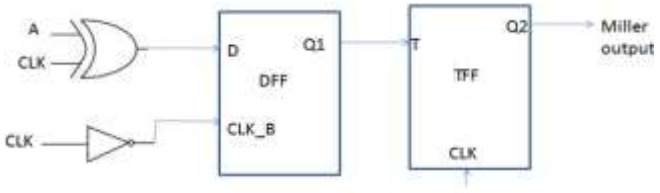

Fig.4. Block diagram of Miller encoder

4. SOLS TECHNIQUE

DSRC encoders make use of FM0, Manchester and Miller encoding techniques. Hence these encoders can be combined together to form a reusable encoder. The final circuit obtained is an integrated architecture of FM0, Manchester and Miller encoding to overcoming various drawbacks of traditional method. Such a reusable encoder of FM0 and Manchester encoder can be illustrated as shown in the figure 5.

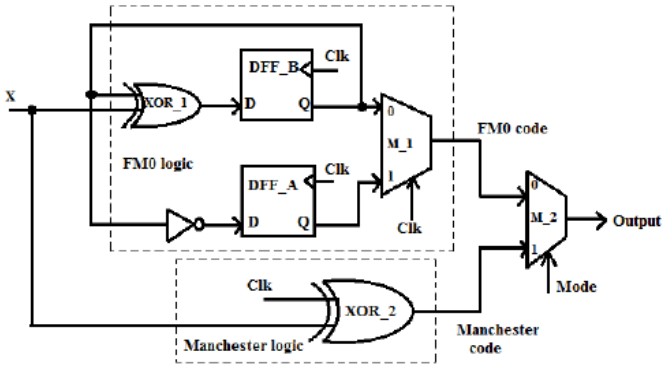

Fig.5. Hardware architecture of FM0 and Manchester encoder

The reason why FM0 encoding dissipates more power than Manchester encoding is explained as follows: The dynamic power can be given as

$$P = \gamma f C V2$$

Where γ , f , C, and V denote the switching-activity, operation frequency, equivalent capacitance of circuitry node, and supply voltage, respectively.

In existing works the coding diversity between the FM0 and Manchester encoders limits the potential to design a fully reconfigured VLSI architecture. To rectify these problems, the FM0 and Manchester and Miller encoders are designed with area compact retiming and balance logic operation sharing techniques, and if this project is implemented, it will construct a fully reused VLSI architecture with high speed and reliability for DSRC application systems.

5. IMPLEMENTATION OF THE ENCODING TECHNIQUES

To implement the project, we need two core concepts to design a fully reused VLSI architecture for FM0 and Manchester codes. These two core concepts are area-compact retiming and balance logic-operation sharing techniques. The area compact retiming relocates the hardware resource and to reduce the number of transistors. The balance logic operation sharing will efficiently combines FM0 and Manchester encodings with the fully reused VLSI architecture. Each part is individually described as follows.

5.1. Area Compact Retiming

This method is mainly used for simplifying the FM0 encoder. In the case of FM0 encoder, the state codes A(t) and B(t) are stored into separate flip flops. Thus the transition of state code only depends on B(t), the encoder needs only a single bit flip flop.

5.2. Balance logic operation sharing

This technique deals with the Manchester encoder. Generally Manchester encoding can be treated as the XORing between the clock and the input signal. It can also be treated as a multiplexer where the data and its complement is given as the data input and the clock is given as the select input. Applying the above two techniques the proposed block diagram shown in the below diagram (figure 5), which shows key modules and their inter-connections:

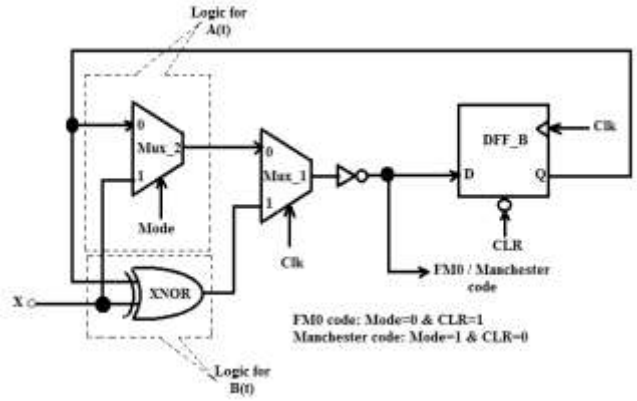

Figure 6. VLSI architecture of FM0 and Manchester encodings using two core concepts with balance computation time between A(t)/X and B(t)/X.

6. EVALUATION METHODOLOGY

PROPOSED DESIGN OF FM0, MANCHESTER AND MILLER ENCODERS

These modules are to be synthesized using Verilog HDL and implemented on FPGA. Here shows the RTL schematic diagram of FM0, Manchester and Miller encoders.

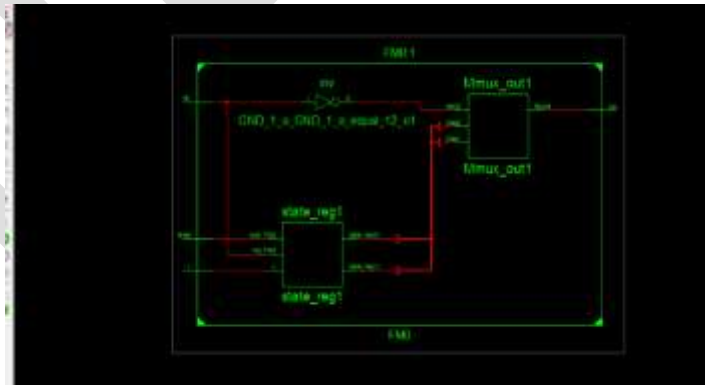

Fig.7. RTL schematic of FM0 encoder

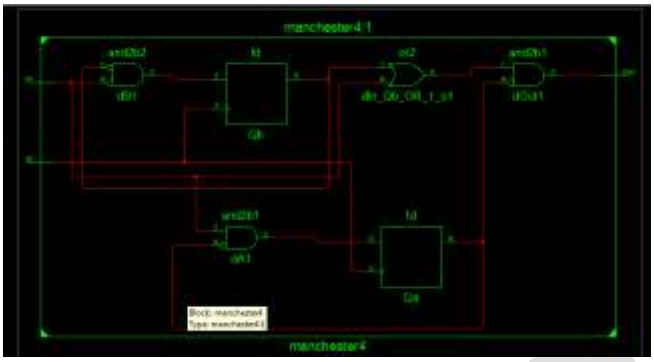

Fig.8. RTL schematic of Manchester encoder

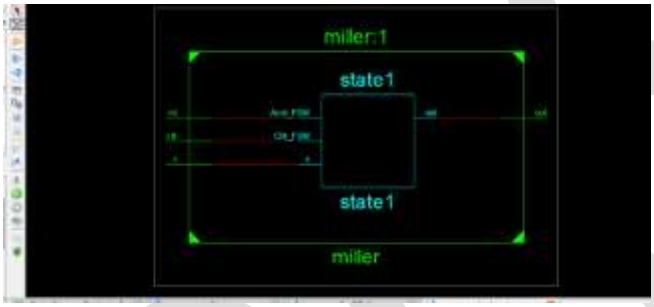

Fig.9. RTL schematic of Miller encoder

This paper adopts the proposed SOLS technique to construct a fully reused VLSI architecture for FM0, Manchester and Miller encodings. Every logic component of this design is utilized in FM0, Manchester and Miller encodings. None of them is wasted in either encoding function; therefore, the HUR of the proposed VLSI architecture is as high as 100%. The performance evaluation classifies the electrical characteristics into the operation frequency, the power consumption, and the area.

The SOLS technique integrates Manchester, FM0 and Miller encodings into a fully reused hardware architecture. Obviously, the coding procedure of FM0 is more complex than that of Manchester. The data path of Manchester encoding restricted to that of FM0 encoding. Then, the operation frequency of Manchester encoding is also limited by that of FM0 encoding. Our work targets at an efficient integration of hardware devices for Manchester, Miller and FM0 encoding instead of operation frequency and power consumption. Generally, more coding methods a hardware architecture can support, more hardware devices it requires. A performance evaluation is given under identical conditions for a more objective evaluation. A building block that can perform FM0, Manchester and Miller encodings is considered an evaluation platform.

PERFORMANCE EVALUATION ON FM0, MANCHESTER AND MILLER ENCODINGS

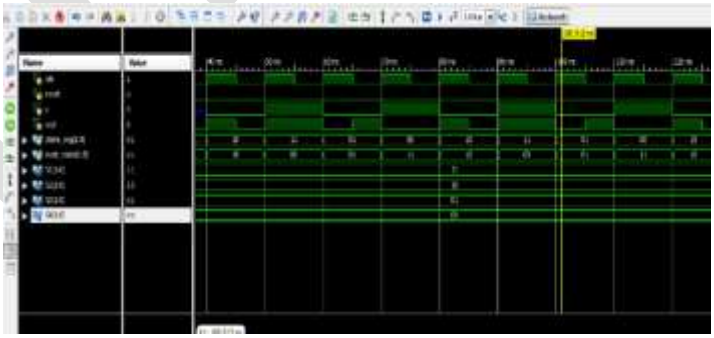

Fig.10. Simulation results for FM0 encoding

Fig.11. Simulation results for Manchester encoding

Fig.12. Simulation results for Miller encoding

The simulation result for FM0 encoding is shown in Figure 10. When the input X is 0, and the CLK is given as a rising edge which produces a transition in middle of that FM0 cycle. When the input X is 1, there is no transition in the FM0 cycle. Also there is a transition in among each FM0 code. The simulation result for Manchester encoding is shown in Fig 11. The Manchester encoding is realized with a XOR operation for CLK and *X*. The clock always has a transition within one cycle, and so does the Manchester code no matter what the *X* is. The simulation results for Miller encoding is shown in Figure 12. The input X plus a positive edge clock produces the output as 0 .

5. CONCLUSION

The coding diversity between FM0, Manchester and Miller codes causes the limitation on designing VLSI architecture. Hence, the fully reused VLSI architecture using area compact retiming and balance logic operation sharing technique for both FM0 and Manchester encodings is adapted. The realization of this project will solve most of the difficulties discussed above and in the problem definition section. This project will have following results:

1. Improved hardware utilization rate (HUR)
2. Area optimization
3. reduced power consumption
4. Lower latency

The coding diversity between FM0, Manchester and Miller encodings causes the limitation on hardware utilization of VLSI architecture design. The area compact retiming and balance logic operation sharing techniques eliminates the limitation on hardware utilization. Area compact retiming concept relocates the hardware resource and to reduce the number of transistors effectively. The Balance Logic operation sharing technique combines FM0 and Manchester encodings with the identical logic components to produce balanced computation time. Every component is active in both FM0 and Manchester encodings and it will greatly improve the

hardware utilization rate to 100% and reduce the power consumption. The FM0 and Manchester encoders are designed with these techniques to achieve high speed and fully reconfigured VLSI architecture for application system. In future the design can be implemented using high performance FPGA devices.

REFERENCES:

[1] Yu-Hsuan Lee and Cheng-Wei Pan, "Fully Reused VLSI Architecture of FM0/Manchester Encoding Using SOLS Technique for DSRC Applications," *Member, IEEE, IEEE trans. in Very Large Scale Integr. (VLSI) Syst., vol. pp, issue 99, Feb 2014.*

[2] Y.C. Hung, M.-M. Kuo, C.-K. Tung, and S.-H. Shieh, "High-speed CMOS chip design for Manchester and Miller encoder" *in Proc. Intell. Inf. Hiding Multimedia Signal Process., Sep. 2009, pp. 538–541*

[3] A. Karagounis, A. Polyzos, B. Kotsos, and N. Assimakis, " 90nm Manchester code generator with CMOS switches running at 2.4 GHz and 5 GHz" *in Proc. 16th Int. Conf. Syst., Signals Image Process., Jun. 2009, pp. 1– 4*

[4] P. Benabes, A. Gauthier, and J. Oksman, "A Manchester code generator running at 1 GHz," in *Proc. IEEE, Int. Conf. Electron., Circuits Syst., vol. 3. Dec. 2003, pp. 1156–1159.*

[5] M. A. Khan, M. Sharma, and P. R. Brahmanandha,"FSM based Manchester encoder for UHF RFID tag emulator ," *in Proc. Int. Conf. Comput., Commun. Netw.,Dec. 2008, pp.1–6*

[6] Mohanraj S. and Dr. Sudha S, Professor, "Low Power VLSI Architecture of Encoder for Downlink Applications," *Aust. J. Basic & Appl. Sci., 9(15): 43-51, 2015.*

[7] Daniel Jiang, Vikas Taliwal, Andreas Meier, Wieland Holfelder, Ralf Herrtwich, "*Design of 5.9GHz DSRC based Vehicular Safety Communication," DaimlerChrysler Research and Technology North America, Inc.*

[8] F. Ahmed-Zaid, F. Bai, S. Bai, C. Basnayake, B. Bellur, S. Brovold, *et al.*, "Vehicle safety communications—Applications (VSC-A) final report," *U.S. Dept. Trans., Nat. Highway Traffic Safety Admin., Washington, DC, USA, Rep. DOT HS 810 591, Sep. 2011.*

[9] J. B. Kenney, "Dedicated short-range communications (DSRC) standards in the United States," *Proc. IEEE, vol. 99, no. 7, pp. 1162–1182, Jul. 2011.*

[10] M. A. Khan, M. Sharma, and P. R. Brahmanandha, "FSM based FM0and Miller encoder for UHF RFID tag emulator," in *Proc. IEEE Adv. Comput. Conf.*, Mar. 2009, pp. 1317–1322.

[11] J. Daniel, V. Taliwal, A. Meier, W. Holfelder, and R. Herrtwich,"Design of 5.9 GHz DSRC-based vehicular safety communication," *IEEE Wireless Commun. Mag.*, vol. 13, no. 5, pp. 36–43, Oct. 2006.

[12] J.-H. Deng, F.-C. Hsiao, and Y.-H. Lin, "Top down design of joint MODEM and CODEC detection schemes for DSRC coded-FSK systems over high mobility fading channels," in *Proc. Adv. Commun. Technol.* Jan. 2013, pp. 98–103.

[13] I.-M. Liu, T.-H. Liu, H. Zhou, and A. Aziz, "Simultaneous PTL buffer insertion and sizing for minimizing Elmore delay," in *Proc. Int. Workshop Logic Synth.*, May 1998, pp. 162–168.