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A NEW SIMPLIFIED ASYMMETRICAL MULTILEVEL INVERTER TOPOLOGY WITH FUNDAMENTAL SWITCHING CONTROL

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***Abstract*—** Multilevel inverters have been a widely accepted solution for high voltage and high power applications. Their performance is highly superior to that of conventional two-level inverters due to reduced harmonic distortion, lower electromagnetic interference, and higher dc link voltages. Their main disadvantage is their complexity, requiring a great number of power devices and passive components, and a rather complex control circuitry. In this paper a new inverter topology for generation of fifteen levels of output voltage with reduced number of switches is presented. This topology requires fewer components compared to existing inverters (particularly in higher levels) and requires fewer carrier signals and gate drives. The inverter is controlled by fundamental switching scheme to have a minimum power loss as compared to PWM scheme. The performance of the proposed topology is demonstrated through the simulation in MATLAB/SIMULINK platform and the results demonstrating the operation of the proposed topology as multilevel inverter is presented.

***keywords*—** Multilevel inverter, power electronics, fundamental switching.

INTRODUCTION

Multilevel power conversion was first introduced more than two decades ago. The general concept involves utilizing a higher number of active semiconductor switches to perform the power conversion in small voltage steps. There are several advantages to this approach when compared with the conventional power conversion approach [1]. Another important feature of multilevel converters is that the semiconductors are wired in a series-type connection, which allows operation at higher voltages. However, the series connection is typically made with clamping diodes, which eliminates overvoltage concerns. Furthermore, since the switches are not truly series connected, their switching can be staggered, which reduces the switching frequency and thus the switching losses. One clear disadvantage of multilevel power conversion is the higher number of semiconductor switches required. It should be pointed out that lower voltage rated switches can be used in the multilevel converter and, therefore, the active semiconductor cost is not appreciably increased when compared with the two level cases. However, each active semiconductor added requires associated gate drive circuits and adds further complexity to the converter mechanical layout. Another disadvantage of multilevel power converters is that the small voltage steps are typically produced by isolated voltage sources or a bank of series capacitors. Isolated voltage sources may not always be readily available, and series capacitors require voltage balancing [2]. Some applications for these new converters include industrial drives, flexible ac transmission systems (FACTS), and vehicle propulsion. One area where multilevel converters are particularly suitable is that of renewable photovoltaic energy that efficiency and power quality are of great concerns for the researchers. There are several classical topologies of inverters that are reported by the researchers [3]. Multilevel inverters with reduced number of switches has also become a popular area. Inverter topologies where not all the semiconductor switches involved in output generation are also presented by the researchers [4].

This paper presents an overview of a asymmetrical fifteen level inverter topology with reduced number of switches. The dc sources are assigned with magnitude arranged in a binary fashion. The inverter is divided into two parts namely level and polarity generator whose function is to generate the necessary levels and reversing of the polarity respectively. The inverter is switched with fundamental switching strategy and the generation of control pulses is analyzed. The proposed topology is simulated using Sim power system toolbox of matlab and the results are presented.

POWER STAGE

Fig. 1 shows the power circuit of the proposed 15-level inverter topology. In conventional multilevel inverters, the power switches are operated to produce a high- frequency waveform in both positive and negative polarities. However there is no need to use all the switches for production of bipolar levels. This is the basic idea that has been put into practice by the proposed topology. The output voltage is synthesized by two stages namely level generator which is responsible for the generation of levels requires in positive polarity and secondly the polarity generator stage which is responsible for generating the polarity of the output voltage. The power semiconductor switches employed in the level generator should have high switching frequency capability for generating the required

levels. Whereas the power switches employed for polarity generation operates at the line frequency. The positive levels generated by the level generator is fed to a full-bridge inverter (polarity generator) which will generate the required polarity of the output voltage. In the proposed topology fundamental switching scheme is employed in which no high frequency PWM is required [5]. The operating modes of the inverter is as shown in Fig. 4. For the simulation Vpu is considered to be 25V. The required output positive voltage levels produced by the level generator are generated as follows:

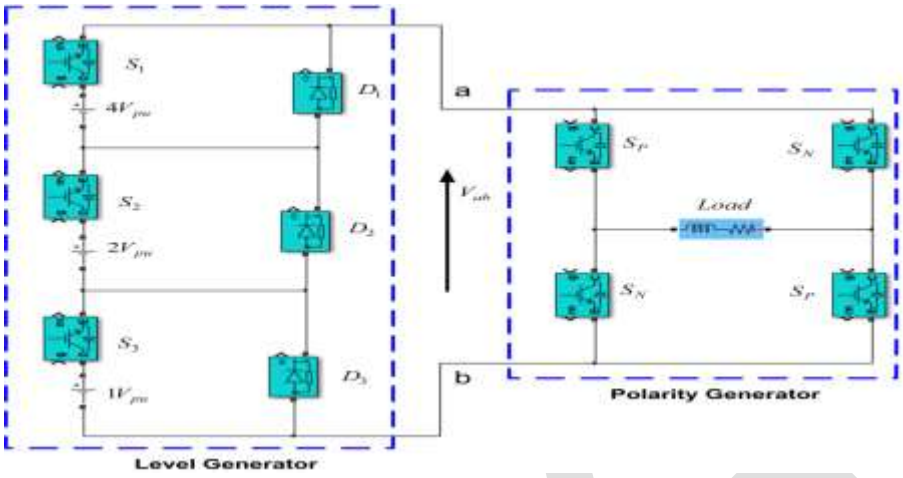

Fig. 1:Proposed asymmetrical 15-level inverter topology.

State 1: V_{ab} = 0V -To obtain this state of level 0 all the switches are turned OFF.

State 2: V_{ab} = 25V -To obtain this state of level 1 switches S3, SP are ON and remaining switches are OFF.

State 3: V_{ab} = 50V -To obtain this state of level 2 switches S2, SP are ON and remaining switches are OFF.

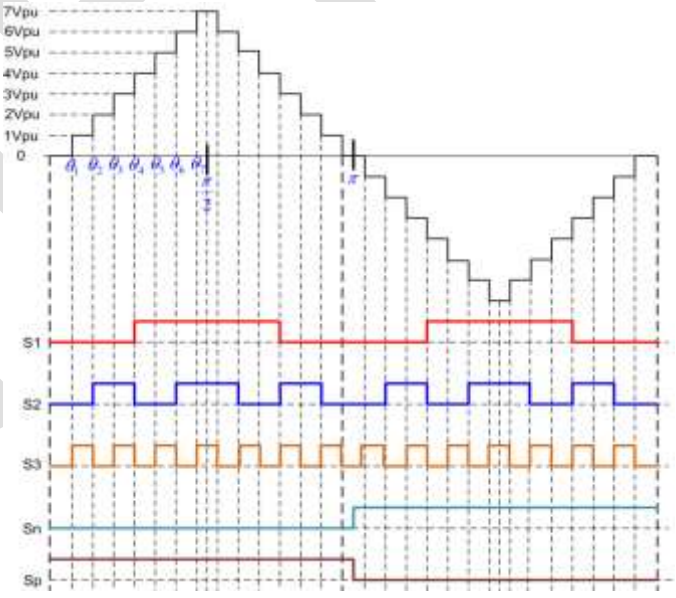

Fig.2: Stepped-voltage waveform consists of the output of proposed inverter topology.

State 4: V_{ab} = 75V -To obtain this state of level 3 switches S3, S2, SP are ON and remaining switches are OFF.

State 5: V_{ab} = 100V -To obtain this state of level 4 switches S1, SP are ON and remaining switches are OFF.

State 6: V_{ab} = 125V -To obtain this state of level 5 switches S1, S3, SP are ON and remaining switches are OFF.

State 7: V_{ab} = 150V -To obtain this state of level 6 switches S1, S2, SP are ON and remaining switches are OFF.

State 8: V_{ab} = 175V -To obtain this state of level 7 switches S1, S2, S3, SP are ON and remaining switches are OFF.

Fig. 2 shows the Stepped-voltage waveform consists of the output of proposed inverter with switching angles for 10 IGBTs. According to the operating states and the output voltage level to be generated the gate pulses for all the switches are derived. The switching angles are used to obtain the switching pulses using a sine wave reference as shown in Fig. 3.

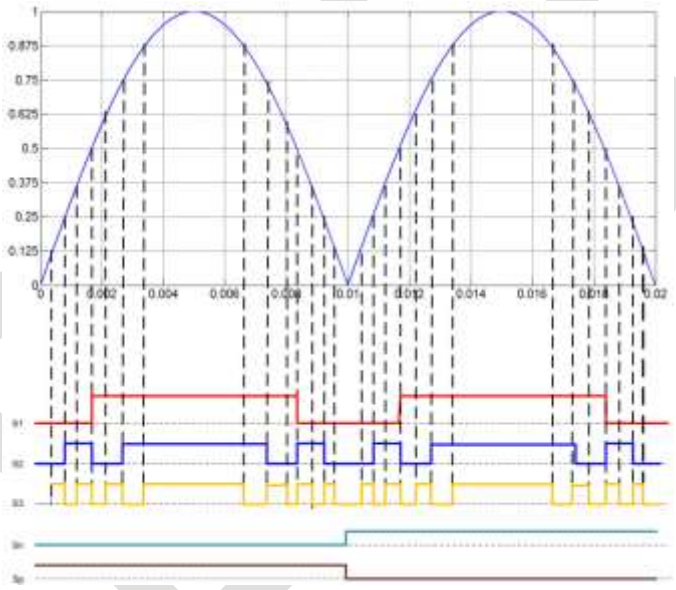

Fig. 3:Reference sine wave and gating signals.

The logic function for the switches is derived from the above waveform as follows. Where V_{ref} is the reference sinusoidal wave.

$$S_1 = \left\{1 \rightarrow \left(V_{ref} > 0.5\right)\right.$$

$$S_2 = \left\{1 \rightarrow \left(\left(0.125 < V_{ref}\right) * \left(V_{ref} < 0.5\right)\right) + \left(0.75 < V_{ref}\right)\right.$$

$$S_3 = \left\{1 \rightarrow \left(\left(0.125 < V_{ref}\right) * \left(V_{ref} < 0.25\right)\right) + \left(\left(0.375 < V_{ref}\right) * \left(V_{ref} < 0.5\right)\right)\right.$$

$$+ \left(\left(0.625 < V_{ref}\right) * \left(V_{ref} < 0.75\right)\right) + \left(0.875 < V_{ref}\right)\right.$$

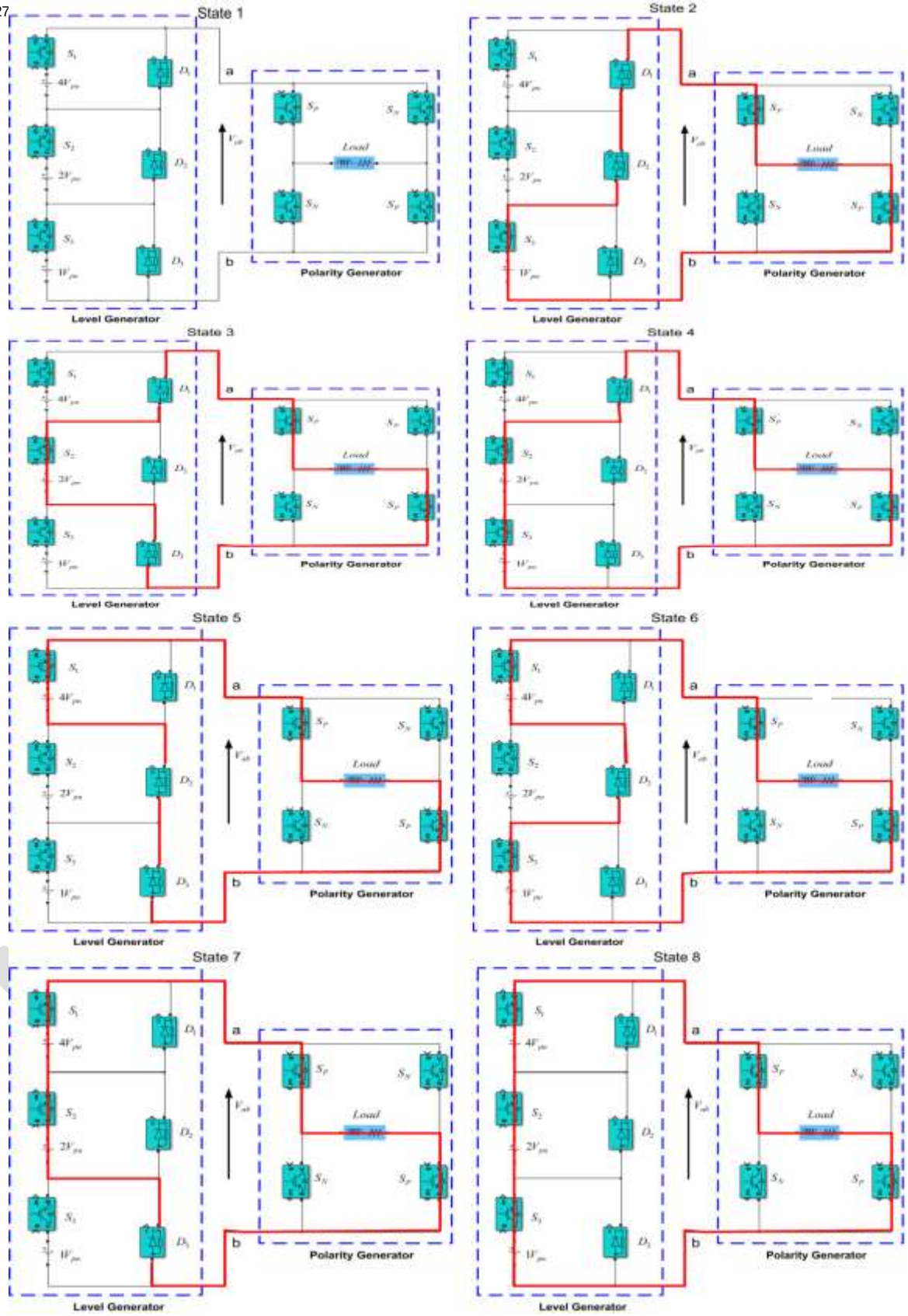

Fig.4: Operating states of the proposed inverter.

SIMULATION RESULTS

In order to verify the proposed inverter topology simulations are carried out on MATLAB/SIMULINK platform. Fig. 5 shows the implementation of the power circuit and the control scheme in Matlab/Simulink.

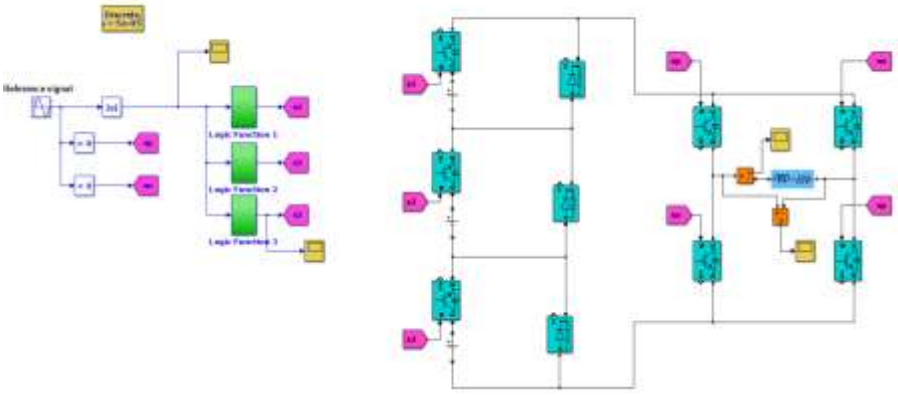

Fig.5: Simulink diagram of the proposed inverter topology implemented in Matlab.

The output waveforms of the inverter feeding a resistive load of 150Ω is shown in Fig. 6. The %THD of the current is 6.63 without any filtering.

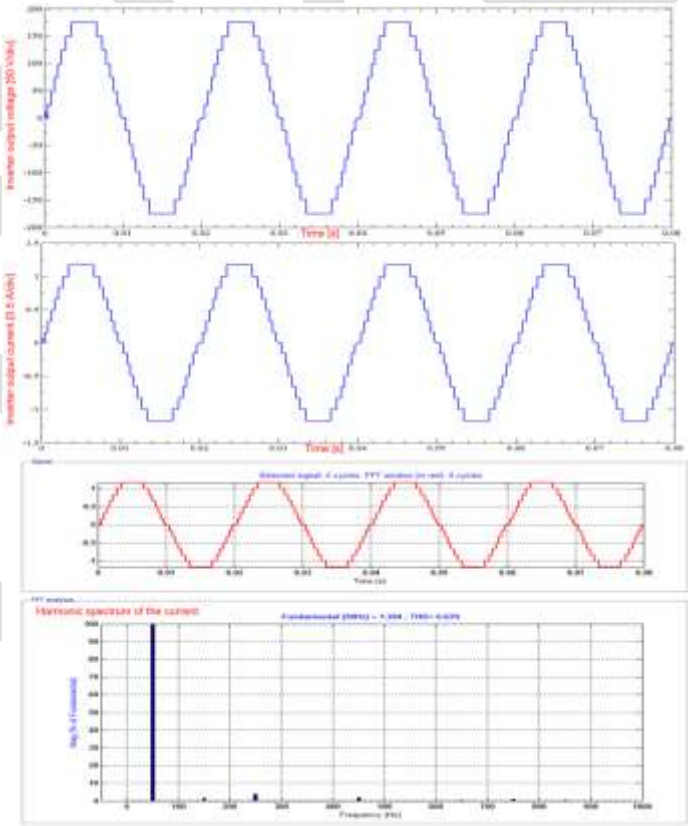

Fig. 6: Output waveform of the inverter feeding resistive load.

The output waveforms of the inverter feeding a resistive-inductive load of 150Ω and 50mH is shown in Fig. 7. The %THD of the current is 4.3 which is in comply with the IEEE 519-1992 standard.

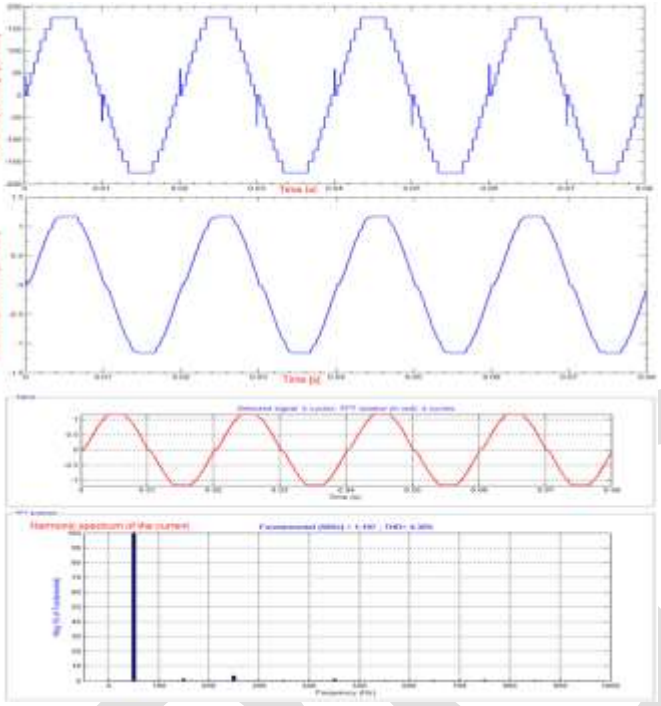

Fig.7: Output waveform of the inverter feeding resistive-inductive load.

TABLE I
COMPARISON OF COMPONENTS REQUIRED FOR PROPOSED TOPOLOGY WITH OTHER POPULAR INVERTERS

	Neutral point clamped	*Cascaded*	*Flying capacitor*	*Proposed*
Main switches	12	12	12	10
Main diodes	12	12	12	10
DC bus capacitors	6	3	6	3
Total number	30	27	30	23

Table I shows the comparison of number of components required for the proposed topology with other popular inverters. It can be seen that the proposed inverter requires less number of components for same level generation and hence has a better efficiency and performance.

CONCLUSION

In this paper a new inverter topology which has superior performance, offering improved output waveforms and lower THD over conventional topology in terms of number of switches required, cost, control system and reliability. The proposed topology and fundamental switching scheme result in a near-sinusoidal waveform. As a result, a significant reduction of output voltage THD is obtained, and the modulation scheme has been discussed in detail. The complexity of PWM for this topology is low since it only needs to generate PWM gating pulses for generation of positive level only. The results obtained clearly shows the effectiveness of the proposed topology as a multilevel inverter with reduced number of switches as a promising topology for multilevel power conversion.

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