Estimation of Software Reliability on the Basis of Bits for Embedded System

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Abstract - As software in an embedded system has taken responsibility for controlling both software, and hardware components, the importance of estimating more accurate reliability for such software has been increased. To estimate the reliability of software, we use software which is a of collection of bits so while analyzing of system the software reliability in terms of bit it gives better result comparison to software reliability in terms of time analysis. The software is the collection of bits and during the execution bits are processed and it defines the level of execution. While we analyze the bit we justify the performance of system and estimate the reliability in a better way. However, many researchers have developed software reliability models assuming that software failures are caused by only software faults, which might lead to inaccurate reliability estimation.

In this paper a Software Reliability model is proposed in which the performance of the existing reliability model is improved.

Keywords – Software Reliability, Embedded Software Reliability, Embedded System, Bit-rate, Clock speed, TPT, BSC.

INTRODUCTION

Software is safety-critical if a failure can directly cause loss of human life or have other catastrophic consequences [1], examples include systems that control aircraft, nuclear reactors, and medical devices. Clearly the reliability and correctness of such software needs to be demonstrated with high assurance, and regulatory agencies in safety-critical industries typically require system providers to meet stringent certification requirements [2]-[4].

Software reliability is defined as the probability of the failure-free operation of a software system for a specified period of time in a specified environment [4]. For mission critical systems, redundancy techniques are commonly applied to achieve high reliability. For embedded systems consisting of software and hardware components, redundancy can be achieved by applying extra copies of these components (in parallel) to handle the system workloads [5]-[7]. Various software reliability growth models (SRGMs) exist to estimate the expected number of total defects (or failures) or the expected number of remaining defects (or failures). Some well known SRGMs are Goel model (1985), Goel and Okumoto model (1979), Kececioglu model (1991), Musa and Ackerman model (1989), Musa et al. Model (1987), Yamada et al. Models (1983, 1985, 1986) etc [8]-[18]. These models have some limitations. Each model can provide good result for a particular data set, but no model is good for all data sets [19]-[28].

In this paper we present a software reliability model which is successfully used to solve the reliability modeling problem according to embedded software size and its execution rate, that are having limited number of bits.

1. EMBEDDED SOFTWARE RELIABILITY

Software is a set of instruction that have several bits to elaborate the bits (0/1). Embedded software are basically design for a specific task for example press, air-condition, aircraft etc. that have a specific length, and can be countable in bits, or during execution we can justify each and every clock cycle for its bits involved. According to clock speed we can also define its reliability of instructions per cycle execution, if we justify the probability of failure free operation then we can easily estimate the reliability problem.

Reliability is the function of time and probability in hardware reliability calculation but software is not having the wear out time so we can say that a software may not fully depend upon time so estimation of software reliability is quite crucial in terms of time. While we consider bit rate and probability of its failure then we can easily derive the reliability in form of total probability theorem and Bernoulli Trials. So the reliability model with respect to bits can be processed data for failure free operation per clock, and estimate the failure per cycle until the whole execution completes.

1.1 SOFTWARE RELIABILITY IN PER CYCLE EXECUTION

Let a system that have ‘n’ bits that execute in one clock cycle and each bit having its own failure probability, where P_f is failure probability per bit and R is reliability. According to the reliability theory reliability is compliment of probability of failure occurred, so reliability occurrences per bit in each cycle is:

$$R(n) = 1-P_f(n) \tag{1}$$

The above expression shows the reliability per bit, where R(n) is the reliability of n^{th} bit, $P_f(n)$ is the probability of failure of n^{th} bit, n is the number of bit per cycle. In case of over-all reliability of n bits in a clock cycle, the execution fails if any bit is missing in the clock. The over-all reliability of ‘n’ bit’s is:

$$F(R_n)=R(1)UR(2)\ldots.UR(n) \tag{2}$$

The above expression shows that the over-all reliability is the union of the all individual bit reliability.

1.2 SOFTWARE RELIABILITY IN TERM OF TOTAL PROBABILITY THEOREM (TPT)

Let a system clock cycle execute 8 bits data (it can have ‘n’ bits), and all bits having its own failure probability ($B_1, B_2, B_3, B_4, B_5, B_6, B_7, B_8$), and the shaded portion shows the probability of failure for clock.
See figure 1.

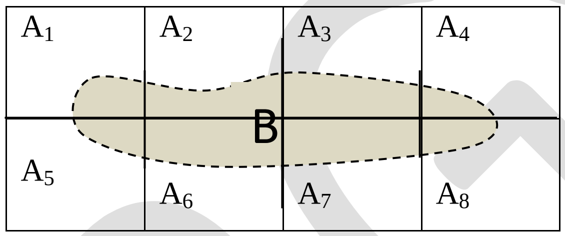


Figure 1:- A system clock having 8 bit.

The shaded portion represents ‘B’, and $B = B_1 + B_2 + B_3 + B_4 + B_5 + B_6 + B_7 + B_8$. Where $B_1, B_2, B_3, B_4, B_5, B_6, B_7, B_8$ is the failure probability of each bits in clock and A_1 to A_8 are mutually exclusive or disjoint event (that bits are process) of clock ‘C’. So $C = A_1 + A_2 + A_3 + A_4 + A_5 + A_6 + A_7 + A_8$.

The total probability theorem let us to compute the probability of an event occurring by enumerating all the different condition that can occur which gives the probability of failure that occurs in the cycle execution ‘P_{fc}’.

So ,

$$P_{fc} = P(B \cap C) \tag{3}$$

$$P_{fc} = P(B\cap(A_1UA_2\ldots UA_8))$$

$$P_{fc} = P((B\cap A_1)U(B\cap A_2)..U(B\cap A_8))$$

$$P_{fc} = \textstyle\sum_i^8 P(B \cap Ai)$$

$$P_{fc} = \textstyle\sum_i^8 P(B \mid Ai)\, P(Ai) \tag{4}$$

This give the failure probability occurs in clock execution.

1.3 RELIABILITY IN TERM OF BERNOULLI TRIALS

For ‘n’ bits, data are processed in per clock cycle, and having failure probability ‘P_e’ for each bits, so the probability of successes is:

$$Q = 1- P_e \tag{5}$$

Failure probability in term of Bernoulli Trials is the probability of achieving exactly k failure in *n* trials.

Let the probability for ‘k’ failure in ‘n’ bits data process, and ‘p_c’ is the failure probability of clock cycle.

$$P_c = \binom{n}{k} P_e^{\,k}\ (Q)^{n-k} \tag{6}$$

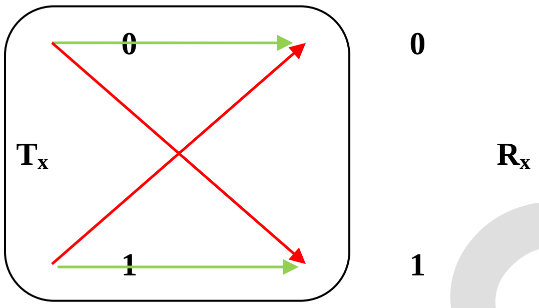
$$P_c = \binom{n}{k} P_e^{\,k}\ (1- P_e)^{n-k}$$

$$P_c = \frac{n!}{k!(n-k)!} P_e^{\,k}\ (1- P_e)^{n-k} \tag{7}$$

Bernoulli trials in term of binary symmetric channel (BSC), Lets probability for error per bit is P_e

$P(0|1) = P(1|0) = P_e$ (red) $\longrightarrow$

$P(0|0) = P(1|1) = 1 - P_e$ (green) $\longrightarrow$



Data process

Figure 2: Binary Symmetric channel

According to Bernoulli trials P_c is the define for 'n' bit clock size having 'k' errors. But if any one bit may miss, that cause failure. That minces for failure free operation 'k' have the minimum value '1'. So for 'k = 1' P_c will be.

$$P_c = \binom{n}{1} P_e^{\,1}(1- P_e)^{n-1} \tag{8}$$

For reliability Rc of a clock if there failure occurrence is P_c then according to reliability theorem.

$$R_c = 1 - P_c \tag{9}$$

So,

$$R_c = 1 - \binom{n}{1} P_e^{\,1}(1- P_e)^{n-1} \tag{10}$$

2. RELATIONSHIP BETWEEN RELIABILITY AND CLOCK SPEED

The clock cycle is the time between two adjacent pulses of the oscillator that sets the tempo of the computer processor. The number of these pulses per second is known as the clock speed, which is generally measured in Mhz (megahertz, or millions of pulses per second) and even in Ghz (gigahertz, or billions of pulses per second).

A system may provide variable response while we are varying the clock speed, this may affect the reliability of the system in different terms (ex.- In term of failure, in term of utility, in term of cost or optimization).

A clock speed may cause failure in execution of the bits. If the clock speed is higher than the band limit of the system then due to internal capacitance a system can't operate beyond the clock speed (ex. ARM TDMI 7 operation is crucial above 30MHz). If the frequency is beyond its range then due to extra attenuation (the cutoff frequency at which the current gain drops by 3 decibels (70% amplitude)) the bits can be missed and failure occur in the system, while increasing the frequency we observe that the fault rate will increases.

When a system operate at low frequency, then it can't provide optimum work due to low speed, there cost utility factor is effective which reduces the reliability as a cost effective function (ex. below 1 MHz operation is better to use other low operating frequency microcontroller then ARM TDMI 7, it increase the product manufacturing cost, ultimately it reduces the reliability in term of cost and speed).

For maximum reliability a system may operate at its desire operating range (ex. ARM TDMI 7 provide optimum response in 1 MHz to 30MHz). In the desire range current gain drops is less then 3 decibels (amplitude grater then 70%).

The above discussion gives a relative graph in between reliability and clock cycle.

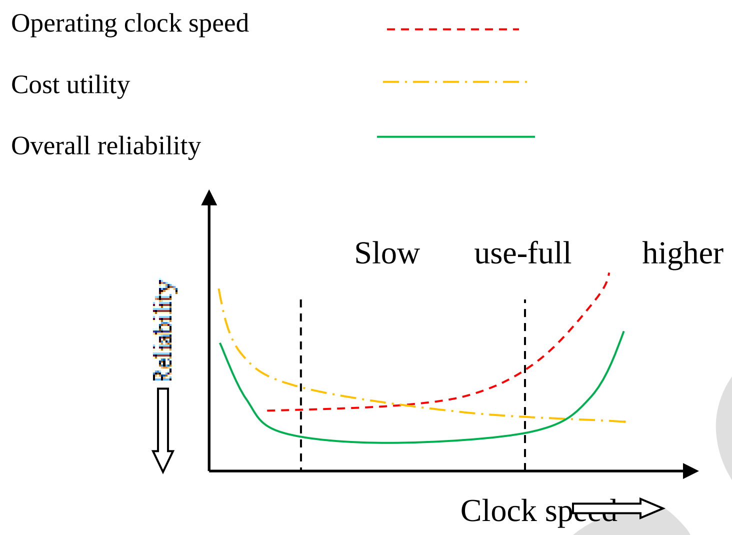


Figure 3: Reliability versus clock speed graph

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CONCLUSION

In this paper we present a software reliability model in terms of bits which is more efficient to estimate the software reliability. A hardware reliability is fully depend upon time so its reliability versus time graph is much suitable to demonstrate in bath tub curve while a software reliability can't because software does not have wear out time. In case of clock speed versus reliability graph, the bath tub curve achieves better reliability in comparison to the time versus failure/reliability graph. Due to fully dependency of software on bits we can easily demonstrate reliability in terms of bits and it gives a better estimation for software reliability.

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