International Journal of Engineering Research and General Science Volume 4, Issue 1, January-February, 2016
ISSN 2091-2730

A Review On Power Effective Memristor Based SRAM Using MTCMOS Technique

Miss. Reena S. Wasankar, Prof. Ashish E. Bhande

HVPM COET,Amravati, Maharashtra,India, reenawasankar@rediffmail.com, 9960290082.

Abstract— In recent years demand of low power devices is increasing and the reason behind this is scaling of CMOS technology. Due to the scaling, size of the chip decreases and number of transistor in system on chip (SOC) increases and this phenomenon also apply on memories that are used in SOC. Generally the number of transistors used in chip to store data is more as compared to the number of transistors used for other function. So in future the need of low power memories is increasing and to design low power memories leakage power is attentive parameter to design low power devices because it plays a major role in increasing the total power consumption of the devices.

In this project, MTCMOS (Multi Threshold CMOS) technique is used recently it is very famous in academia and industry. It is a power reducing technique that helps in reducing leakage power in the SRAM by turning of the inactive circuit domains. Designing and calculation of parameters of simple SRAM, Memristor based SRAM and MTCMOS based Memristor SRAM has been done with CMOS Design tool and that will do at 45 nm technology.

Keywords— Low power, Speed, Non Volitle Memory,CMOS, Memristor,MTCMOS,SRAM.

INTRODUCTION

VLSI technology has got enormous in recent years and scaling of chip in VLSI technology decreases very rapidly whose result is that complexity and density of chip has increased. So the low power devices are the first choice of VLSI designers and these low power devices fulfill the goal of the systems. The value of power that can be dissipated from the power supply mathematically is represented as-

$$P_{av} = \left[\left(\frac{1}{T}\right)\int_0^T Idt\right] \times V \quad (1)$$

Where *Pav* is average power, T is time, I is current and V is voltage. In future demand of battery operated portable systems such as mobile phones, laptops, PDA tools and other handheld devices in electronic field increases. The major concern is that portable systems use power then low power need of low power system in electronic field increases and these systems to store their data use memories. Memory define as it collection of storage cell with proper input and output and one type of these memories is SRAM. In SRAM cell does not need refreshing technique this quality of SRAM indicate by the static word and it is volatile in nature that means when power is plugged in, data is stored and as the power is plugged out data will get lost other qualities of SRAM is it use number of transistors to store a single bit in system on chip (SOC)
and it reduces the delay between the processor and memories. These advantages of SRAM are used to design portable systems that is why low power SRAM is very demand full in handheld devices therefore in this paper designed MTCMOS based Memristor SRAM. Memristor and MTCMOS have been used to designed low power SRAM. Memristor was invented by Leon O. Chua in 1971 and according to Chua Memristor is a fourth missing, two terminal passive elements with variable resistance also called as memristance that give relation between flux (Φm) and charge (q). Memristor is defined as a two terminal non-volatile device in which the magnetic flux (Φm) between the terminals is a function of the amount of electric charge q that has passed through the device and it is denoted by M and its unit is Ω and mathematically represented as-

$$M(q) = \frac{d\varphi m}{dq} \quad (2)$$

Where M is the Memristor, Φm is the magnetic flux and q is the charge. First Memristor was manufactured in HP labs by the R. Stanley Williamsin 2008. Memristor is a new type of device that can be used to design memristive system, devices and memories that can be proved by the mathematical models and that models should be accurate in terms of behavior of physical devices. In this paper also apply MTCMOS technique on Memristor based SRAM it is a power switch technique and use sleep transistors which improves the speed of the devices and decrease the power remarkable.

Literature Review:

Thangamani.V [2] presented by the approach to design memristor based nonvolatile 6-T static random access memory (SRAM) and analysis the circuit performance with conventional 6-T SRAM cell in order to prove the parameter optimizations. Then we address the memristor-based resistive random access memory (MRRAM) which is similar to that of static random access memory (SRAM) cell and we compare the nonvolatile characteristics of MRRAM with SRAM cell.

Uma Nirmal, Geetanjali Sharma, Yogesh Sharma [3] presented by the main objective is to provide new low power solution for Very Large Scale Integration (VLSI) designers. MTCMOS is an effective circuit-level technique that provides a high performance and low-power design by utilizing both low and high-threshold voltage transistors. MTCMOS technique has been proposed in this paper and the proposed technique has small power dissipation as compared to CMOS technique. Simulations based on BSIM 3V3 180nm CMOS technology. It shows 4 bit adders of the proposed technique have low power dissipation as compared CMOS technique.

Nobuaki Kobayashi, Ryusuke Ito and Tadayoshi Enomoto [4] presented by the static random access memories (SRAMs) having high "read" and "write" margins, and a small standby power (*P*ST) are needed for use in low supply voltage battery driven portable systems. The decrease in MOSFET sizes increases not only leakage currents, but also threshold voltage variation that results in smaller margins. To solve these problems a very small circuit called a "Selfcontrollable Voltage Level (SVL)" circuit] was used in the newly developed (dvlp.) SRAM. The dvlp. SRAM succeeded in increasing margins, reducing the standby power and lowering a supply voltage (*V*DD).

Farshad Moradi and Jens K. Madsen [5] presented by a novel 7T-SRAM cell for ultra-low power applications is proposed. The proposed SRAM cell is fully functional at subthreshold voltages down to VDDmin=200mV. In this technique, separate read/write bitlines and wordlines are used that makes read and write operation independent. The 7TSRAM cell proposed in this paper, improves static read noise margin, write margin, and write time by 2.2X, 27%, and 6% in comparison to the standard 6T-SRAM cell. The 7T-SRAM cell proposed in this paper, improves write margin of the conventional 7T-SRAM cell, as well. The proposed 7T-SRAM cell is designed in 65nm CMOS technology**.**

Mika Kutila, Ari Paasio and Teijo Lehtonen [6] presented by the 8T SRAM and 6T SRAMmemory cells are compared in order to establish guidelines for choosing SRAM cell constructions for NTC systems. 8T SRAM is traditionally concerned as a more reliable memory cell, but we have managed to design 6T SRAM which executes read operation with an acceptaple reliability; read being the most vulnerable operation of conventional 6T SRAM cell. Also, our 6T SRAM cell has 31% smaller area and smaller power consumption.

Amit Grover [8] presented by the motivation of reduction of the dynamic power in SRAM memory and focuses on the analysis in terms of power dissipation, delay and area of the 7-transistor SRAM memory cell at 90 nm technologies by using the Tanner tool. The article targets towards short circuit power dissipation as well as switching power dissipation. The circuit is characterized by using the 90 nm technology which is having a supply voltage of 1.0 volts and threshold voltage is 0.3 volts.

Proposed Work :

CMOS technology is used for low power devices. Due to this, size of the chip decreases and number of transistor in system on chip (SOC) increases and this phenomenon also apply on memories that are used in SOC

SRAM (Static Random Access Memory) is a type of memory that provide a link with CPU and designing of SRAM is very critical because it takes large part of power and area therefore to achieve low power SRAM we have designed Memristor based SRAM**.** Memristor is a forth missing non-linear resistor which acts as memory and it improves the power and speed.

MTCMOS (Multi Threshold CMOS) technique is used, recently it is very famous in academia and industry. It is a power reducing technique that helps in reducing leakage power in the SRAM by turning of the inactive circuit domains.

A) Memristor based SRAM

Electrical scheme of the proposed SRAM cell is shown in Fig.1(a). Two memristors are acted as memory element. The arrangement is in such a way that during write cycle, they are connected in parallel but in opposite polarity and during read cycle, they are connected in series. These connections are recognized by two NMOS pass transistors T1 and T2. A third transistor T3 is used to isolate a cell from other cells of the memory array during read and write operations. The gate input of T3 is the Comb signal which is the OR of RD (Read) and WR (Write) signals. RD is set to the LOW state and WR and Comb are set to the HIGH state for write operation. As a result, circuit of Fig.1(b) is formed. The voltage across the memristors here is (*VD-VDD*/4). Depending on the data, it can be either positive (*VD= VDD*) or negative (*VD*= 0 V). Since the polarities of the memristors are opposite, change of memristances

(or resistances) will also occur in the opposite direction. Now RD and Comb are kept in the HIGH state and this forms the circuit shown in Fig.1(c). Voltage at *D* is now:

$$V_D = \left(\frac{V_{DD}}{2} - \frac{V_{DD}}{4}\right) \times \frac{R2}{(R1+R2)} + \frac{V_{DD}}{4}$$

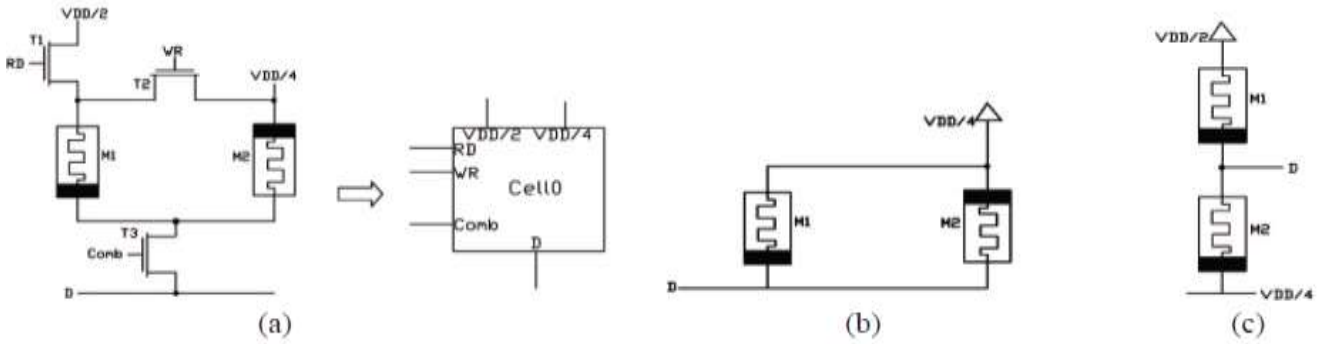

Fig1.
(a) Three transistor-two memristor SRAM cell (b) Circuit when rd=0, wr=1, and comb =1. (c) Circuit when rd=1, wr=0, and Comb=1.

Where, R1 and R2 are the resistances of M1 and M2 respectively. If "1" was written during write cycle, R2 becomes significantly greater than R1 (R2<R1) and then VD is greater than VDD/4 (VD<VDD/4). If "0" was written, *R*1 becomes significantly greater than *R*2 (R1<R2) which makes *VD* to be as close as *VDD*/4. A comparator can be used as a sense amplifier to translate these voltages as HIGH or LOW properly.

B) MTCMOS Technique

Supply and threshold voltages are reduced with the scaling of CMOS technologies. Lowering of threshold voltages leads to an exponential increase in the subthreshold leakage current. In modern high performance integrated circuits (ICs), more than 40% of the total active mode energy can be dissipated due to the leakage currents. With more transistors integrated on-die, leakage currents will soon dominate the total energy consumption of high performance ICs. A popular low leakage circuit technique is the Multithreshold Voltage CMOS (MTCMOS).

The multi threshold CMOS technology has two main features. First, "active" and "sleep" operational modes are associated with MTCMOS technology, for efficient power management. Second, two different threshold voltages are used for N channel and P channel MOSFET in a single chip. This technique based on disconnecting the low threshold voltage (low-Vt) logic gates from the power supply and the ground line via cut-off high threshold voltage (high-Vt) sleep transistors is also known as "power gating". The schematic of power gating technique using MTCMOS is shown in Fig.2 .The transistors having low threshold voltage are used to implement the logic. The transistors having high threshold voltage are used to isolate the low threshold voltage transistors from supply and ground during standby (sleep) mode to prevent leakage dissipation.

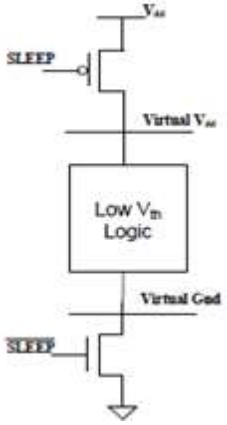

Fig2 .Power Gating Technique using MTCMOS.

In the active mode, sleep transistors are turned on and the logic consisting of low *VT* transistors can operate with high speed and low switching power dissipation. When the circuit is in sleep mode the high *VT* transistors are turned off causing isolation of low *VT* transistor from supply voltage and ground thereby reducing sub-threshold leakage current.

CONCLUSION

In this paper we have proposed Memristor based SRAM with the help of various techniques. It is non volatile in nature because of Memristor and size of Memristor is in nano scale thus it increases the packing density and reduces the power. In this paper we have reviewed on power effective Memristor based SRAM using MTCMOS technique. SRAM takes large part of power & area, therefore to improve power & speed here we are designing Memristor based SRAM. MTCMOS technique is used for reducing leakage power.

REFERENCES:

[1] Vijay Singh Baghel and Shyam Akashe, "Low power Memristor Based 7T SRAM Using MTCMOS Technique," 2015 Fifth International Conference on Advanced Computing & Communication Technologies in MP,India.
.

[2] Thangamani.V, "Memristor-Based Resistive Random Access Memory: Hybrid Architecture for Low Power Compact Memory Design," Control Theory and Informatics ISSN 2224-5774 (Paper) ISSN 2225-0492 (Online) Vol.4, No.7, 2014.

[3] Uma Nirmal, Geetanjali Sharma, Yogesh Sharma, "A Low Power High Speed Adders using MTCMOS Technique," IJCEM International Journal of Computational Engineering & Management, Vol. 13, July 2011.

[4] Nobuaki Kobayashi, Ryusuke Ito and Tadayoshi Enomoto, "A High Stability, Low Supply Voltage and Low Standby Power Six-Transistor CMOS SRAM," 978-1-4799-7792-5/15/$31.00 ©2015 IEEE

[5] Farshad Moradi and Jens K. Madsen, "Robust Subthreshold 7T-SRAM Cell for Low-Power Applications," 978-1-4799-4132-2/14/$31.00 ©2014 IEEE

[6] Mika Kutila, Ari Paasio and Teijo Lehtonen, "Comparison of 130 nm Technology 6T and 8T SRAM Cell Designs for Near-Threshold Operation," 978-1-4799-4132-2/14/$31.00 ©2014 IEEE

[7] G.-F. Wang, W. Kang, Y.-Q. Cheng, J. Nan, J.-O. Klein, Y.-G. Zhang, and W.-S. Zhao, "Low Power Computing Paradigms Based on Emerging Non-Volatile Nanodevices," JOURNAL OF ELECTRONIC SCIENCE AND TECHNOLOGY, VOL. 12, NO. 2, JUNE 2014

[8]Amit Grover, "Low Power 7-T SRAM using 90 NM Technology with Tanner Tool," 2013 First International Conference on Artificial Intelligence, Modelling & Simulation.

[9]U. Supriy, K. Ramana Rao, "Design of Low Power CMOS Circuits using Leakage Control Transistor and Multi-Threshold CMOS Techniques," IJCTA ,July-August 2012.

[10] Bastien Giraud and Amara Amara, Andrei Vladimirescu, "A Comparative Study of 6T and 4T SRAM Cells in Double-Gate CMOS with Statistical Variation," 1-4244-0921-7/07 $25.00 © 2007 IEEE.

[11]Nikhil Raj, Rohit Lorenzo "An effective design technique to reduce leakage power" IEEE Students," Conference on Electrical, Electronics and Computer Science, pp 1-4, March 2012 in Bhopal.

[12]Shyam Akashe, Mayank Shastri, "Read write stability with leakage minimization of 4t SRAM cell for nano CMOS technology,"IEEE Nanoscience engineering and Technology, pp.355-359, 30 November 2011 in Chennai.