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A 4 GHz High-Efficiency High-Linearity GaN Doherty Power Amplifier with Dual DC-Power Supplies

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Abstract: This paper elaborates the basic operation principle of the Doherty power amplifier (DPA) and analyzes the method of improving the linearity of the DPA. A novel DPA with dual DC power supplies and a high linearity is designed and implemented at the operating frequency of 4 GHz. EM (Electro Magnetic)/Circuit Co-Simulation shows that under one tone test, the DPA can obtain the high performance of the 40.4 dBm saturated output power, about 63% maximum power added efficiency (PAE) and about 50% PAE at 6 dB output power back-off (OBO). Under two tones test, the third order inter-modulation distortion (IMD3) is less than -30 dBc when the input power is less than 27dBm. Moreover the DPA delivers the maximum PAE of 61% with the corresponding input power of 26.5 dBm and output power of 38.5 dBm respectively.

Keywords: Doherty power amplifier; GaN; High efficiency; High linearity; Dual DC power supplies.

1. Introduction

For data rate enhancement and the utilization of the full system capacity, most communication systems of the third generation (3G) and the fourth generation (4G), use spectrally highly efficient signals [1]. Modern wireless communication systemssuch as Wideband Code Division Multiple Access (WCDMA), Code Division Multiple Access (CDMA)-2000 and Long Term Evolution (LTE), use digital modulation techniques which produce signals with high peak-to-average power ratio (PAPR) [2], [3]. This puts the emphasis on the importance of improving the average efficiency of RF power amplifiers (PAs) when driven with high PAPR signals by reducing their power consumption in the back-off region. Therefore, in order to avoid distortion and to satisfy the linearity requirement, a RF power amplifier is usually biasing on Class A or Class AB, and it has to operate in deep output power back-off (OBO) region. For example: it usually operates at least 6 dB to 9 dB OBO. Moreover with the decrease of the size and cost of the modern wireless communication systems, the cooling system is becoming more and more simple accordingly, which requires the power amplifier perform as highly efficiently as possible when it operate in OBO region. While the traditional Class A or Class AB power amplifiers have low efficiency in OBO region which cannot satisfy the requirements of the recent wireless communication systems.

There are a few methods to solve the low efficiency problem: envelope elimination and restoration (EER), envelope tracking (ET), and Doherty PA (DPA) [4]-[15]. By adjusting the drain/collector bias voltage, the first two solutions provide good efficiency to minimize the dissipated power consumptions. However some problems existed in these two kinds of systems, such as difficulty of the delay adjustment of the RF

and envelope paths and the complexity of the linkage between the PA and bias modulator. Moreover they require a highly efficient bias modulator as well as the PA [4]-[7]. The Doherty PA can accomplish the high efficiency by employing two PAs: one PA, the carrier amplifier which is operational from a low power region, another PA, the peaking amplifier which is turned on at a high power region. The output powers of the two amplifiers are combined by the self-adjusted load modulation technique, and the Doherty amplifier enhances the efficiency at the low power region [6]-[9]. A significant amount of research has been focused on the Doherty PA to improve its efficiency.

Recently, many high efficiency DPA designs are reported [10]-[11], and the operating frequency of these designs mostly are below 3.5GHz. There are few DPAs implemented using packaged transistors operating above 4GHz. And almost all of the reported DPA designs have four DC power supplies. In this paper, a high-efficiency high-linearity DPA with dual DC-power supplies operating at 4 GHz is proposed. The test procedures have been significantly authenticated. Using a GaN HEMT (High Electron Mobility Transistor), the proposed Doherty PA delivers the PAE of about 60% when IMD3 $\leq$ -30dBc, and the output power of about 38dBm under two tones test.

2. Doherty Power Amplifier Operation

2.1 Basic principle of DPA

The DPA technology was firstly developed by W. H. Doherty at the Bell Lab., in 1936 [8]. The original Doherty amplifier consists of two tube amplifiers and impedance inverting network. Unlike modern transistors, vaccum tubes have extra grids that make trans-conductance easy to control. The prototype of the DPA is shown in Figure 1. Most PAs have constant load impedance and one maximum efficiency point is at the peak power, because the full output voltage swing is achieved only at the peak output power. On the other hand, the Doherty PA provides dynamic load modulation and achieves high efficiency at back-off output power level as good as at the peak power. A classical DPA consists of two power amplifiers, the main (carrier) amplifier and the auxiliary (peaking) PA, which are in parallel. The main PA is biased at Class AB or Class B mode, and the auxiliary PA is biased at Class C mode. The output terminal of main PA output connects with a transmission line with the electrical length $\lambda/4$, which preforms like an impedance transformer to increase main PA output current. Meanwhile a $\lambda/4$ length transmission line adds to the input of the auxiliary PA to make sure the main and the auxiliary PA output have the same phase.

DPA has three basic operating sections: the low, the medium and the peak output power region. In the low power region the input signal is very weak and only the main PA is operating. In the medium region, main PA output voltage reaches the saturation and the efficiency is 78.5% in max theoretically. At the same time, if we increase the power of the input signal, the auxiliary PA will start operating. Because of the pull function to the main PA by the output current from the auxiliary PA, the output impedance of the main PA will decrease. That means, although the output voltage of the main PA saturates, the output efficiency will increase as the load decreases. When input power keeps increasing, the auxiliary PA will saturate and the output power will reach the peak. In this way, DPA technology will make the main PA get the same efficiency at 6 dB OBO, therefore the system can get high average efficiency.

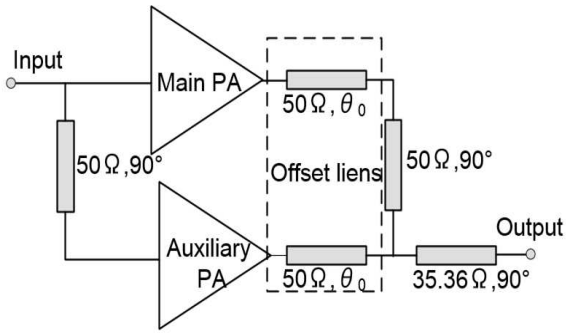


Figure 1 Basic structure of the Doherty power amplifier.

2.2 Linearity of the DPA

DPA technology can improve the linearity of power amplifier. The linearity of the Doherty amplifier is more complicated than that of a Class AB amplifier. In low input power region, with the Class AB bias voltage carrier amplifier has a load impedance which is twice large and the high impedance of the carrier amplifier compensates the low gain characteristic due to the input power division. The power amplifier linearity entirely depends on main PA linearity. Hence main PA must have high linearity when its output impedance is high.

In high input power region, the two amplifiers generate full power using normal load impedances, equal-

izing the power gain. The harmonic cancellation occurs to improve the linearity of DPA from the two amplifiers using appropriate gate bias voltage. The third-order harmonic generation coefficient gm3 of a general transistor and the bias points of the two amplifiers are illustrated in Figure 2. As the auxiliary PA which biases at Class C mode has a gain expansion, the amplitude and phase of its IM3 (Third Order Inter-Modulation) increases; whereas the main PA which biases at Class AB mode has a gain compression, the amplitude of IM3 increases while the phase of IM3 reduces. By setting the main and auxiliary PA biased at an appropriate point, their amplitude of IM3 can be the same while the components must be 180° out of phase. Then when the main and the auxiliary PAs are connected in parallel, the gain feature can be compensated. Therefore, the peaking amplifier should be designed appropriately to cancel the harmonics of the carrier amplifier. Hence, DPA can get a better linearity than traditional Class AB mode PA.

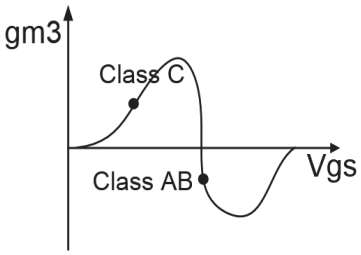


Figure 2 Large-signal gm3 versus gate bias for general FET and bias points of the Doherty power amplifier [9].

3. Implementation of the Proposed Doherty PA

According to the aforementioned theoretical analysis, both the main PA and the auxiliary PA are used by the CGH40006P GaN HEMT, which is made by the Cree. Since the GaN HEMT has the advantages of high electron mobility, high power density and high breakdown voltage and so forth, the GaN HEMT is a suitable candidate for the RF power amplifier design, which has the high efficiency and high power. In the design of Doherty PA, the power distribution is chosen to the Hybrid 90° branch line power divider considering the influence of the circuit size. That is, one of the branch output and input is connected to the main PA and the phase difference of the output and input is 0°. The other is connected to the auxiliary PA and the phase difference is 90°. To achieve the optimal impedance matching, the output and input matching circuit of the PA is used by the double-stub matching network. In addition the 50Ω resistance and 3pF capacitance are added into the input matching circuit to form the parallel LC stability circuit, which can guarantee the stability of the PA. Moreover the 50Ω resistance is installed to the gate in series to guarantee the stability of low frequency.

In order to save the number of DC power supplies during the test, a 10kΩ variable resistance is involved into the gate to achieve bleeder. In this way, when the gate of the auxiliary PA is supplied power, the gate DC power supply can be obtained by changing the value of the variable resistance. Since the drain of the main PA and the auxiliary PA are supplied by 28V, the drain offset line of the two branches can be connected by the wire directly. Therefore the whole circuit only requires two power supplies to realize direct current bias power supply, which provides a great convenience for the test. According to the trade-off optimization of the Doherty PA linearity and efficiency, the full schematic of the proposed Doherty power amplifier is shown in Figure 3.

4. Simulation Results and Discuss

4.1 Small signal parameters simulation

With the increasing need to reduce development time, power amplifier designers are increasingly employing simulation tools which need accurate data. Small-signal gain (S21), and input and output return losses (S11 and S22) were simulated using ADS simulation tool under the following bias condition: the gate voltages of the carrier and peak amplifiers are biased at -3V (Class AB) and -5V (Class C), and the drain voltages are both biased at 28V. Figure 4 shows the simulated small signal characteristics from 0.1 GHz to 5GHz. Input impedance was matched to 50 ohms over large frequency range from around 1 GHz to 4.2 GHz with lower than -10 dB of S11, and the output impedance was also matched to 50 ohm around 4 GHz well. Moreover the DPA has small gain of 12.3 dB at 4 GHz.

Figure 5 shows the DPA is stable over the enter frequency bands with a simulated stability factor $K > 1$ over the frequency range from 0.1 GHz to 5 GHz.

4.2 One tone simulation

In order to get the large signal performance of the proposed Doherty PA, the power Gain, output power and PAE have been simulated using harmonic balance

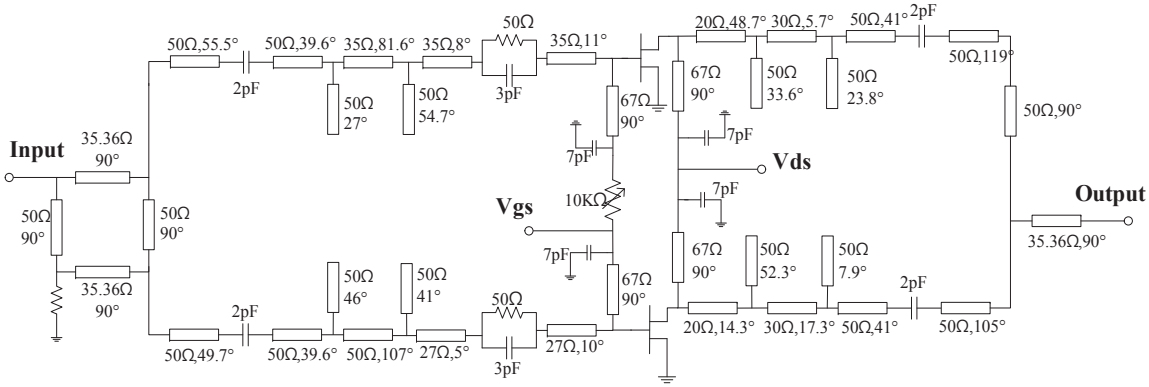
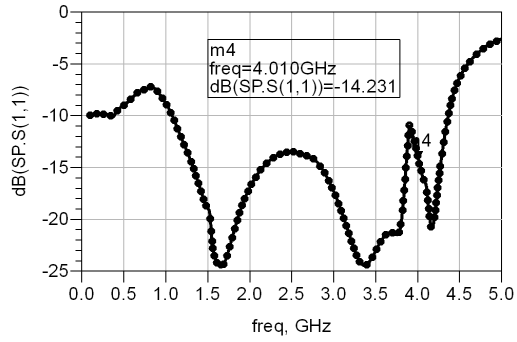
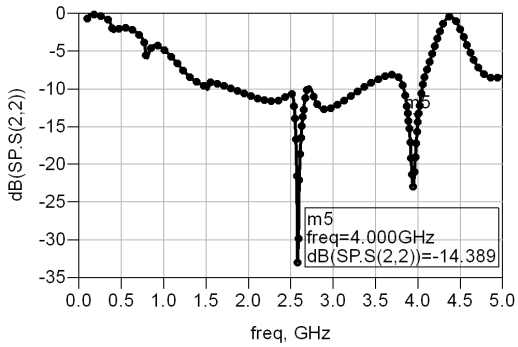


Figure 3 The full schematic of the proposed Doherty power amplifier.



(a)



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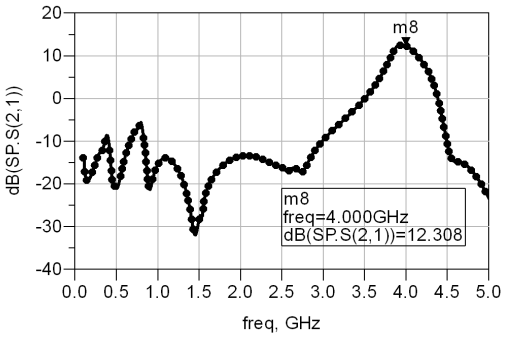


(c)

Figure 4 Small signal S-parameters.(a) S11, (b) S22, (c) S21.

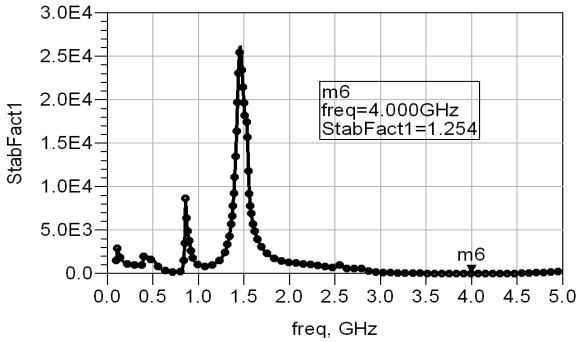


Figure 5 Stability factor.

(HB) simulation in ADS (Advanced Design System) software, which is EM circuit co-simulation. The proposed DPA is simulated under the following bias condition: the gate voltages of the carrier and peak amplifiers are biased at -3V (Class AB) and -5V (Class C), and the drain voltages are both biased at 28V.

To obtain the PAE gain and output power, the continuous wave (CW) signals are applied. Figure 6 shows the proposed Doherty PA provides 63% peaking PAE at the saturated output power of 40.4 dBm, 50% PAE at 6 dB output power back-off (OBO) and 12 dB power gain at 1 dB compression point at 4 GHz.

4.3 Two tones simulation

The linearity properties of the proposed DPA are evaluated by the third-order inter-modulation (IMD3) measurement. Two-tone signals with 5 MHz frequency spacing at the center frequency of 4GHz are applied for the IMD3 measurement. In the ADS software it is taken that EM co-simulation to Doherty PA uses the signal of dual tones.

From the two tones simulation results, the proposed DPA provides 39.2 dBm saturated output power, 61.5% peaking PAE and 11dB gain at the full out-

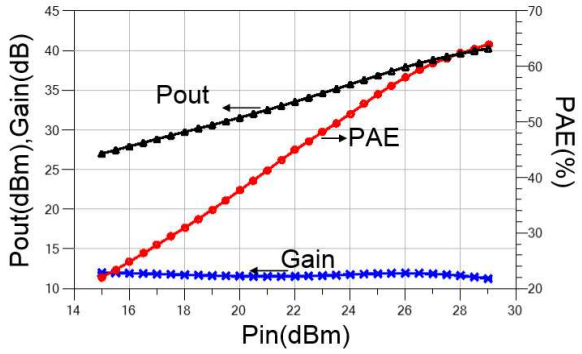
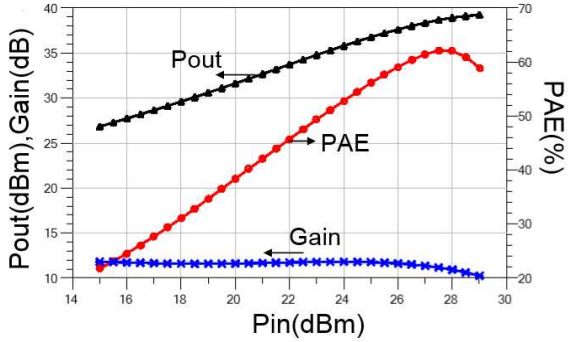
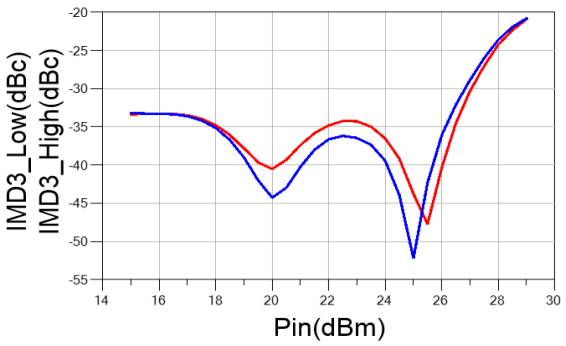


Figure 6 The output power (Pout), PAE and gain of the DPA in terms of input power (Pin).

put power level, as shown in Figure 7(a). As shown in Figure 7(b), the IMD3 of the proposed DPA is lower than -30dBc as the input power is equal and less than 20dBm. The maximum PAE is up to 61% with the corresponding output power of 38dBm when the IMD3 is less than -30dBc.



(a)

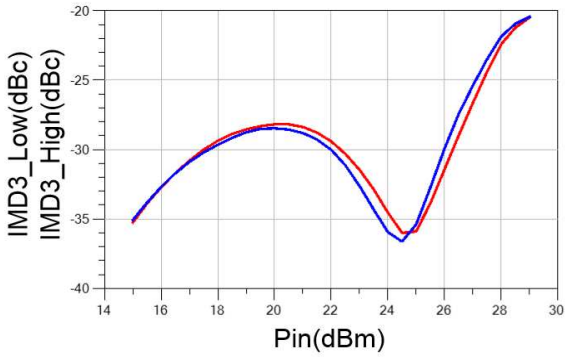


(b)

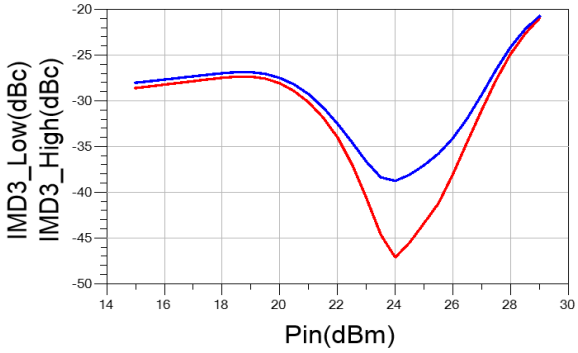
Figure 7 EM co-simulation to Doherty PA using the signal of dual tones. (a) Output power (Pout), PAE and gain of the DPA in terms of input power (Pin) under two tones test. (b) IMD3 in terms of Pin under two tones test.

4.4 Effect of linearity under different gate bias voltage

The linearity performance can be further enhanced to meet the specific requirements by changing the bias conditions of the DPA. In order to analyze the effects of linearity at different gate bias voltage, IMD3 has to be obtained under different gate bias voltage of the peaking power amplifier under two tones simulations. The simulated IMD3 results at Vgs $= -4.5$V and Vgs $= -5.5$V by adjusting the variable resistor carefully which is shown in Figure 8 (a) and Figure 8 (b) respectively. From the comparison of three results, the IMD3 tends to degrade rapidly when the gate bias voltage shifts from the optimum value. Hence, the linearity of the DPA is determined to a large degree by the gate bias conditions of two path PAs. By properly choosing the bias conditions, the performance of the DPA including the linearity, PAE and output power can be obtained optimal.



(a)



(b)

Figure 8 IMD3 being obtained under different gate bias of the peaking power amplifier under two tones simulations. (a) IMD3 in terms of Pin when the gate bias voltage of the auxiliary PA is -4.5 V under two tones test. (b) IMD3 in terms of Pin when the gate bias voltage of the auxiliary PA is -5.5 V under two tones test.

5. Conclusion

This paper describes a novel Doherty power amplifier with dual DC power supplies and a high linearity. By EM circuit co-simulation the test shows that the designed PA has good performance. The basic principle of the Doherty PA and the improvement of the linearity are analyzed. A high efficiency and high linearity Doherty PA, which can work at 4GHz, is designed by using GaN HEMT. In order to further demonstrate the effectiveness and efficiency of the designed Doherty power amplifier, the small signal parameters simulation has been shown in this paper. Furthermore dual power supplies are involved to provide the DC power with the two power amplifiers. Under the one tone testthe DPA can obtain the high performance of the 40.4 dBm saturated output power, about 63% maximum power added efficiency (PAE) and about 50% PAE at 6 dB output power backoff (OBO). The DPA delivers the maximum PAE of 61% with the corresponding the input power of 26.5 dBm and output power of 38.5 dBm respectively. The linearity of the Doherty PA is largely determined by the drain bias conditions of the two power amplifiers. Thus a reasonable choice of the drain bias condition can improve the linearity of the Doherty PA.

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