CMOS Integrated VDBA-ISFET Device for Water Quality Monitoring

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Abstract: The paper presents a performance analysis of low power CMOS Integrated "Voltage Differencing Buffered Amplifier Ion Sensitive Field Effect Transistor" (VDBA-ISFET). The main focus is on simulation of power and performance analysis along with the comparison with existing devices, which is used for water quality monitoring. This approach can improve the calibration of device to a fairly wide range without the use of a high speed digital processor. The conventional devices generally used consume high power and are not stable for long term monitoring. The conventional device has a drawback of low value of slew rate, high power consumption, and non linear characteristics but in this novel design, the device exhibits a better slew rate, piece-wise linear characteristics, and seen consuming low power of the order of $11.3\mu W$. The functionality of the circuit is tested using Tanner simulator version 15 for CMOS process model. The proposed circuit reduces total power consumption per cycle, increases speed of operation, fairly linear and is simple to implement.This device has a simple architecture, and hence is very suitable for water quality monitoring applications.

Keywords: Slew rate, Calibration, Simulation, Ion sensitive field effect transistor, Frequency compensation and low power.

1. Introduction

Monitoring the pH of water resources and sewage system for water pollution is a typical and necessary task in today's overdeveloped scenario. Nowadays we have Semiconductor based micro sensors which are easily available and economical and able to react with the ion concentration. The ISFET has many features like small size, high sensitivity and single chip integration; also it can be implemented by CMOS technology. These features make it the first choice for VLSI electrochemistry biomedical applications. ISFET has been modeled and has been found several drawbacks related to thermal dependency, long-term drift, linearity, and dynamic range. To improve the accuracy in the biomedical applications, it is necessary to find the compensation method to make the applications free from these effects. In order to capture the output response of the ISFET sensors, a readout interface is necessary. In this paper a new approach having greater linearity, low power consumption and large bandwidth by using current mode circuits (CMC's) is proposed.

Conventional water quality monitoring applications are made up of voltage mode circuits (VMC) based on op-amps and OTA's [1-3]. These applications suffer from low band widths (BW's) arising due to stray and circuit capacitances. Also the need for low voltage and low power circuits makes these circuits not suitable for water quality monitoring as these circuits require the minimum bias voltage depending on the threshold voltage of the MOSFETs. There are many analog signal pro- cessing circuits using active elements. Many active devices are developed such as Operational Transconductance Amplifier (OTA), Current Differencing Trans conductance Amplifier (CDTA), Current Differencing Buffered Amplifier (CDBA) and Second Generation Current Conveyor (CC-II). In the circuit principle

called VDBA (Voltage Differencing Buffered Amplifier) is proposed as an alternative to the existing CDBA (Current Differencing Buffered Amplifier). The only difference between CDBA and VDBA lies in the fact that the former uses voltage as input rather than current. Both devices have almost the same properties such as high input and low output impedances. Although VDBA has voltage as input but it has a distinct advantage of providing properties of current mode circuit such as greater bandwidth, lower power consumption, higher slew rate and wider linearity compared to OPAMP [4-7]. The main difference between VDBA and OTA is that VDBA has low output impedance that is more suitable than voltage-mode circuit because there is complete elimination of loading effect. The above advantages motivate us to propose a device using VDBA for water quality monitoring applications.

Why Integrated Circuits?

The idea of placing multiple electronic devices was started in late 1950's. In the last 50 years, the technology got changed drastically producing simple chips having one billion transistors or in other words more than 10 million devices. According to Gorden Moore, the number of transistor per chip has continued to double approximately every eighteen months. Also, the dimensions of transistors has dropped from 25μm in 1960 to about 20nm in the year 2010, resulting in highly improvement in terms of size and speed of integrated circuits.

Why CMOS?

The basic MOSFET was patented by J.E Lilienfeld in the 1930s, before the invention of the bipolar transistor. Due to fabrication limitations, the MOS technologies got popular in 1960's with first generations producing only n-type transistors. In mid 1960's complement-tary MOS (CMOS) devices were introduced afterwards, there was a revolution in the semi-conductor industry. Due to several advantages like low power, small size, full voltage swing less noisy and lower fabrication cost, these devices are much popular in the analogy circuit design.

2. ISFET

An ISFET is an ion-sensitive field-effect transistor which has a property of measuring ion concentrations in solution; when the ion concentration (such as H^+) changes, the current through the transistor will change accordingly [3]. Here, the solution is used as the gate electrode. A voltage between substrate and oxide surfaces arises due to an ions' sheath.

The ISFET has similar structure as that of the MOSFET except that the poly gate of MOSFET is removed from the silicon surface and is replaced with a reference electrode inserted inside the solution, which is directly in contact with the hydrogen ion (H+) sensitive gate electrode [4].The Sub circuit macro model of ISFET consists of four terminal, source(S), drain (D), bulk (B) and floating gate with the reference electrode potential as shown in Figure 1.
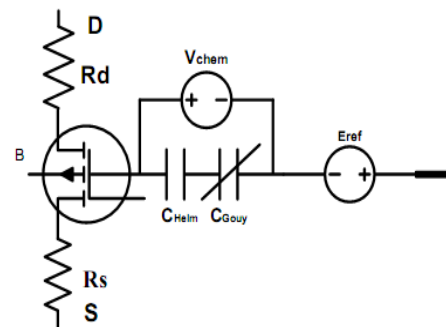

Figure 1 Sub circuit block of ISFET macro model

At the interface between the gate insulator and the solution, there is an electric potential difference that depends on the concentration of H+ of the solution, or so called, pH value. The variation of this potential caused by the pH variation will lead to modulation of the drain current [8-10]. As a result, the I_d-V_{gs} transfer characteristic of the ISFET, working in triode region, can be observed similarly with that of MOSFET:

$$I_{ds} = \frac{\mu C_{ox} W}{L}\left[\left(V_{gs}\text{-}V_{th\_isfet}\right)V_{ds} - \frac{1}{2}\left(V_{ds}\right)^2\right] \quad (1)$$

where Cox is oxide capacitance, V_{gs} is gate souce potencial, V_{th_isfet} is threshold voltage of ISFET, and V_{ds} is drain souce voltage. Wand L the width and length of the channel μ is the electron mobility in the channel

The threshold voltage is a parameter which is different in case of MOSFET. In ISFET, defining the metal connection of the reference electrode as a remote gate, the threshold voltage is given by:

$$V_{th(ISFET)} = E_{Ref} + \Delta\phi^{1j} - \Psi_{eol} + \chi^{sol} + \frac{\phi_s}{q} - \frac{Q_{OX} + Q_{SS}}{C_{OX}} +$$
$$\gamma\{2\varphi£\}^{1/2} + 2\phi_£ \quad (2)$$

where E_{Ref} is the potential of reference electrode, and $\Delta\phi^{1j}$ is the potential drop between the reference electrode and the solution, which typically has a

value of 3mV[6]. Q_{ox} and Q_{ss} are the accumulated charges in oxide and oxide silicon interface. ϕ_s is the work function of substrate. Ψ_{eol} is the potential which is pH independent. It can be viewed as a common-mode input signal for an ISFET interface circuit in any pH buffer solution and can be nullified during system calibration and measurement procedures with a typical value of 50 mV [11-13]. χ^{sol} is the surface dipole potential of the solvent being independent of pH, and the terms in the parentheses are almost the same as that of the MOSFET threshold voltage except that of the absence of the gate metal function. Other terms in the above equation are a group of chemical potential, among which the only chemical input parameter shown has to be a function of solution pH value. This chemical dependent characteristic has already been explained by the Hal and Eijkel's theory [14] which is elaborated using the general accepted site-binding model and the Gouy-Chapman-Stern model.

3. VDBA (Voltage Differencing Buffered Amplifier)

VDBA is a recently reported active component suitable for a class of analog sensor applications [15-17]. As a distinct advantage of the device, i.e., its being able to operate in both current and voltage modes provides flexibility and enables a variety of circuit designs. The differential nature of signals at the input of the device considerably simplifies the implementation of VDBA-based designs. The difference of the input currents I_p and I_n, is reflected to terminal z, whereas the voltage of terminal follows the voltage of terminal z. Moreover, the difference of the input currents is conveyed to terminal voltage via impedance connected to terminal z. The electrical symbol of VDBA is shown in Figure 2.
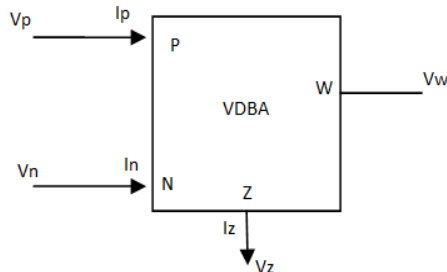

Figure 2 Electrical symbol of VDBA

The relationship among the different values of currents and voltages are given as:

$$I_P = 0, \ I_N = 0, \ I_Z = g_m V_P - g_m V_N, \ V_W = V_Z \quad (3)$$

where I_P, I_N, I_Z, V_p and V_W are the currents and voltages in the respective terminals of VDBA，g_m is the trans conductance of VDBA and V_N is the voltage ratio of the VDBA

Matrix relationship between input and output is shown below.

$$\begin{pmatrix} I_P \\ I_N \\ I_Z \\ V_W \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ g_m & -g_m & 0 \\ 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} V_P \\ V_N \\ V_Z \end{pmatrix} \quad (4)$$

The above matrix representation is very useful to represent the current voltage relationship for the device.

4. CMOS VDBA-ISFET

For the integrated sensors, the measurement circuit tracks the threshold voltage of the ISFET as the electrolyte pH is varied. A practical solution to integrate the sensor with electronics is to view the ISFET sensor as a circuit component in an integrated circuit rather than as an add-on sensor whose output signal is further processed. In this paper, the ISFET is used as one of the input transistors in the differential stage of the VDBA as shown in Figure 3.VDBA circuit basically consists of two parts, of which (M1-M9) is based on OTA circuit and the other part (M10-M16) is the Voltage buffer. The Input stage of VDBA is OTA which is a current mode device and the output is connected to voltage buffer amplifier. The various device parameters are shown in Table 1 with simulate under 0-35μm Technology.

Table 1 Various device parameters

Transistor	W(μm)	L(μm)
M_1-M_4, M_{10}, M_{11}, M_{15}, M_{16}	7	0.35
M_5, M_6	21	0.7
M_7, M_8	7	0.7
M_9	3.5	0.7
M_{12}-M_{14}	14	0.35

When the VDBA-ISFET is configured in such a way that the output voltage (V_o) is equal to the input voltage (V_{in}), any differences in threshold voltages and bias currents between the two input transistors at the differential input stage will also appear at the output. As one of the transistors used is taken as ISFET and shown in Figure 3, the change in gate voltage due to sheath of Hydrogen ions 'saround the electrode inside the solution will appear at the output which can be further expressed in terms of pH of
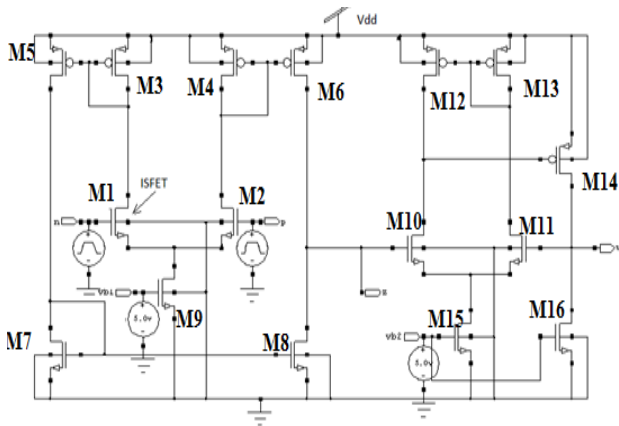
the solution.

Figure 3 Circuit diagram of COMS based VDBA

The simulation of a device for water quality monitoring using ISFET involving analog active com-ponent VDBA has been carried out on Tanner simulator. The output response of the device with respect to time i.e. transient analysis shown in Figure 4 justifies that the device is highly linear and has better slew rate than the conventional device. The waveform obtained shows the highly linear output, which shows that the device is fairly linear device as compared to other conventional circuits used so far [18].
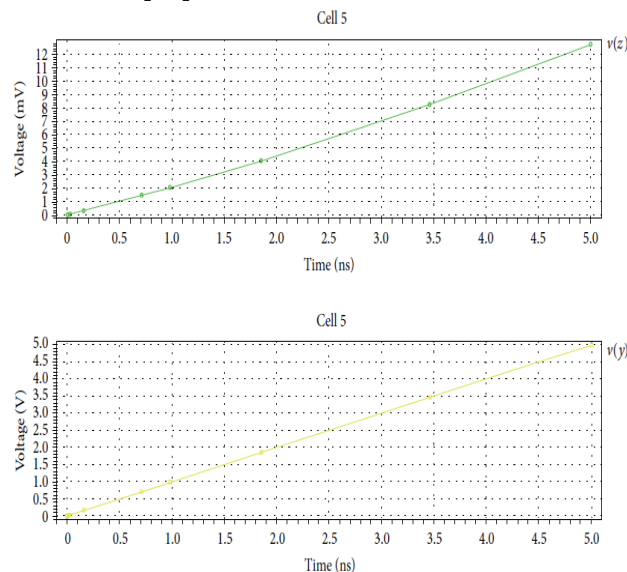

Figure 4 Output waveform

The variation of input voltage at the gate of the ISFET due to the sheath of Hydrogen ion concentration and the output voltage at the V_w terminal of the VDBA is tabulated in Table 2.

Figure 5 shows that on plotting a linear trend line between V_{out} and V_{in}, the coefficient of determination R^2 is found to be 99.7% with standard error of 0.026. The coefficient of determination R^2 is

useful because it gives the proportion of the variance (fluctuation) of one variable that is predictable from another variable. It is a measure that allows us to determine how certain one can be in making predictions from a certain model. The coefficient of determination is a measure of how well the regression line represents the data. If the regression line passes exactly through every point on the scatter plot, it would be easy to explain all the variations.

Table 2 DC Analysis

V_{in}(V)	V_{out}(V)
0.12	0.09
0.67	0.54
0.95	0.78
1.09	0.89
1.31	1.09
1.60	1.33
1.92	1.62
2.30	1.96
2.75	2.37
3.29	2.86
3.93	3.47
4.67	4.21
5.00	4.58
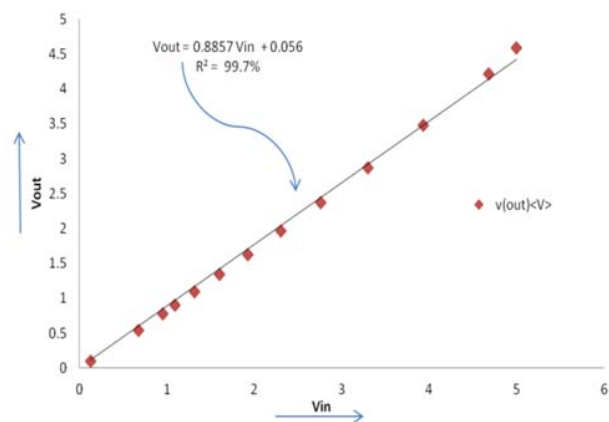
Figure 5 Plot between V_{out} and V_{in}

Table 3 Regression analysis

Regression Statistics	
Multiple R	0.99
R Square	0.99
Adjusted R Square	0.99
Standard Erros	0.05
Observations	14.0

Inference from Table 3

a) The value of R^2 in case of Spice Model is 0.999 which shows the direction of a linear relationship between input and output voltages.

b) The value of standard error is found to be 0.057 which shows the accuracy of the device.

The normal probability plot is a graphical practice for regularity testing. The data are plotted against a notional normal distribution in such a way that the points should form an approximate straight line. Departures from this straight line point toward departures from normality. In given Figure 6, the normal probability plot flows approximately a linear straight line indicating the regularity, accuracy and stability of the device.
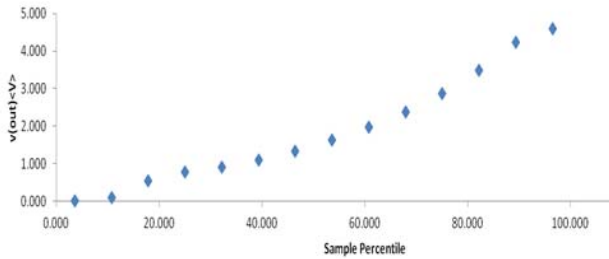

Figure 6 Normal probability plot

The residual plots can be used to appraise the quality of the regression. One can scrutinize the essential statistical assumptions about residuals such as constant variance, independence of variables and normality of the distribution. For these assumptions to hold factual for a particular regression model, the residuals would have to be randomly distributed around zero. The Residual plot is given in Figure 8 whose random nature around zero indicates the regression model is well defined for the device.
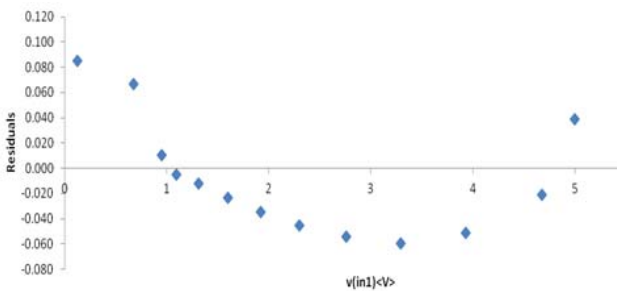

Figure 7 Residual plot

5. Result Analysis

The various device process parameters including power supply, load regulation, line regulation, current range, average power consumed, max power obtained during experiment are shown in Table 4.

The various results obtained are summarized in this section. Figure 8 and 9 show component count and the power consumption comparisons of the new with the exciting device.

Table 4 Device process parameters

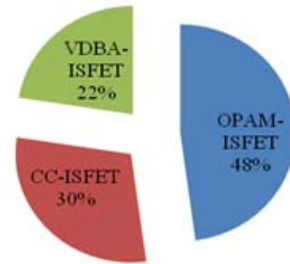| Process Parameter	
Power Supply(V)	5.00
Load Regulation(m)	3.93
Line Regulation(m)	0.60
Current range(μA)	1-50
Average Power Consumed(W)	1.13e-0.05
Max Power(W)	0.44e-0.05

Figure 8 Component Comparison Chart
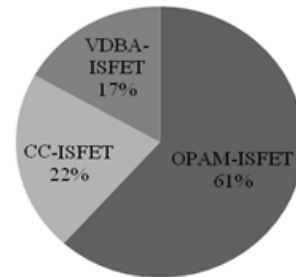
Figure 9 Power Comparison Chart

Table 5 Analysis of various schemes

↓ Parameters	OPAM-ISFET	CC-ISFET	VABA-ISFET
Technology	CMOS	CMOS	CMOS
Power supply (VDD, GND)	5V-0V	5V-0V	5V-0V
No. of Mosfets	27	16	16
Capacitor	2	2	0
Current Source	4	3	0
NMOS	17	10	8
PMOS	10	6	7
Resistor	5	3	0
Voltage Source	4	2	2
Max power Dissipation (Watts)	1.635414e-005	0.574213e-005	0.445088e-005
Stability analysis	Closed loop stable	Closed loop stable	Closed loop stable

For the same technology i.e. CMOS technology deployed for all the four analog IC's and the same power supply, we arrive at the following comparative results:

Inference form the Table 5

a) The number of MOSFET's is 27 in conventional devices, 16 in new devices, Later deploys 37% of components over 63% used in the previous one shown in Figure 8.

b) No capacitor is used in the new technique.

c) The number of current sources deployed is 4-3 in conventional devices and 0 in new devices.

d) The number of n-MOS and p-MOS required are as follows: 17 and 10 for conventional device, 10 and 6 for new device.

e) No resistor is required in the new technique.

f) The voltage sources required for proper operation of the devices are 4 for conventional devices and 2 in new devices.

From this table analysis, we can figure out that there is a significant saving in terms of Components.

6. Conclusion

In this novel design, a new device employing VDBA-ISFET is proposed. VDBA introduced is a convenient building block that provides a simplified approach to the design of linear analog systems. It also consumes considerably low power of the order of 11.3μW. There is significant improvement in the slew rate. The output observed in Fig 4 is highly linear. A significant advantage of the proposed design is its simple architecture, and low component count. Hence, we come to a conclusion that the circuit proposed here meets all our requirements in terms of component saving, i.e., miniaturization and power efficiency. This study may be extended for further improvements in terms of power and size, besides the wiring and layout characteristics level.

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