European Journal of Academic Essays 1(2): 61-69, 2014
ISSN: 2183-1904
www.euroessays.org

Fine-Tuned PID Controller for fast Transient Response of DC-DC Converter

<Chander, Subhash>[1], <Agarwal, Pramod>[2] <Gupta,Indra>[3]

[1]Department of Electronics and Communication Engineering, Govt. College of Engineering and Technology, Jammu
Jammu, Jammu and Kashmir-181122, India
subrag11121@gmail.com
[2]Department of Electrical Engineering, Indian Institute of Technology, Roorkee
Roorkee-247667, Uttrakhand, India
pramgfee@iitr.ernet.in
[3]Department of Electrical Engineering, Indian Institute of Technology, Roorkee
Roorkee-247667, Uttrakhand, India
indrafee@iitr.ernet.in

Abstract: Ziegler-Nichols tuned PID controller's performances usually are not acceptable for applications requiring precise control. In this paper a fine-tuned discrete PID control scheme aiming to improve the transient response of DC-DC Converter during the large load and source changes, is presented. This method is recommended particularly whenever large source/load changes are expected or there is a need of fast transient response time of the DC-DC converter, which is not presented by a simple PID Controller. The algorithm developed in this paper employed a simple logic to modify the PID controller parameters during load/source changes with a minimum computing complexity. The parameters of PID Controller are automatically modified whenever load/source change occur otherwise it will behaves like a normal PID Controller. First the algorithm is developed and is applied to buck converter to improve its performance. A MATLAB/Simulink model is developed and considered for a well designed Buck Converter with non-linear effects such as S/H, quantization, delay, and saturation are considered in the close loop model of the buck converter. The responses of this buck converter are obtained with proposed Fine-Tuned PID (FT-PID) and normal PID Controller and the comparison is presented. A significant improvement in the transient response and rise time of the Converter is observed with the FT-PID Controller. The detailed analysis, simulation results are presented to demonstrate the effectiveness of the developed algorithms.

Keywords: DC-DC Converter, PID Controller, Fine-tuned PID controller, FT-PID, modeling and simulation**.**

1. Introduction

Switch-mode DC–DC converters are power electronic systems that convert one level of electrical voltage into another level by switching action [1]. These converters are very popular because of their high efficiency and smaller size [1]-[2], and therefore are used extensively in personal computers, computer peripherals, communication, medical electronics and adapters of consumer electronic devices to provide different level of DC voltages. The widespread use of switching DC–DC converters in many electronic systems makes a necessity for many design engineers to design and develop efficient and reliable converters according to demand. Switching converters are in general, time-variant, non-linear dynamic systems. The inherent switching operation of electronic converters results in the circuit components being connected together in periodic changing configurations. They represent different circuit configurations within each switching cycle. A closed loop design helps to achieve a well regulated steady state performance in DC-DC converters. However, the challenge is how to handle when unexpected and fast transients occur during the load step-up or step-down. Thus the number of efforts has been put into increasing the transient response of the DC-DC converters and helps the power stage to respond faster to any input and load changes.

Now-a-days, various advancements in process control techniques has taken place, still PID Controllers have been very popular in closed loop control [3],[4]. An extensive survey on the controllers used in industries reveals that 97% of them are of PID structure, due to their simplicity, applicability and ease of implementations[5]. By varying the PID compensator gains during transients the required error signal can be minimized which ultimately enhances the transient response. This could be the more effective method in DC-DC converters for low voltage applications without increasing the circuit instability.

Although many tuning methods have been proposed for PID controllers, but for many of them, performance is quite poor due to among other factors, inadequate tuning of the controller parameters [6],[7].A simple ZN tuning rules is one of most popular method of tuning to obtain reasonable good initial setting of PID Controllers [8] because of familiarity and ease of use [4]. This rule performs satisfactorily for first order system, but they fail to provide acceptable performance for higher order and non-linear systems [7],[8], due to large overshoots and poor load regulation. To

Corresponding Author: Subhash Chander, Govt. College of Engineering and Technology, Jammu,
subrag11121@gmail.com

overcome such drawbacks several tuning schemes are proposed [7],[8] which are essentially applicable for linear systems. Auto-tuning is the desirable feature for managing difficult tasks in non-linear system control nowadays [4]. In a digitally controlled converter, a key advantage is the possibility of auto tuning the controller parameters to adapt to the specific power stage. Efficient, robust and simple implementation of digital controller with embedded tuning capabilities could be a significant breakthrough for digital control in power electronics. The auto tuning process should satisfy two important requirements [9]-Firstly, it should not affect converter operation under nominal condition and secondly, it should be based on a simple and robust algorithm whose complexity should not significantly increase the silicon area of the IC controller. Several auto tuning techniques for PID have been available in the literature [10]–[14]. Due to the fact that PID regulators are widely accepted in industrial applications and also the applications of microcontrollers, DSPs and FPGAs have been rapidly increased in power electronics applications, mainly in the medium/high power range [9]. However, that most of the existing solutions are too complex for small-power DC–DC converters with integrated digital controllers. Some nonparametric methods for the on-line assessment of system dynamics in DC–DC converters are discussed in [15], [16]; but they requires open-loop operation during the identification process and complex signal processing. The approach presented in [15], [16] has been recently applied to controller auto tuning in [17]. A compressive study has been done [5],[18] and scheme is presented for Ziegler-Nichols tuned PI & PID controller to improve the transient response under set-point change and load disturbances.

In this paper general auto-tuning scheme proposed in [5],[18] is adapted for fine tuning of DC-DC converter. Simple fine tuning method for DC–DC converters in which Proportional, Integral and Derivative gains of the controller are continuously modified based on the converter output trend. The purpose of this paper is to implement this scheme to DC-DC converter in discrete form, describing its operation, implementation, simulation results and study the performance of converter with load and source variation

2. Design of Buck Converter

The equations and design parameters considered for the design of Buck converter are given in this section.

2.1. Design equations

For the Synchronous buck converter of Figure1 operating in CCM, the relationship between the input voltage (V_i) and the output voltage (V_O) is given as:

$$\frac{V_0}{V_i} = \frac{t_{ON}}{T_s} = D = duty\ ratio \tag{1}$$

Where T_S is the switching period and t_{ON} is conducting time of the switch. The critical value of the inductor L_{min} and is given by [2]:

$$L_{\min} = \frac{(1-D)}{2} RT_s = \frac{(1-D)}{2\ f_s} R \tag{2}$$

Where, R is the load resistance, and f_S is the switching frequency. The selected inductance should be greater than L_{min} for CCM [2]

However, In practice, the value of inductor is an important design parameter; it influences the overall size of DC-DC converter and the magnitude of ripple current in output capacitor as well as load current at which the converter enters discontinuous mode.

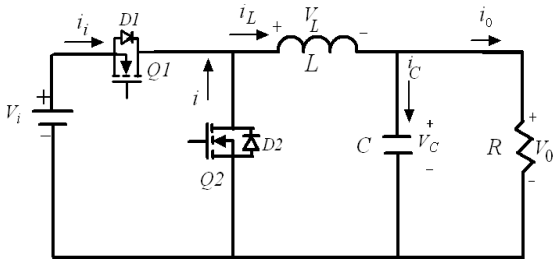

Figure1: Power stage of synchronous buck converter

Normally, a ripple of less than 30% of the average output current is considered for design [19],[20] so as to provide the reasonable efficiency. The actual value of L can be determined as:

$$D(V_i - V_0) = f_s L \Delta I_L \tag{3}$$

Similarly, the initial choice of the capacitor C is then determined by the allowed voltage ripple ΔV, which is typically 2% of output voltage. The overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor and is given as[20]:

$$\Delta V_0 = \Delta I_L \left[r_C + \left(\frac{1}{8C\ f_s} \right) \right] \tag{4}$$

However, the output capacitance increases in presence of a load transient requirement [19].The value of capacitance depends on the change in the load, the speed of the loop and the size of the inductor and is given by:

$$C = L \left[\frac{I_{OH}^2 - I_{OL}^2}{V_f^2 - V_i^2} \right] \tag{5}$$

Where, I_{OH} and I_{OL} is the output current under heavy load and light load conditions respectively. V_f *and* V_i is the final peak and the initial capacitor voltage respectively.

2.2. Design parameters

The following parameters are considered for design of Buck converter:

- Input voltage V_i = 5± 10% V,V_{ref}=2.5V
- Output voltage V_0 = 2.5 ± 2%V
- Nominal load current I_0 = 1.25A
- Output ripple voltage ΔV_0 = 25mV(P-P) at nominal load current
- Parasitic parameters of capacitor and inductor are r_C = 2mΩ, r_L=11mΩ
- MOSFETs $R_{ds(on)}$ = 14mΩ
- Load resistance R = 2Ω (nominal), variation in load between 2Ω and 1Ω.
- Maximum output power P_0 = 6.25 Watts

- Maximum ripple current through inductor = 0.5A = 20% of the nominal load current.
- Fixed PWM frequency = 195.3 kHz.
- Conduction mode: CCM

Based on parameters considered for design as given above, filter inductor and capacitor of synchronous buck converter are designed as:

$$L = 10\,\mu H$$

$$C = 47\,\mu F$$

3.Development of Simulink model of Buck Converter Power Stage

The Simulink model, of the converter for simulation requires the system equations of its power circuit. The Simulink model of Figure 2, is developed from the system equations as shown in Figure 3. Whereas, Figure 4 shows the various sub-systems of the Simulink model of Figure 3.

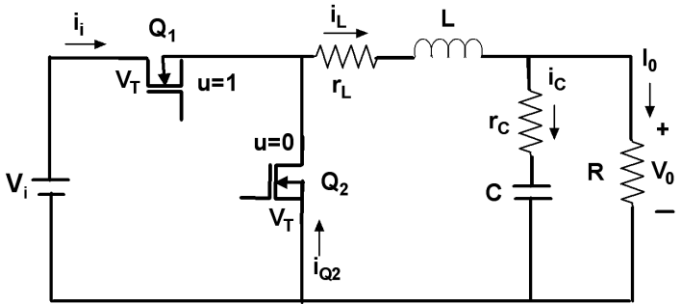

Figure 2: Buck converter with non-ideal components

The dynamics of the converter of Figure 2 operating in CCM, can be understood by using analysis of the circuit and the conduction status of the MOSFET switches *Q1*and *Q2*, described by the switching function *u*, which accepts the values of 0 and 1 [20] . For active switch (*Q1*) conducting:$u_{Q1}=1;u_{Q2}=0$ and for freewheeling switch (*Q2*) conducting:$u_{Q1}=0;\ u_{Q2}=1$. For ideal non-isolated buck converter ON-time: $u_{Q1}=u=1$; OFF-time:$u_{Q2}=\bar{u}=1$. The dynamic and output equations of the converter after simplifications are used for Simulink model of the power stage as under:

$$L\frac{di_L}{dt} = (V_i - V_T)u - V_T\,\bar{u} - i_L r_L - V_C G_1 - i_L G_3 \qquad (6)$$

$$C\frac{dV_C}{dt} = i_L G_1 - V_C G_2 \qquad (7)$$

$$V_0 = V_C G_1 + i_L G_4 \qquad (8)$$

Where, $G_1 = \left[\frac{R}{R+r_C}\right], G_2 = \left[\frac{1}{R+r_C}\right], G_3 = \left[r_L + \frac{R r_C}{R+r_C}\right]$ and

$$G_4 = \left[\frac{R r_C}{R+r_C}\right] \qquad (9)$$

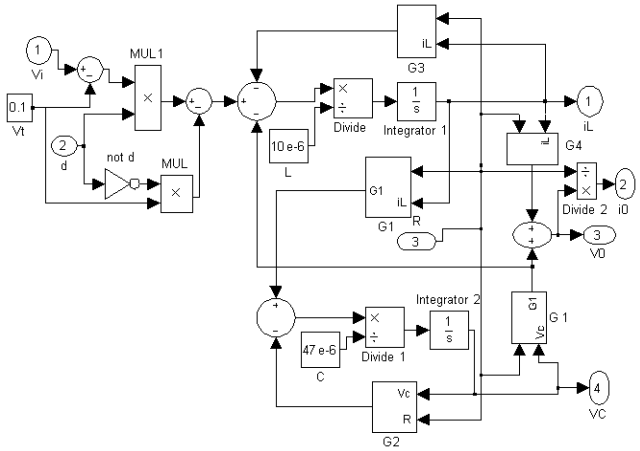

Figure 3: Simulink Model of buck converter (Power stage)

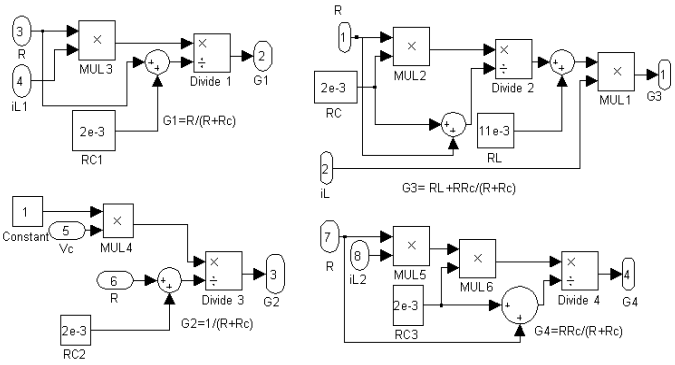

Figure 4: Simulink model of sub-systems G1, G2, G3, and G4 of Figure 3

4. Close loop control of a Switching Converter

As shown in Figure 5, the switching converter block utilizes one or more energy storage elements, depending on the topology, such as inductors, capacitors or transformer to transfer energy from input to the output of the converter at periodic intervals. This energy transfer results in a change of the value of the DC output voltage relative to the input voltage, and can also (in case of the isolated converters) provide electrical isolation between the input and the output ground references. A PWM circuit is also used in the control part of the circuit as well as a sensor circuit and a compensator circuit. The PWM is used to switch the power MOSFET between ON and OFF states. In each period of the output, PWM output is high during a time dT_s (where d is variable duty cycle and T_s is the switching period). In common the converter topology, sensor circuit is a voltage divider, comprising precision resistors. The sensed output signal is then compared with an input voltage. The design objective is to keep output voltage equal to reference voltage, regardless of disturbances or component variations in the compensator circuit. All these blocks constitute the feedback circuit. It helps to maintain required output voltage during variations in load or input voltage by controlling duty cycle d at the gate of power MOSFET switch. The feedback circuit should be designed to achieve good dynamic performance in terms of frequency response, stability, overshoot or transient response to load changes.

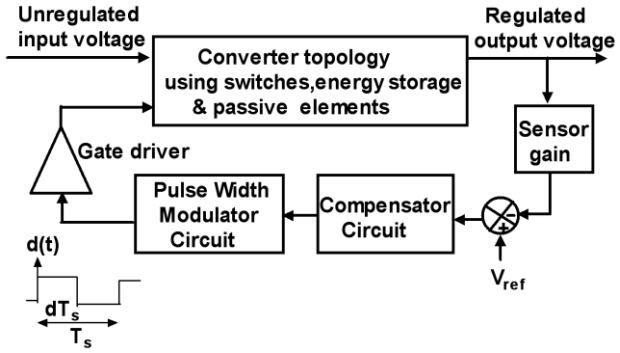

Figure 5: Detailed block diagram of closed loop control of switching converter topologies

Figure6 shows the closed loop control system of the general DC-DC switching converter with PID-based feedback. The goal here is to minimize the error between V_{Ref} and $V_{0.}$

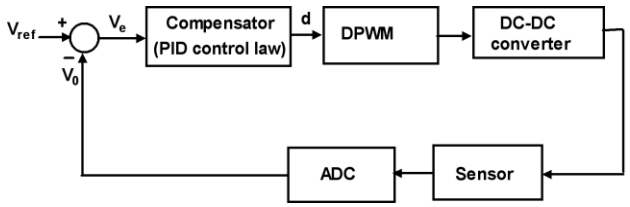

Figure 6: General PID-based feedback Control of switching converter

As seen in Figure 6, there are four major function blocks: ADC (analog-to-digital conversion), COMPENSATOR (error compensation), DPWM (digital pulse width-modulator) and DC-DC Converter [21]-[23]. ADC is for sampling of analog variable, DPWM is for generating driver signal according to corresponding control laws and COMPENSATOR is for generating the control signal by compensating the error signal the error (V_e). The error V_e is (V_{Ref} –V_0) is processed by COMPENSATOR block with PID compensation algorithm to generate control signal. The control signal will affect the converter characteristics significantly. In DC-DC Converters the PID controller is used to compute the duty cycle command corresponding to error V_e, which is applied to DPWM block to generate the switching pulses for the Converter.

5.Discrete PID Control algorithm and parameters determination

Discrete PID control algorithm and the method of determination PID controller parameters are given in detail in this section.

5.1. Discrete PID Controller

A PID controller may be considered as an extreme form of a phase lead lag compensator with one pole at the origin and the other at infinity, provides the compensation in the feedback control of the switching converters. The ideal continuous time PID controller can be expressed as:

$$u(t) = K_P[e(t) + \frac{1}{T_i}\int_0^t e(t)dt + T_d\frac{d}{dt}e(t)] \quad (10)$$

Where $u(t)$ is the control output, K_p is constant coefficient of the Proportional gain, T_i is integral time or reset time, T_d is the derivative time or rate time and e is the error between the reference V_{Ref} and output V_o. The transfer function of standard PID controller is generally written in parallel form given by (11) as:

$$u(s) = \left[K_P + \frac{K_i}{s} + K_d\, s\right]e(s) \quad (11)$$

Where K_P, K_i, and K_d are the Proportional, Integral and the Derivative gains of the controller, respectively. The continuous time domain controller of (11) is transformed into discrete time domain using backward integration method (Euler Method). Using this method, transfer function of a numerical differentiator (12) and integrator are obtained. Then the control action of discrete form of conventional PID controller in z-domain is given by (13).

$$s = \frac{z-1}{zT_s} \quad (12)$$

$$u(z) = \left[K_p + \frac{K_i T_s z}{z-1} + \frac{K_d}{T_s}\frac{z-1}{z}\right]e(z) \quad (13)$$

The structure of the discrete PID controller can be constructed using (14), as shown in Figure7

$$u(z) = \left[K_p + K_i T_s \frac{1}{1-z^{-1}} + \frac{K_d}{T_s}\left(1-z^{-1}\right)\right]e(z) \quad (14)$$

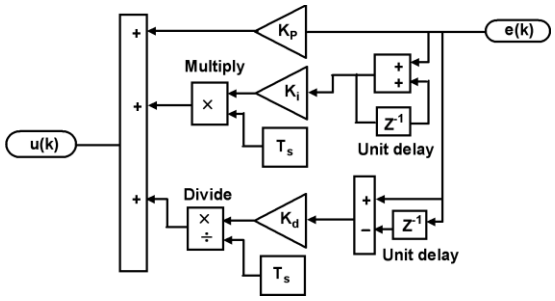

Figure 7: Discrete form PID Controller structure

where, u(k) is control action at K[th] sampling instant, K_P, K_i, and K_d are the Proportional, Integral, and Derivative gains respectively.

Similarly, for digital PID control with sampling periods T_s, the following digital PID control algorithm can be obtained by replacing the derivative term and the integral term with abackward difference function and a sum using rectangular integration respectively. The difference equation is given by:

$$u(n) = K_P\{e(n) + \frac{T_s}{T_i}\sum_{j=0}^{n} e(j) + \frac{T_d}{T_s}[e(n) - e(n-1)]\} \quad (15)$$

Where, index n and j refer to the time instant. The digital PID block can further be simplified as:

$$u(n) = K_P e(n) + K_i\sum_{j=0}^{n} e(j) + K_d[e(n) - e(n-1)] \quad (16)$$

Where, K_i=$K_P T_S/T_i$ is the digital integral coefficient, K_d=$K_P T_d/T_S$ is the digital derivative coefficient and K_P is the digital proportional coefficient. To compute the sum, all the past errors have to be stored. This algorithm is called the "position algorithm" [24]. Also, T_i, T_d and T_s are the integral, derivative time and sampling interval respectively.

5.2. Determination of PID Controller parameters

In this work, the K_P, T_i and T_d are calculated according to ZN ultimate cycle tuning rules. The Ziegler-Nichols ultimate-cycle or closed-loop tuning has been widely known as a fairly accurate heuristic method to determine good settings of PID and PI controllers for a wide range of common industrial processes . The Ziegler-Nichols tuning rule is based on the empirical knowledge of the ultimate gain k_u and ultimate period t_u, as shown in Table 1

Table.1: Ziegler-Nichols tuning formulae

	PID	PI
Proportional gain (K_P)	0.6.Ku	0.45Ku
Integral time (T_i)	0.5.tu	0.85 tu
Derivative time (T_d)	0.125.tu	

The initial values of Controller parameter gains are determined using Ziegler-Nichols ultimate sensitivity method .The criteria for adjusting the parameters are based on evaluating the system at the limit of stability rather than on taking a step response. The PID controller parameters for a converter that may or may not include a delay. Briefly, the experimental technique is as follows:

- Place the controller in proportional mode only.
- Set K_P as variable, T_i is infinity and the value of T_d is equal to zero.
- K_d is increased from zero to critical value i.e until the closed loop system output goes Marginally stable; record K_d, which is the *ultimate gain* called as K_u and the *ultimate period*, $t_{u.}$
- The Ziegler-Nichols tuning formulae of Table.1 are based on the empirical knowledge of the ultimate gain $K_{u,}$ and ultimate Period, $t_{u.}$

These are then used to obtain the tuning parameters of PID controller using Table 1.

6. Proposed Fine Tuned PID (FT- PID) Control Scheme

The simplified block diagram of the proposed FT-PID is shown in Figure 8, the complete design of FT-PID and its control strategy are given in this section is detail

6.1. Design of FT-PID Scheme for DC-DC Converter

A fine-tuning method for DC-DC converters in which gains of PID controller are dynamically modified based on the state of output voltage of the converter. The purpose of the scheme is to improve transient response of buck converter, by simply modifying PID controller parameters automatically, with small modification in PID controller structure. In this paper scheme is implemented on DC-DC converter in discrete form, and performance of the converter is investigated with load and source variation.

The simplified block diagram of the proposed Fined tuned controller is shown in Figure8. It shows that the gain updating factor β is a function of converter's normalize error e_N and corresponding change of normalize error Δe_N. The e_F and e_L represents the full error and limited error values respectively. The gain updating factor β continuously fine tuned the parameters of the PID controller whenever the transients occur. S**i**nce, the starting point of the Fine-tuned PID for the buck converter is its corresponding PID. So, the parameters of PID Controller can be obtained by any standard tuning rules

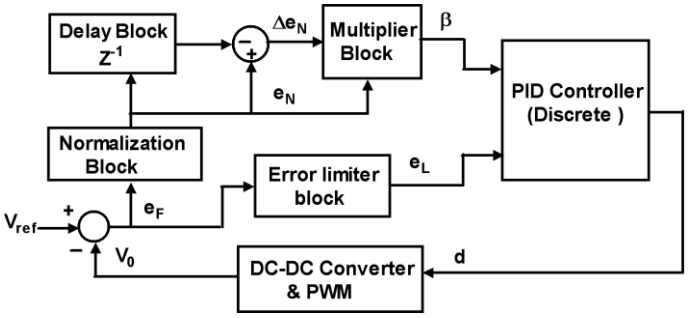

Figure 8: Block diagram of Fine-Tuned Discrete PID Controller structure

In this work, the PID controller parameters are obtained using standard ZN tuning rules, which mean that initial settings of the proposed Fine-tuned PID controller are based on ZN tuning rules. Each of such ZN tuned parameters i.e. Proportional, Integral and Derivative gains is then updated online by a single modifying factor β(k) through some simple relations:

For considered buck converter the error *e(k)* and change in error *Δe(k)* are expressed as:

$$e(k) = V_{ref} - V_0(k)$$
$$\Delta e(k) = e(k) - e(k-1) \quad (17)$$

Where V_{ref} is the reference voltage and V_0 output voltage of the converter. The proposed gain updating factor β is defined as:

$$\beta(k) = e_N(k)\,\Delta e_N(k) \quad (18)$$

Here, $e_N(k) = \left[\frac{e(k)}{e_{\max}}\right]$ and $\Delta e_N(k) = \left[e_N(k) - e_N(k-1)\right]$ are the normalized values of error *e(k)* and change in error *Δe(k)* respectively and e_{max} is the maximum possible value of the error. From (18) it may be assumed that the possible variation of β will lie in the range [-1,1] for all closed loop stable operation. In this method K_p, K_i and K_d are continuously modified by the gain updating factor β(k) with the following simple empirical relations:

$$K_p^m(k) = K_p\left(1 + k_1 \left|\beta(k)\right|\right)$$
$$K_i^m(k) = K_i\left(1 + k_2\,\beta(k)\right) \quad (19)$$
$$K_d^m(k) = K_d\left(1 + k_3 \left|\beta(k)\right|\right)$$

$K_p^m(k)$, $K_i^m(k)$ and $K_d^m(k)$ are the modified proportional, integral and derivative gains respectively at k^{th} instant k_1, k_2, and k_3 are three positive constants, which are used to produce the required variations of $K_p^m(k), K_i^m(k)$ *and* $K_d^m(k)$ from their respective initial values to achieve the desired response. These parameters are properly tuned by choosing the appropriate value of k_1, k_2, and k_3, keeping in mind an overall improved performance of the converter under source and load variations. The transfer function of fine-tuned PID controller is given as:

$$u^{FT}(s)=\left[K_p^m+\frac{K_i^m}{s}+K_d^m s\right]e(s) \quad (20)$$

The corresponding z domain transfer function of fine-tuned PID controller is given as:

$$u^{FT}(z)=\left[K_p^m(k)+K_i^m(k)T_s\frac{1}{1-z^{-1}}+\frac{K_d^m}{T_s}(k)\left(1-z^{-1}\right)\right]e(z) \quad (21)$$

For any change in source voltage or load disturbance, the three parameters $K_p^m(k), K_i^m(k), and\ K_d^m(k)$ are continuously adjusted by a nonlinear updating factor β in order to have a quick recovery of the process during source and load transient without large number of oscillations. Hence it offers the faster dynamic response as verified in the simulation results. Equation (19) indicate that in fine-tuned both K_p^m *and* K_d^m are increased throughout the entire operating cycle; though may not be in same proportion due to difference in values of k_1, and k_3. While, integral gain K_i^m is either increased or decreased from its initial value depending upon the sign of error. An important feature of this fine-tuned PID controller is that, while it preserves the traditional control structure, necessary modifications can be undertaken by incorporating the easily computable dynamic factor β. Moreover, the proposed scheme is model free since β depends only on the instant buck converter output states, normalized error e_N and normalized change in error Δe_N.

6.2. Tuning Strategy for FT-PID Scheme

The objective of the propose fine-tuned scheme for DC-DC converter is that for any change in the source and load disturbance, the Proportional and Integral gains of the FT-PID will be continuously modified to have the quick recovery of the process without a large oscillation. While designing the FT-PID, the following important points are taken into consideration, to provide the appropriate control action in different operating phases. For understanding of the FT-PID on DC-DC converter in CCM being second- order system, a typical close-loop response of DC-DC converter as a second order under damped system is shown in Figure 9.

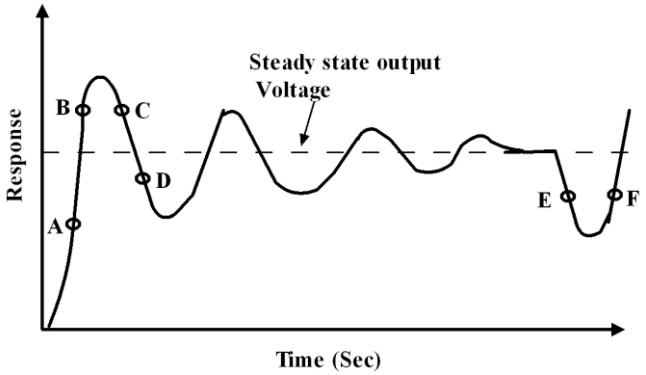

Figure 9: Typical closed loop response of DC-DC converter as second order (Under damped) system

- When the output voltage is far from the refrence voltage/steady state output voltage and moving towards input voltage e.g Point A ,C or F in Figure 9, Proportional should be reasonably large to reach the steady state voltage /refrence voltage quickly but at the same time integral gain should be small enough to prevent the large accumulation of control action , which may result in a large overshoot or undershoot in future. At the same time, to reduce oscillations derivative gain should be increased for higher damping .In such transient phases error *e(k)* and change in error $\Delta e(k)$ are of opposite sign. Therefore dynamic factor β becomes negative .Which will make both the Proportional and derivative gains higher and intergral gain higher than the initial values. This will try to adjust the parameters of the FT-PID reducing the overshoot and /or undershoot without sacrificing the speed of response

- When the output voltage is moving further away from the reference voltage (e.g points B,D or E) increased Proportional, derivative as well as integral gains are expected to bring back the output voltage to its desired values quickly. Under such situations both *e(k)* and $\Delta e(k)$ will have the same sign, therefore making β positive ,which in turn makes all the gain parameters of FT-PID larger than their respective initial values. As a result the control action becomes more aggressive, which will try to restrict further deterioration of such situations. Therefore FT-PID satisfies the need for a relative strong control action to improve the output voltage recovery

7. Fine-Tuned Discrete PID Controller implementation on Buck Converter

The initial values of Controller parameter gains are determined using Ziegler-Nichols ultimate sensitivity method discussed in section 5.2. From these initial values of controller parameters; with trial and error approach the final tuned values for K_p, K_i and K_d are obtained.

Fine-tuning of PID controller parameters has been demonstrated on already designed PID controller as whose transfer function is given as:

$$G_c(s)=\frac{3475}{s}+0.4+1.145e-005s \quad (22)$$

From equation (22), following controller parameters are obtained:

$$K_p=0.4, K_i=3475, K_d=1.145\times10^{-5} \quad (23)$$

These initial values of controller parameter gains are determined off-line. The discrete PID structure with tuned controller parameters obtained is shown in Figure7. The z transfer function of discrete fine-tuned PID controller using (23), are determined using following empirical relations:

$$\begin{aligned} K_p^m(k)&=K_p\left(1+k_1|\beta(k)|\right)\\ K_i^m(k)T_s&=K_iT_s\left(1+k_2\beta(k)\right)\\ \frac{K_d^m(k)}{T_s}&=\frac{K_d}{T_s}\left(1+k_3|\beta(k)|\right)\end{aligned} \quad (24)$$

With tuned parameters, the final empirical relations applicable to synchronous buck converter are:

$$\begin{aligned} K_p^m(k)&=0.4\left(1.5+15|\beta(k)|\right)\\ K_i^m(k)T_s&=(3475)\left(5.12\times10^{-6}\right)\left(1.6+20\beta(k)\right)\\ \frac{K_d^m(k)}{T_s}&=\frac{1.145\times10^{-5}}{5.12\times10^{-6}}\left(1+200|\beta(k)|\right)\end{aligned} \quad (25)$$

$$K_p^m(k) = 0.4\left(1.5 + 15\left|\beta(k)\right|\right)$$
$$K_i^m(k)T_s = 0.017792\left(1.6 + 20\ \beta(k)\right) \quad (26)$$
$$\frac{K_d^m(k)}{T_s} = 2.236328125\left(1 + 200\left|\beta(k)\right|\right)$$

The SIMULINK model of complete structure of fine-tuned, discrete PID controller is shown in Figure10 and the modified controller parameters are given in Figure11.

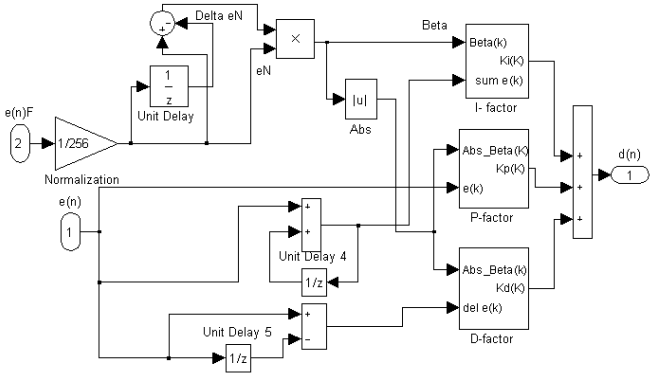

Figure10: Simulink model of Fine-tuned PID Controller structure for DC-DC Converter

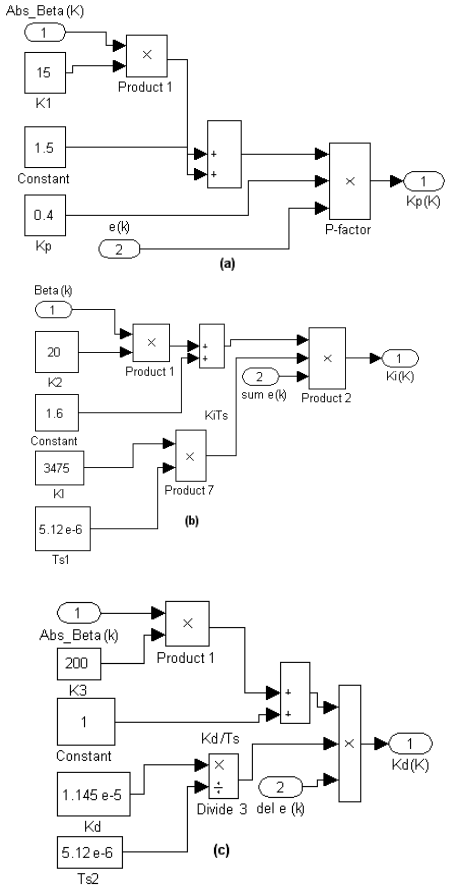

Figure 11 : Modified controller gains (a) Proportional (b) Integral and (c) Derivative

8. Simulation results and Discussion

A MATLAB/SIMULINK closed loop system model of converter with discrete fine-tuned PID controller is shown in Figure12. It includes behavioral models of all controller blocks including discrete fine-tuned PID controller (section 7) and power stage (section 3).

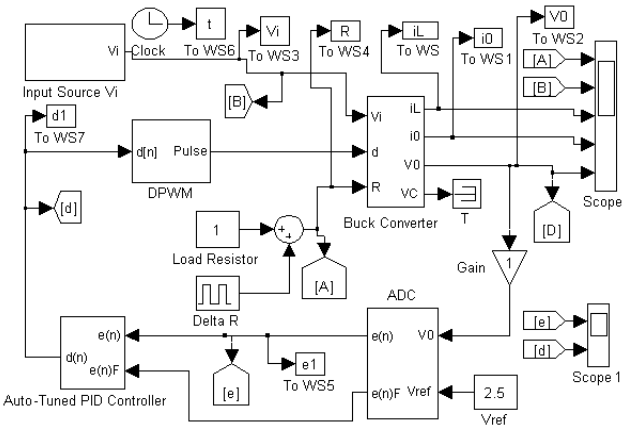

Figure 12: Closed loop Simulink model of buck converter with Fine-tuned Discrete PID Controller

The ADC model used with discrete fine-tuned scheme consists of an element that performs subtraction of output voltage from reference to generate error voltage, ADC gain, sample and hold, quantization effects, delay, and saturation blocks. The error is multiplied by ADC gain and the two values of error signal e[n] and $e_F[n]$ are generated, which are limited to ±31 and ±256, respectively by the saturation block. The full error $e_F[n]$ is utilized for gain updating factor β(k), which is a function of converter's normalized error e(k) and normalized change of error Δe(k) as shown in Figure10. The performance comparison of converter with discrete PID (Figure7) and discrete fine-tuned PID controller (Figure8) is made through simulation of Figure13 with discrete PID structure (with parameters given in (23)) with discrete fine-tuned PID controller designed (with parameters given in (26)). The simulation results for, output current i_0, inductor current i_L and output voltage V_0 (with PID), output voltage V_{01} (with fine-tuned PID) are shown in Figure13.

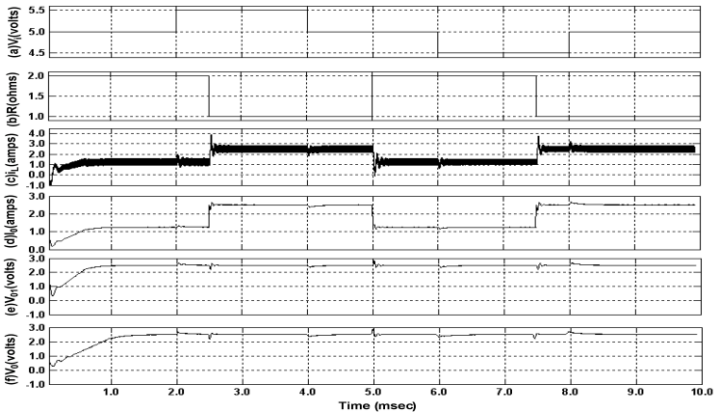

Figure13: Closed loop response of buck converter-(a) Input source voltage V_i (b) variation in load resistance R (c) Inductor Current (i_L) (d) load current i_0 (e) output voltage of converter with normal PID Controller (f) output voltage of converter with Fine-tuned Discrete PID Controller

The response of the system to step change in input voltage is shown in Figure13(a). The nominal voltage of 5.0V changes to 5.5V, 5.0V, 4.5V, and back to 5.0V at 2ms, 4ms, 6ms and 8ms, respectively. The converter has load of 1.25A and changes to 2.5A and back to 1.25A in t = 0ms, 2.5ms,

5.0ms respectively corresponding to change in R from 2Ω to 1Ω, and back as shown in Fig 13(b). The performance parameters are given in Table 2. It is observed that, for input voltage transient, the % overshoot/undershoot is around 5.5% for discrete fine-tuned and 8% for discrete PID controller respectively. An improvement of 2.5% in the overshoot/undershoot is observed with discrete fine-tuned PID controller. Further, for load transient, these values are 13% and 15%, while with discrete fine-tuned PID controller with load transient for 0 to100% and 100% to 0% (of the nominal load), it is 11%, which is improvement of 2% and 4% in corresponding values. Additionally, reduction of around 40% in the rise time with discrete fine-tuned PID controller as shown in Table 2, is an significant improvement. Thus, response of the converter is much faster with discrete fine-tuned PID controller. The settling time for input transient and load transient is about 0.32ms and 0.2ms respectively, for discrete fine-tuned PID as compare to 0.4ms and 0.2ms respectively with discrete PID, which indicates an improvement of 20% in settling time for input transient with discrete fine-tuned PID. This validates that the converter response with discrete fine-tuned PID controller settles to steady state value faster than discrete PID controller. Simulation results show that discrete fine-tuned PID controller has higher dynamic performance as compared to discrete PID controller.

Table.2. Performance comparison of converter with discrete PID and Discrete Fine tuned -PID controllers

Performance parameters	Type of transient	%	Discrete PID	Discrete fine-tuned PID	% decrease over PID
Transient response	Input transient	Overshoot	08.0	05.5	02.5
		Undershoot	08.0	05.5	02.5
	Load transient	Overshoot	13.0	11.0	02.0
		Undershoot	15.0	11.0	04.0
Rise time (ms)	---	---	01.0	0.60	40.0
Settling time (ms)	Input transient	---	0.40	0.32	20.0
	Load transient	---	0.20	0.20	0.00

9. Conclusion

In this paper, a simple model independent Fine-tuned discrete PID control scheme has been presented for DC-DC converter. The proposed scheme continuously adjust the controller gains through some easily interpretable heuristic rules using a single non-linear gain updating parameter β defined on the instantaneous process states. It can be easily applied to an existing controller. The effectiveness of the proposed controller has been tested through simulation experiments on buck converter. The performance of the converter is compared with general PID controller when applied with initial parameters. The discrete fine-tuned PID has shown consistently enhanced performance in transient condition.

Moreover, the proposed scheme is model free since gain modifying factor β depends only on the normalized error e_N and normalized change in error $\Delta e_{N.}$ The proposed method can easily be applied to other converter topologies. The scheme can easily be implemented using DSP or FPGA

References

[1] S. S. Aug, "A practice-oriented course in switching converters, *IEEE Transaction on Education*, vol.39, pp.14-18, Feb., 2003.

[2] N. Mohan, T. M Undeland and W.P. Robbins," *Power Electronics Converters, Applications, und design*, Second Edition, John wiley and Sons, 1996.

[3] K. J. Åström and T. Hagglund ,"The feature of PID control" *Control engineering practice*, vol.9, No.11,pp.1163-75, Nov.2001

[4] K. H. Ang, G. Chong and Y.Li," PID control system analysis, design and technology," *IEEE Transaction on Control Systems Technology*, Vol.13 , No.4, pp.559-76,July 2005

[5] C. Dey and R. K. Mudi, "An improved auto-tuning scheme for PID controllers," ISA Transactions, vol.48, pp. 396-402, 2009.

[6] K. J.Åström and T. Hagglund,, "Revisiting the Ziegler-Nichols step response method for PID Controller," *Journal of process control*, Vol.14, No.6, pp.635-50, Sept.2004.

[7] K. J. Åström, C. C. Hang, P. Persson and W.K.Ho, "Towards intelligent PID control," Automatica, Vol.28,No.1,pp.1-9,Jan 1992.

[8] C.C. Hang, K. J. Åström, and W.K. Ho, "Refinements of Ziegler-Nichols tuning formula," *IEE Proceeding-D,*Vol.138,No.2,pp.111-18, March1991.

[9] W. Stefanutti, P. Mattavelli, S. Saggini, and M. Ghioni, "Auto-Tuning of Digitally controlled DC-DC converters based on relay feedback," IEEE Trans. On Power Electronics, vol.22, No.1, pp.199-207, Jan.2007.

[10] K. J.Åströmand T. Hagglund, *Automatic Tuning of PID Controllers*, Research Triangle Park, NC: Instrum. Soc. Amer., 1988.

[11] K. J. Åström and B. Wittenmark, *Computer-Controlled Systems*, Englewood Cliffs, NJ: Prentice-Hall, 1990.

[12] B. Johansson and M. Lenells, "Possibilities of obtaining small-signal models of DC-to-DC power converters by means of system identification," *Proc. Telecommun. Energy Conf. (INTELEC)*, 2000, pp.65-75.

[13] Y. Q. Chen, C. Hu, and K. L. Moore, "Relay feedback tuning of robust PID controllers with iso-damping property," *Proc. 42nd IEEE Conf. Dec. Contr.*, Dec. 9–12, 2003, vol. 3, pp. 2180–2185.

[14] A. Lev, "PID autotuning algorithm based on relay feedback," *Proc. Inst. Elect. Eng. D*, Vol. 140, No. 5, pp. 328–338, Sep. 1993.

[15] B. Miao, R. Zane, and D. Maksimovic, "System identification of power converters with digital control through cross-correlation methods," *IEEE Trans. Power Electron.*, Vol. 20, No. 5, pp. 1093-1099, Sep.2005.

[16] B. Miao, R. Zane, and D. Maksimovic, "Practical on-line identification of power converter dynamic responses," *Proc. IEEE Appl. Power Electron. (APEC'05)*, Austin, TX, Mar. 2005.

[17] B. Miao, R. Zane, and D. Maksimovic, "Automated digital control design for switching converters," *Proc. IEEE Power Electron. Spec. Conf. (PESC'05)*, Recife, Brazil, Jun. 2005, pp. 2729–2735.

[18] R.K. Mudi, C. Dey and T. T. Lee, "An improved auto-tuning scheme for PI controllers" ISA Transactions, vol.45,pp.45-52,2008.
[19] Texas Instruments Data Sheet,(May,2008). TPS40050: wide-input voltage synchronous buck controller, Ref.no. SGLS219,[online].Available: http:// www.ti.com
[20] V. Ramanarayanan ," Course Material on Switched Mode Power Conversion," *Department of Electrical Engineering, Indian Institute of Science, Banglore-India*,Jan.2009,Ch.5,pp.135-165.
[21] M. Dragan, Z. Regan, R. Erikson, "Impact of digital control in power electronics", *International Symposium on Power Semiconductor Devices and ICs (ISPSD) record*, 2004,pp13-22.
[22] T.W. Martin, and S. S. Ang. "Digital Control for Switching Converters", *International symposium on Industrial Electronics*, 1995, pp.480-484.
[23] Mingzhi he, and Jianping Xu. "Digital predictive V2 control of switching DC-DC converters", *IEEE International Conference on Industrial Technology (ICIT*), 2006.
[24] W. Zhao, B. H. Kim, A.C. Larson and R.M. Voyles, " FPGA Implementation of Closed-Loop Control System for Small-Scale Robot," proc. 12th IEEE International conference on Advanced Robotics, 2005,pp.73-77.

Author Profile

Subhash Chander graduated in Electronics and Communication Engineering from National Institute of Technology, Srinagar (J&K) India in 1993. He received his Post-graduate in Electronics and Communication Engineering from Indian Institute of Technology, Roorkee (IITR)-India in 2004. He completed his PhD in FPGA based Chip Design for DC-DC converters from IITR in 2012. He is an Associate Professor in the Department of Electronics and Communication; he is also holding the Charge of Headship of Electrical Engineering, Govt. College of Engineering and Technology, Jammu (J&K). Currently, he is on the Editorial Board and Reviewers Board of many international Journals. He has been acting as Reviewer for many Journals of international repute like IEEE Transaction on Industrial Electronics, IEEE Transaction on Power Electronics, IET Journal of Power Electronics, Australian Journal of Electrical and Electronics, Journal of Electrical Engineering (Springer) etc. His fields of interest include Micro-Electronics, Low-power VLSI designs and FPGA based design, FPGA based controller design, DC-DC Converters for low voltage applications-topologies and their control

Pramod Agarwal obtained his Bachelor's degree in Electrical Engineering from University of Roorkee, now Indian Institute of Technology Roorkee (IITR), India. He received his Post-graduate and completed his PhD in Electrical Engineering from IITR in 1985 & 1995 respectively. He was a Postdoctoral Fellow with the University of Quebec, Montreal, QC, Canada, from 1999 to 2000. Currently, he is Professor and Head Department of Electrical Engineering, IITR. His fields of interest include electrical machines, power electronics, power quality, FPGA based design, microcontroller, microprocessors and microprocessor-controlled drives, active power filters, multilevel converters, and application of dSPACE for the control of power converters.

Indra Gupta obtained his Bachelor's degree in Electrical Engineering from HBTI Kanpur, in 1984 He received his Post-graduate and completed his PhD in Electrical Engineering from University of Roorkee now Indian Institute of Technology Roorkee, India in 1986 & 1996 respectively. Currently, he is an Associate Professor in the Department of Electrical Engineering, IITR. His fields of interest include simulation, Process Control applications, Microprocessor applications, ANN, Online Control applications and FPGA based Design