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Near Threshold Voltage (NTV) Regulation for System-on-Chip (SoC)

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Abstract— Integrated Circuits (IC)of CMOS (Complementary Metal Oxide Semiconductor) technology have become daily part of our lives. The CMOS technology has been playing a huge role and serving industries with many solutions to design digital circuits. Many different processes, offered by leading semiconductor manufacturing industries, for designing CMOS based transistors that ranging from 16nm to 180nm with different range of input-output voltages, allowing flexibility to design engineers to achieve their set goals. Such increase in number of transistors aggressively in an IC tends to increase power consumption substantially which results in heat and sometimes breakdown of the device. This paper mainly focuses on unique technique to reduce power consumption of the large integrated circuits by reducing the supply voltage (VDD) slightly higher than their process threshold voltages (V_{th}). Near this area energy usage is considerably low. This area is called as Near Threshold Voltage (NTV). The NTV technology in this work includes variation in aspect ratio of width and length of transistor channels and variation in number of gate stages of the CMOS circuits. The designed chip proves to be efficient in consuming power between 10 to 480 times less than their requirement of commercially specified voltage, while maintaining the switching of the devices within expected limits by using this NTV technology.

Keywords—IC; Near Threshold Voltage; CMOS; Aspect Ratio; LTspice IV; V_{th}; MOSIS; MAGIC; Voltage Regulation; SoC; IC Pad; VCO; C5N process; Static Power; Dynamic Power.

INTRODUCTION

Semiconductor based technologies are become important today in our daily lives. CMOS transistor logic systems have become the choice of today's technologies for ICs as their dynamic power is reduced [1]. Fast growing digital world of CMOS technology, electronics industries have adapted with it, because of simple structure designs, wide range of amplification capability and high reliability. At this point, it can be said that there is no successor to CMOS yet which is viable commercially [2]. Sometimes these are also called as Complementary-Symmetry Metal Oxide Semiconductors as they are used in complimentary and symmetrical pairs for different functionality. CMOS are used in all kinds of memories such as RAMs, ROMs, EPROMs and EEPROMS also in digital circuits like MUX, DEMUX and DECODERS etc. [3]. Designing digital logic has become much easier with CMOS Devices in ICs.

CMOS generally don't have the waste heat as of other logics and high noise immunity as well. To understand fundamental concepts of semiconductor devices we must apply modern physics to solid materials. Most integrated circuits has silicon material. Silicon is a Group IV; it forms covalent bond with four adjacent atoms. Due to all the electronics involved in chemical bonds silicon is a poor conductor. To improve the conductivity it has to be tied with Group V material that is arsenic which has 5 electrons in it. 4 atoms replaces silicon atoms and one is loosely bound [4]. So the electron is free to move in room temperature and can carry current. This is called as n-channel semiconductors as of negatively charged electrons. Similarly for p-channel Group III dopant can be used, boron for the matter, the dopant atom borrows electron from neighboring silicon atom and becomes short by 1 electron. The electron and hole can propagate about the lattice making it a P-channel semiconductor being holes as the primary charge carriers. While making Metal Oxide Semiconductors, many processes are used including oxidation of silicon, doping, photo-resist, passivation, resistive deposition, etching etc.

Though CMOS has gained popularity in these years there have been major constraints that come along. CMOS device was basically built for low power consumption but when the system or device is considered the power consumed is more. Today in digital world the technology has been increasingly growing the density of transistors per area and decrease in die size that affects a major factor known as power consumption which can be true for any digital or analog circuits. As power consumption is increasing the cooling techniques have been developed but they lack in providing sufficient cooling as fast as the need [5]. Reduction in power consumption makes device more reliable. There are many factors that affect power consumption in a circuit. Such as output loading effect, variable input, capacitance of each node. Static and dynamic power consumption are the two type which define power consumption in CMOS circuits [6]. Static power consumption is caused due to diffused region and substrate. The reverse leakage current is between diffused region and substrate. It is a product of device leakage current and supply voltage. Dynamic power consumption is due to switching of transistors. When transistors are switching from one logic level to other the nodes are charged and

discharged. This is also dependent on what frequency the circuit is switching. When circuit is switching, current flows between nodes. Most power consumption occurs because of dynamic power consumption.

The power consumption also depends upon the device technology used to manufacture the CMOS based transistors. The change in device technology is a part of reducing induced power [7]. The device technology is being reduced making the parts smaller and making the devices slimmer. Power consumption in any circuit is because of speed and number of CMOS devices. The primary focus of this paper gives a solution over these issues. This paper proposes to use NTV technology for all the circuits in the designed System-on-chip. The voltage used is slightly greater than the NTV to assure the hysteresis region. An IC designed for this paper has different circuits with combinations of different aspect ratio of W/L such as 1, 3 and 5. Also with different combinations of number of stages such as 3X, 11X, 21X, 51X, 201X [8]. In this work, power consumption is analyzed for each circuit for different supply voltages.

PRIOR WORK

Prior research work was focused primarily on Near Threshold Voltage (NTV) region of different circuits. It was needed to find the amount of voltage required to operate any circuit. For this work NTV was approximately 12%-20% of the supply voltage, so the power consumption should be significantly less. To achieve the near threshold voltage, some changes were made in CMOS simulation and design process. The method also required changing the aspect ratio of W/L. MeMDRL_UTSA and other institutions have done some studies in this area [8]. The primary aim of that work was to layout and simulation based on Ring Oscillators for initial study. The circuits were built with different aspect ratios of n- and p-channels. The results have been taken for Wp/Wn=1, 2, 3, 2.5 for limited different number of stages like 1X, 2X, 3X. The best result was found for Wp/Wn= 2.5 and number of stages = 1X.

Near Threshold Operation:

There have been documented before that when smaller architecture of technology of CMOS process develops, logic gate densities increase, but the power consumption is reduced by per gate. As a result, the older designs require redesign efforts and extensive and engineering research to readjust the ICs to the newer technology for reduced power consumption in order to sustain in today's competitive, tough consumer market. Unable to coop such financial stress to re-tech ICs, can drive many designs and logic ICs to run out of business. Near threshold voltage concept is created to power the older ICs at lower voltage and at least at the 1/10 of the power. Here, this lower voltage is at the near threshold voltage where supply voltage is approximately equal to threshold voltage of the transistor. Near this area power consumption is found to be minimal and the performance characteristics are much favorable [9]. The purpose behind this paper is not only to reduce power consumption, but also to improve the performance of the digital signal to be very accurately delivered, as well as few analog and mixed-signal circuits that are considered here. CMOS can work at very low voltages and the power consumption occurs at the nodes of it. The charging and discharging of the internal node capacitances result in power consumption [10]. When VDD is set low, but higher than its threshold and hysteretic voltage region, the circuit can still switch at desired speed but the power usage becomes very low. In this research, extensive work is done on NTV for different supply voltages, run circuit at NTV voltage and also older process VDD. Thereafter, then power is calculated to compare improvement. NTV is achieved by the voltage parameters in CMOS circuits by help the new concept of low power driving MOS transistors and additionally to that FET circuits are placed for assuring the constant voltage regulation.

OBJECTIVES AND GOALS

Main purpose of this work is NTV technology on various circuits and reduction of power consumption. We are also looking for designing a chip and having it fabricated from MOSIS services. The goals and objectives of this project will be as follows,

- Analytical verification on voltage regulators, digital and analog components.
- Numerical verification of comparing circuits under NTV switching.
- Parametric evaluation of threshold voltage at NTV.
- Parametric evaluation at commercial study voltage of 5V at C5N process.
- Run electrical simulation on every component and complete power analysis based on aspect ratio and logic level stages.

DESIGN METHODOLOGY

For designing test circuits, layouts of different circuits were completed to prove the NTV regulation concept. The circuits are both analog and digital. For creating layout MAGIC VLSI tool is used [11]. This tool is used for designing chip as well. Different circuits have been chosen such as Voltage Controlled Oscillator, Ring Oscillator, Current mirror circuit, Differential amplifier for the IC. Each circuit has been designed with different aspect ratio of width and length of transistors. The aspect ratios selected are 1, 3 and 5. These circuits contain different number of stages including 3X, 21X, 51X, 201X. Number of stages increase number of CMOS devices in circuit to give good results in terms of power consumption and also operating frequency. Circuits have been placed in the chip as a

part of the NTV test system. This SoC has 40 pads acting as input output pads. Each side has 10 pads. These circuits are designed using only metal 1 and metal 2. Voltage Controlled Oscillator and ring oscillator have feedback from the output. So these circuits are provided with different supply voltages. The chip also contains voltage regulation circuit based on FET transistor. The voltage regulation circuitry is designed to provide constant voltages. Many voltage regulation circuits are present in market, which give constant voltage. The reason behind building the regulation circuit is that it will provide selected voltage to internal circuit without requiring any additional supply voltage source externally. This voltage regulation circuit can automatically stabilize voltage needed by the circuit regardless of process technology. To design a layout the lambda needs to be set as this design is going under manufacturing. So chosen is the AMI C5N process where lambda is 0.5.

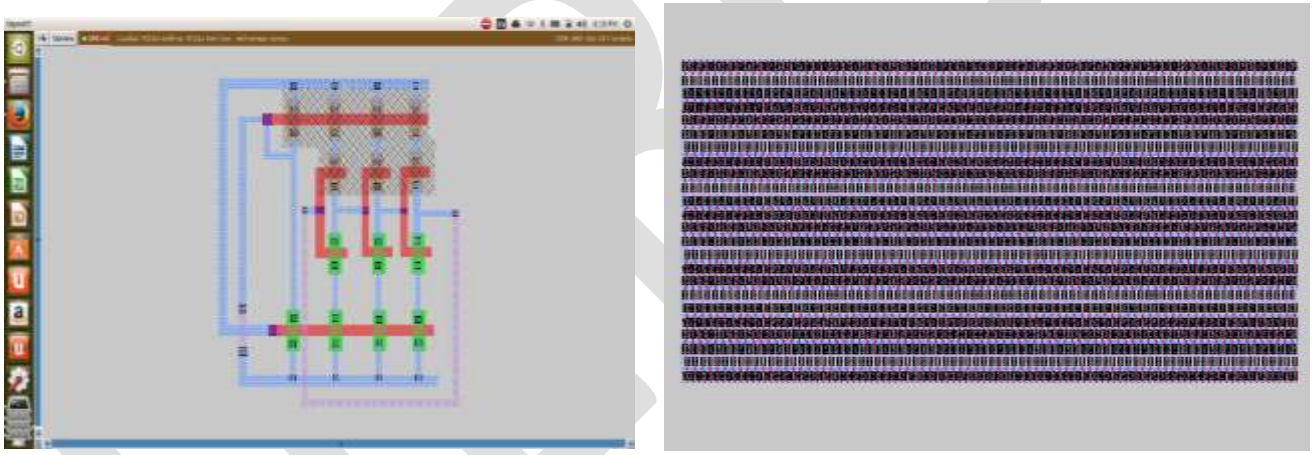
The circuits have been simulated for varying voltage values of VDD. First was to determine the near threshold voltage of each circuit. The values noted are at the point where satisfied toggling has occurred. When the NTV is found the VDD is increased till 5v and results have been taken. To calculate power the current values at different voltages have been noted down and graph has been plotted. Thus this technology ensured to verify results of simulations for circuits normal operations.

Circuits Design for NTV Technology Verification:

All choices of circuits are in different aspect ratios of W/L of transistors and number of stages.

a. Voltage Controlled Oscillator circuit
b. Ring Oscillator
c. NFET based Voltage Regulation Circuit
d. PFET based Voltage Regulation Circuit

Figure 1 Shows layout of the VCO and ring oscillator circuit. Likewise, each circuit layout has been designed with MAGIC VLSI tool. Default bonding pads have been designed to connect the I/O pins. To design desired IC 0.5um process configuration is used that is supported by MOSIS fabrication services.



(a) (b)

Figure 1: Layout design of a 3-Stage Voltage Controlled Oscillator (a) and a 961-Stage Ring Oscillator (b).

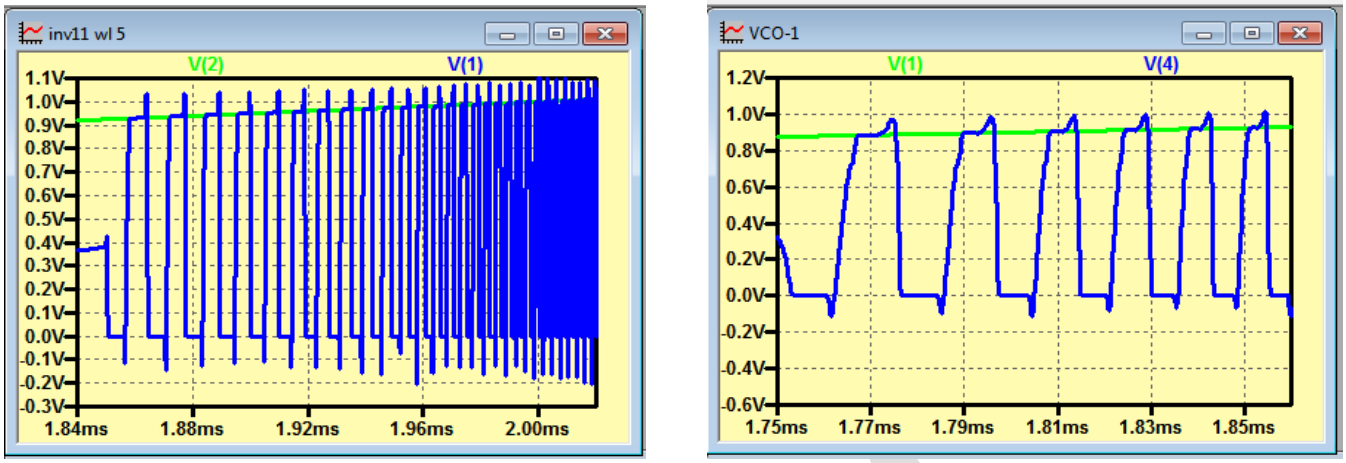
The width and length of PMOS and NMOS are chosen with aspect ratio of 1, 3, and 5. For all the circuit metal1, metal2 have been used and for contacting materials n-diffusion, p-diffusion, and poly have been used.

SIMULATION RESULTS

In this research work, one of the most important goals was to successfully simulate the electrical operations and parametric evaluations. Explained here are the simulation output results for each circuit designed.

Voltage Controlled Oscillator:

Voltage Controlled Oscillator (VCO) produces continues clock as it has a feedback from output therefore it is used for clock generation in digital circuits [12] [13]. VCO is provided with VDD as an input and VDD is varied for different voltages and results have been taken. PSpice is used to simulate all small circuits. The figure 2 shows the output waveforms of VCO. The figure 2 shows VDD (Green) and output (Blue) waveforms.



(a) (b)

Figure 2: Waveform of VCO following VDD (a) and output waveform at toggling (b).

The VDD is ramped from 0V to 5V. It was found to have the NTV = 0.954. AMI C5N process has the parameters for PMOS and NMOS are defined at 0.7640855 and -0.9444911 respectively. Considering the same reason, it can be assured to set NTV at 0.954V. To assure safety of operation, the VDD can be a bit higher than 0.954V, which is 1V. The circuit has been simulated for different aspect ratios of width and length of transistors and number of stages and NTV is calculated. Table 1 shows the results of the NTV.

Table 1: NTV of VCO circuit at different aspect ratios and its number of switching stages.

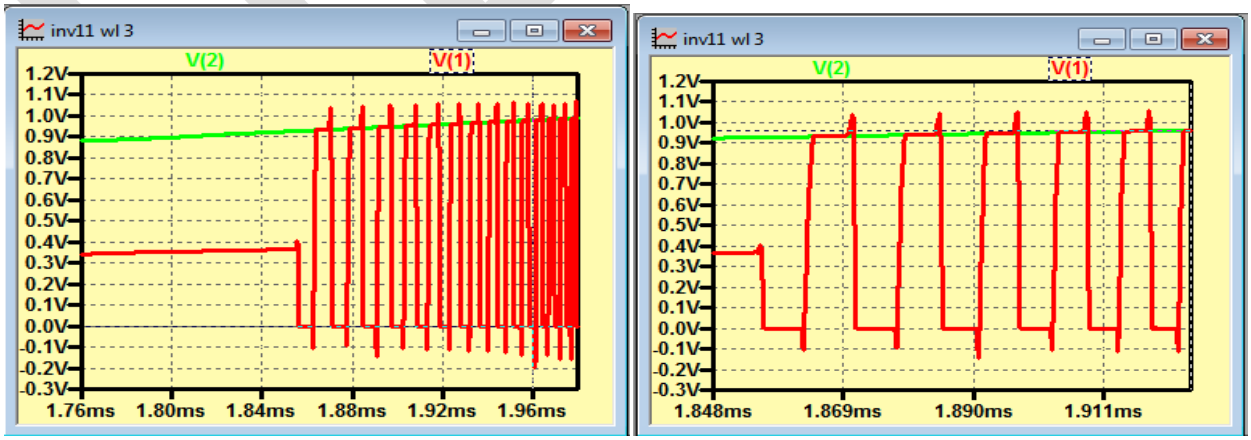
VCO (Number of Stages)	Wp/Wn= 1	Wp/Wn= 3	Wp/Wn= 5
3X	0.957 V	0.925V	0.875V
5X	0.925V	0.899V	0.88V
9X	0.9V	0.89V	0.875V

Ring Oscillator:

Figure 3 shows the special technique of simulation to determine the NTV of any particular circuit design. The toggling output waveform of a ring oscillator at the rising voltage indicates the operation of the circuit at threshold voltage and at NTV. For ring oscillator the VDD (Green) is ramped up from 0V to 5V and output (Red) is toggling near to 0.95V. So considering the safe operation of the circuit, NTV for ring oscillator is set to 1V. The ring oscillator also simulated for different aspect ratio of width and length of the transistor and for different number of stages. The ring oscillator's inverter stages required is given by,

Ring oscillation stages, $S = 2n + 1$

Where, n is the number of inverters required for the circuit.



(a) (b)

Figure 3: Waveform of Ring Oscillator following VDD (a) and output toggling (b).

As explained earlier the near threshold voltage for CMOS in AMI C5N process is near 0.9V the table 2 shows the similar values. Being the primary focus of this paper the ring oscillator was simulated for Voltage at VDD and for current to find the power consumption of circuit.

Table 2: NTV of Ring Oscillator circuit for different aspect ratios and number of stages.

Ring Oscillator	Wp/Wn=1	Wp/Wn=3	Wp/Wn=5
3X	0.91V	0.9V	0.9V
11X	0.98V	0.99V	0.93V
21X	0.975V	0.95V	0.945V
51X	1.0V	0.975V	0.97V
201X	1.03V	1.0V	1.0V

Voltage Regulation and Reliability for NTV Circuits:

As this paper focuses on the technology reliability on low voltage as circuits operate on, power source provides regulation by custom NFET. All circuits in chip are given input that is VIN with value equal to supply voltage that is 5V. The circuit has a varying load resistor (R1). With different load resistance value output voltage has been noted down the same load has cascaded Vth. Significant power efficiency can been seen.

Initially, VIN (V1) is given as a 5V. The load R1 is 125Ohms. Therefore current is 40mA. With the same load, the voltage regulation of NFET for NTV with cascaded V_{th} (Diode) has output of 1.35V-1.42V and current is 10.96mA, shown in figures 4 and 5; thus ensuring excellent regulation of the technology in C5N process. It also proves the same for any other fabrication processes.

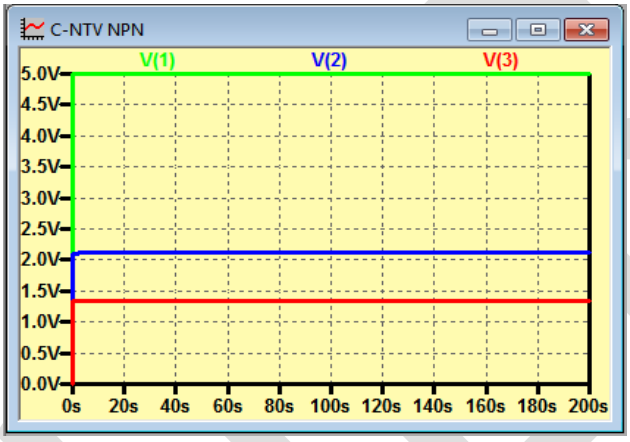


Figure 4: VIN (V1) = 5V, NTV V (3) = 1.35V R1= 125Ohms.

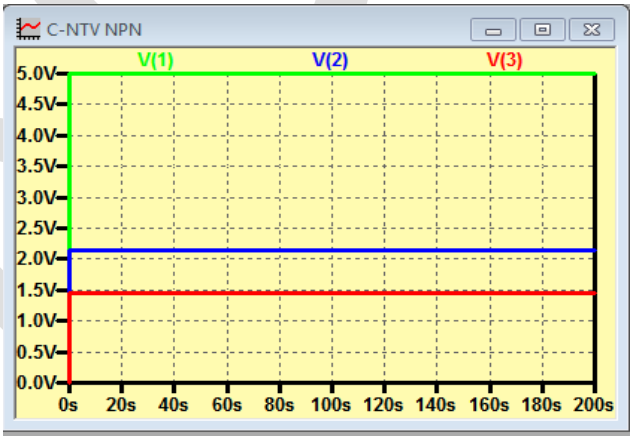


Figure 5: VIN (V1) = 5V, NTV V (3) = 1.42V R1=1KOhms.

So the power can be easily calculated for different input voltages and power ratio can be determined. That is, the Power Ratio = 200mW/15.015mW = 13.32. So the power reduction is almost 13.32 times which can easily be carried out in large CMOS IC's. The simulated results show that for large current load at 125Ohms the output is 1.35V and for small current load at 1KOhms the output is 1.42V. So the regulation of NTV has the reliability of more than 95%.

PFET Based Voltage Regulator:

Figure 6 and 7 shows the NTV regulator design based on the load that is determined for the various circuits suitable to run in many ICs regardless of process technologies. Similar simulations have been carried out and the power ratio in PMOS has been 11.42. That is the power reduction is almost 11.42 times, and also better responses on load conditions than NFET NTV technology. PFET based regulators have more reliability than NFET base regulators that can be clearly seen from simulations. For large current loads at 125Ohms the output (red) is 1.36V and for small current load at 10KOhms it is same as 1.37V so the reliability is almost 100%.

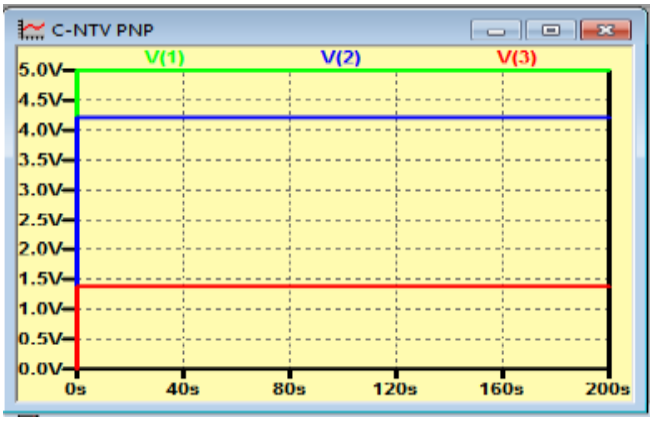


Figure 6: VIN (V1) = 5v NTV V (3) = 1.37V R1= 125Ohms.

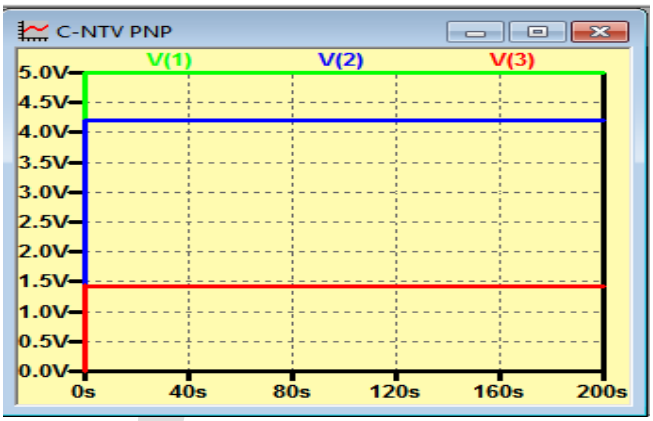
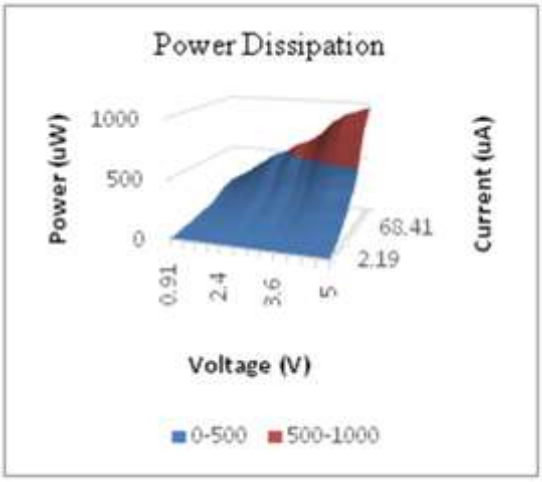


Figure 7: VIN (V1) = 5v NTV V (3) = 1.37V R1= 10KOhms.

Power Consumption by the Circuits:

Below shown are 4 graphs. Those are plotted for comparing results of power consumption of CMOS circuits.



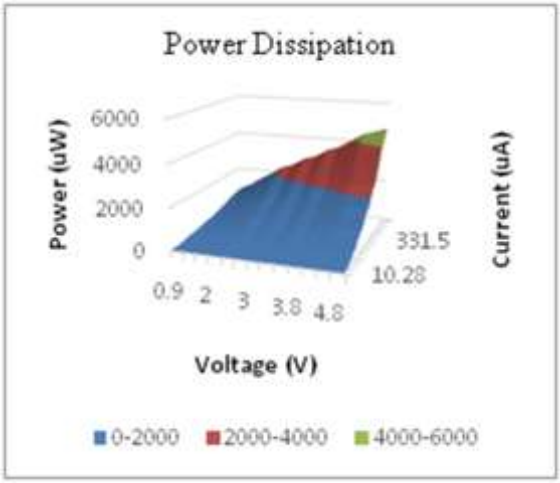
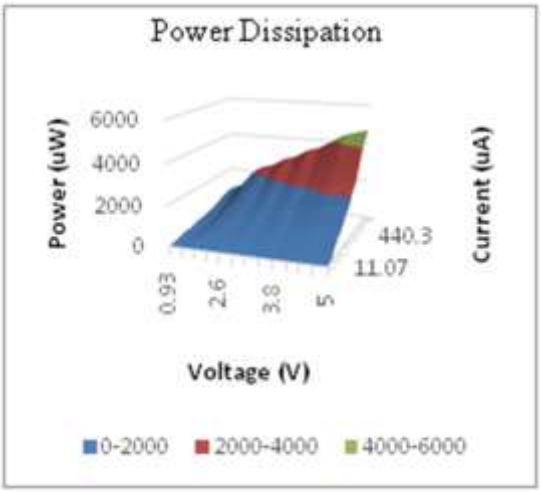


Figure 8: W/L=1, No. of Stages= 3.Figure 9: W/L=5, No. of Stages= 3.



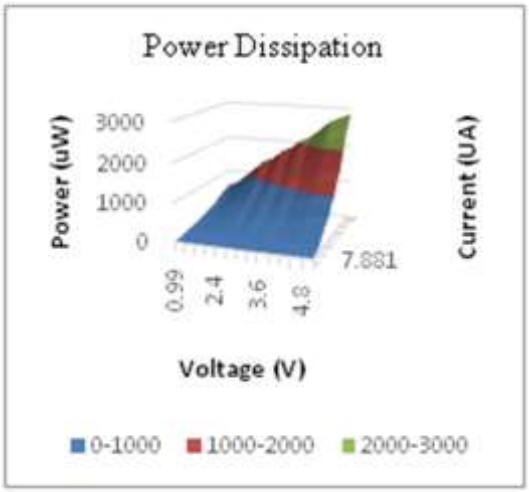


Figure 10: W/L=5, No. of Stages= 11. **Figure 11: W/L=1, No. of Stages= 11.**

To calculate the power, the formula has been used as,

$P_{real}= (V_{rms}/\sqrt{2}) * (I_{rms}/ \sqrt{2})$

Where, P_{real} = Power (uW), V_{rms}= Voltage (VDD) and I_{rms} = Current (uA)

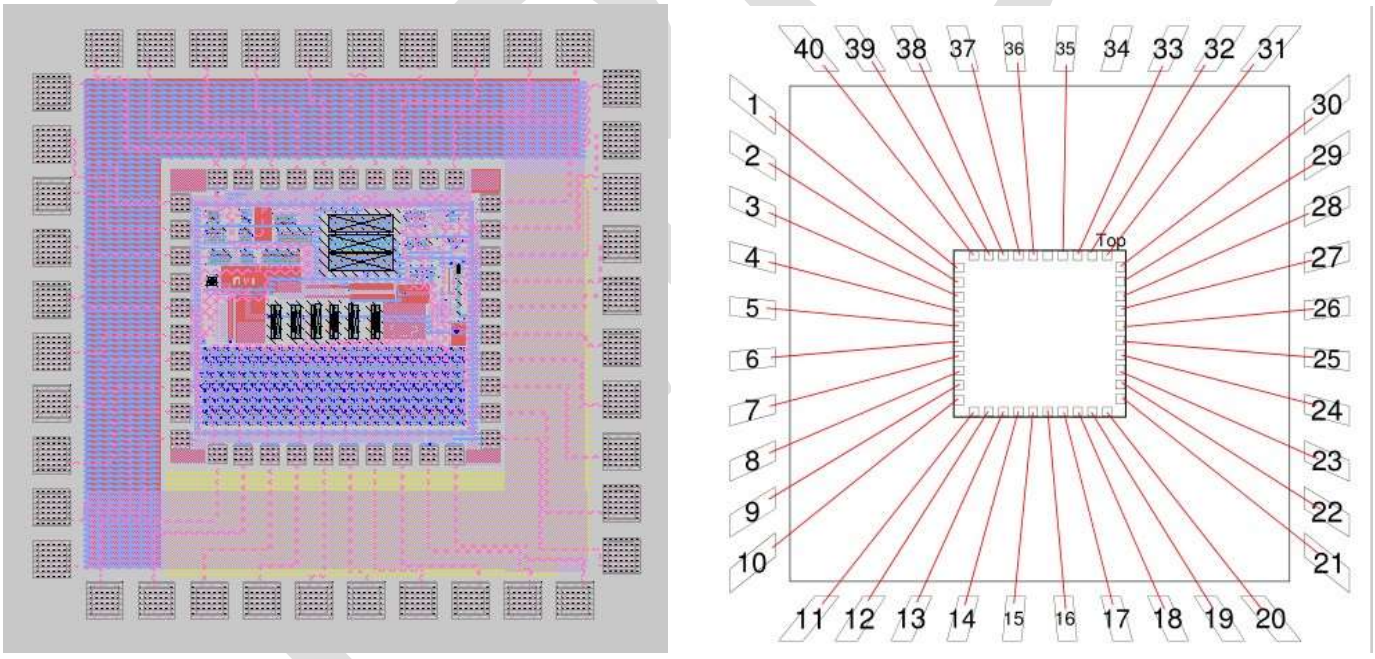
As the VDD increases, power also increases at the rate of VDD^2. From the simulation, power is carried out for all the circuits shown in figures 8 thru 11 show the graphs of power consumption. Also here smaller the aspect ratio, smaller the power consumption becomes. But as the aspect ratio of width and length of transistors and number of stages keep on increasing, the power consumed becomes much higher. At NTV, power consumed is always very low for any number of stages for any aspect ratio used in the design.

Clearly seen from the graphs, it can easily be confirmed that power consumption in the same type of circuit is increased when the number of logical stages are increased i.e. the number of devices increased. But at NTV, the power consumption is always low and switching of devices also stay within normal limits. To further analysis about power consumption where few necessary circuits are found to determine minimum and maximum power values. In 3X ring oscillator power consumption has increased by approximately 480 times starting from NTV to VDD = 5V. In 11X ring oscillator the power consumption has increased by approximately 470 times. The table 3 below shows the power reduction ratio by different designed circuits at NTV driven by the voltage regulation circuit.

Table 3: Power reduction ratio of designed circuits of multiple stages

Designed Circuits	Power consumed in multiple terms
Voltage Controlled Oscillator	284X – 480X
Ring Oscillator	470X - 480X
Current Mirror Circuit	37X – 38X

Chip Layout Considerations:



(a) (b)

Figure 12: **Layout of the NTV Voltage Regulation SoC (a) and IC Pad wire bonding diagram (b).**

In figure 12, the test chip design for the NTV SoC of AMI C5N process, currently under fabrication, had considered these:

Total area of the chip = 1500um X 1500um = 2.25sq-mm

Outer pad area = 90um X 90um

Inner pad area = 45 um X 45um

Min. pad interspace = 30um

Scribe line width = 60um

ACKNOWLEDGMENT

The authors would like to thank the UTSA_OCI team for their encouragements and systematic supports for the new idea and explore effective application of the voltage regulation techniques at NTV for proving the concepts and successfully design the manufacture-able chip. This technology is currently under process of filing for a patent at USPTO through UTSA_OCI.

CONCLUSION

The presented analysis shows that the power consumption in circuits is low at NTV and slightly more than NTV where switching occurs at normal speed without affecting the circuit characteristics. The desired output is achieved by variation in number of stages of circuits and different aspect ratio of width and length of transistors showing that power consumption is also dependent upon these 2 factors as well. The circuits are simulated for values of voltages from NTV to VDD and found that energy improved is up to 480 times at NTV region. Therefore, Instead of operating circuit at VDD the device can operate at NTV regions, but must ensure the normal operations. For voltage regulation as well it is found that confidence of reliability is 95% for wide range of current load. The analysis provides guidelines for operating device at NTV and also provides proof for reduction in power consumption. Initial idea of a type of voltage regulation is placed for the study purposes in the chip for further understanding of the system behavior running under this NTV technology.

The chip is designed to carry out further simulation as part of hardware for tests in future. The chip has analog as well as digital circuits simulated for results have been analyzed. The chip will be used for different upcoming educational projects towards the NTV technology for the future.

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