International Journal of Engineering Research and General Science Volume 3, Issue 6, November-December, 2015
ISSN 2091-2730

Study of VLSI Implementation of Fractional-N PLL using 32nm and 45nm Technology

Amruta Chore, Akanksha Goel, Mily Lal

DYPIEMR, Akurdi, amrutachore2404@gmail.com

Abstract— Nowadays, Low power designs is a very hot topic in electronic systems. The high speed and low power dissipation required in multigigahertz communication systems such as wireless products and optical data links offered by Deep submicron CMOS technologies. **Very-large-scale integration** (**VLSI**) is the process of mounting thousands of transistors on single chip called as integrated chip. Power is way of measuring how fast a function can be carried out. Accuracy and efficiency in power estimation involved in the design phase is important in order to meet power specifications without high cost redesign process. This paper presents the comparison of design and simulation of an chip layout of fractional –N phase locked loop for wireless application using45nm and 32nm VLSI technology. This is a comparison of fractional N-PLL based on latest 45nm and 32nm technology. It offers high speed performance at low power. Sigma delta modulator and low pass filter and improves the performance of the system. Phase locked loop (PLL) represents the leading method in the wireless communications system among variety of frequency synthesis techniques.

Keywords— Voltage controlled oscillator, Phase detector, Charge pump, Sigma delta modulator, loop filter, fractional –N divider.

INTRODUCTION

Phase Locked Loop (PLL) circuits are used for frequency control. PLL can be used as frequency multipliers, demodulators, tracking generators or clock recovery circuits Figure 1 shows a block diagram of a basic Phase locked loop. The phase of a voltage controlled oscillator (VCO)is controlled by PLL. The input signal is applied to one input of a phase detector. The other input is connected to the output of a divide by N counter. A signal is sent to the PLL from some signal source. The two parts of the PLL will work together so that the output of the VCO is same as to the input of the phase detector. If the VCO is lagging behind the input, the phase detector will note down this and increases VCO slightly to keep the two signals aligned, and if the VCO gets leading of the input signal, the phase detector will make the VCO slow down. The output of the phase detector is a voltage relative to the phase difference between the two input signals. This signal is applied to the loop filter or low pass filter. It is the low pass filter determines the characteristics of the phase locked loop circuit. The filtered output signal of low pass filter controls the VCO. The output of the VCO is at a frequency that is N times the input given to the frequency reference input.

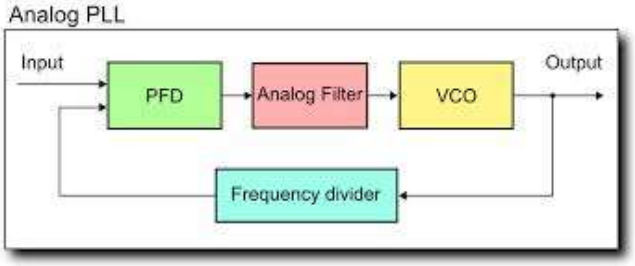

Figure 1 Block diagram of PLL

IMPLEMENTATION OF PLL USING VLSI TECHNOLOGY:

DESIGN OF PHASE DETECTOR USING VLSI TECHNOLOGY

Phase detector circuit in the PLL compares the phases of two signals and generates a voltage signal according to the phase difference between the two signals. Phase difference detection is very important in many applications, such radar and telecommunication systems, servo system and demodulators. The phase detector in the PLL is XOR gate. Its output produces a regular square oscillation when the clock input and signal input have one quarter of period shift (90° or π /2). When the two signals are compared in phase, the XOR gate will have a constant level of zero as output. The XOR detector generates a square-wave output at twice the reference frequency. Layout of phase detector using VLSI technology shown in figure 2.

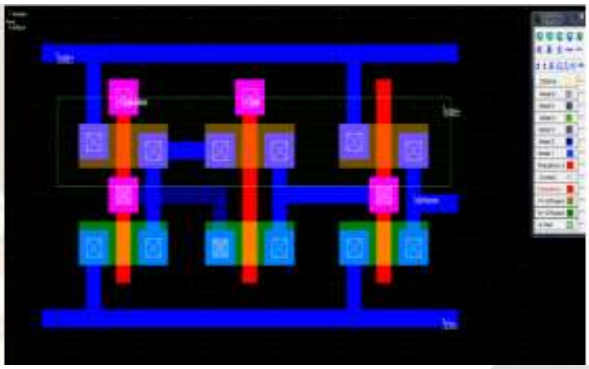

Figure 2 Layout of phase detector

DESIGN OF LOW PASS FILTER USING VLSI TECHNOLOGY

The features of loop filter in order to increase the performance of PLL are-

1) Removes high frequency noise of the detector.

2) Influences the hold and capture ranges.

3) Increases the switching speed of the loop.

In this design passive second order low pass filter is used. It offers the advantages like linearity, low noise and unlimited frequency range. Loop filter is used to removes the unwanted spurious tones and also decreases noise of the control line for VCO. This filter consist of charge pump offers the advantages as reduced noise, reduced power consumption, no offset voltage. The filter is consist of capacitor C charged and discharged through the resistance of the switch. The RC delay creates a low-pass filter. The layout shown in figure 3.

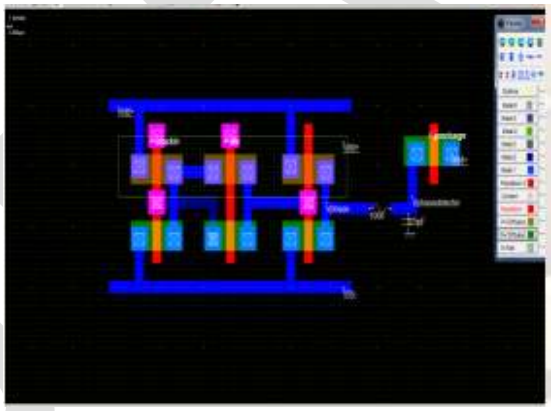

Figure 3 Layout of phase detector with filter

DESIGN OF VOLTAGE CONTROLLED OSCILLATOR (VCO) USING VLSI TECHNOLOGY

Oscillation frequency of VCO is controlled by a voltage input. It is usually used to generate clock in phase locked loop circuit. The VCO oscillates at a higher or lower frequency based on the control voltage, which affects the phase and frequency of the feedback clock. To the low pass filter, the output of phase detector is provided and used as a control signal to drive a VCO. High performance VCO provides very good linearity which is used in this phase locked loop. The principle of this high performance VCO is a delay cell with linear delay dependence on the control voltage. The delay cell consists of a pulldown n-channel MOS, controlled by vplage and a pchannel MOS in series. The delay dependence on vcontrol is almost linear for the fall edge. Figure 4shows the layout of VCO.

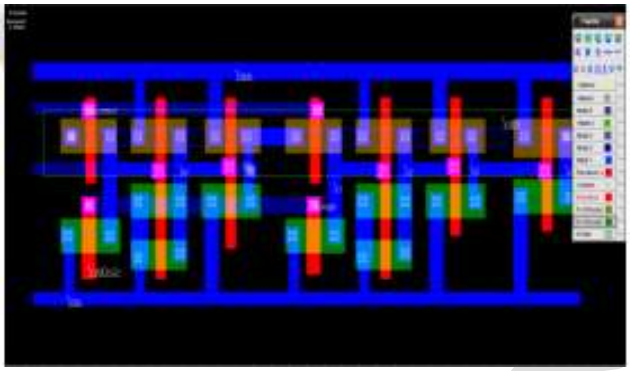

Figure 4 Layout of VCO

IMPLEMENTATION OF FRACTIONAL-N PLL USING VLSI TECHNOLOGY

Modulation is a method for encoding higher-resolution digital signals into lower-resolution digital signals. In this work sigma-delta modulator is designed using VLSI technology with microwind 3.1 software. The desired fractional division number (α) is the input of sigma-delta modulator where the output is a DC component y[n] which is proportional to the fractional input (α) plus the quantization noise introduced due to use of integer divider instead of ideal fractional divider. The frequency divider divides the output frequency of the VCO is divided by frequency divider by Nint+y[n], where Nint is an integer value and y[n] is the output sequence of the modulator.

Among all the frequency synthesis techniques, phase locked loop (PLL) represents the leading method in the wireless communications systems. Current PLL ICs are highly integrated digital and operate on very low power. These ICs require an external crystal (Xtal) reference, voltage controlled oscillators (VCO) and minimum external passive components to generate the abundant range of frequencies needed in a modern communication systems. Figure 6 shows the optimum, high efficient chip design of low power fractional-N PLL frequency synthesizer using sigma delta modulator using VLSI technology. This layout design is implemented using NMOS and PMOS BSIM4 transistors with good dimensions of transistors and metal connections according to the Lambda based rules of microwind 3.1 software. For the PLL, power supply VDD of 1 volt is used. Figure 6and 7 shows comparison of the voltage versus time response of fractional-N PLL using 45nm and 32nm technology respectively. Figure 8 and Fig. 9 shows comparison of frequency versus time response of PLL using 45nm and 32nm technology respectively.

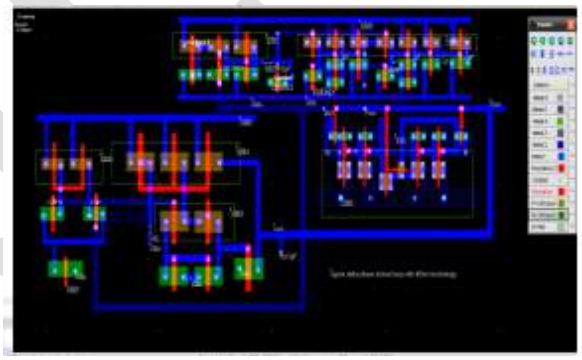

Figure 5. The optimum, high efficient layout design of low power fractional-N PLL with sigma delta modulator using VLSI technology

COMPARISON OF VOLTAGE VS. TIME AND FREQUENCY VS. TIME OUTPUT OF FRACTIONAL-N PLL BETWEEN 32NM AND 45NM TECHNOLOGY

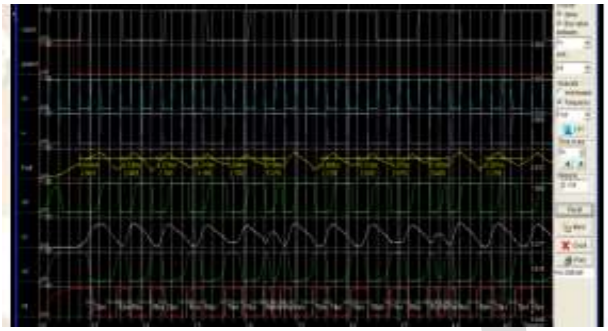

Figure. 6 Voltage verses time output using 45nm technology

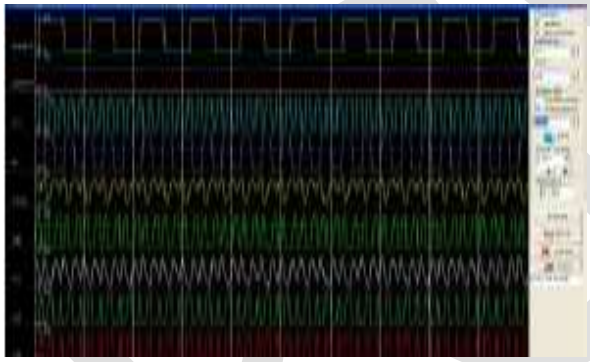

Figure. 7 Voltage verses time output using 32nm technology

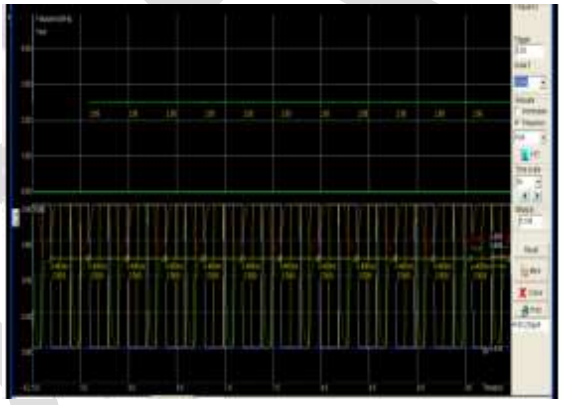

Figure. 8 Frequency verses time output using 45nm technology

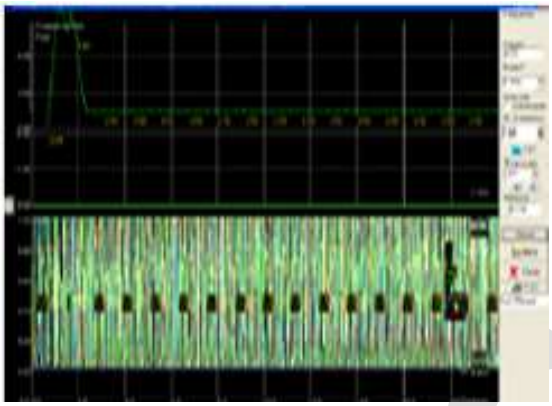

Figure. 9 Frequency verses time output using 32nm technology

PARAMETRIC COMPARISON SUMMARY OF PLL USING 45NM AND 32NM VLSI TECHNOLOGY

SR. NO.	PARAMETERS	VALUE using 45nm	Value using 32nm
1	VDD	1.0 volt	1.0 volt
2	VDD DIV/2	0.5 volt	0.5 volt
3	Ioff N (nA/µm)	5-100	5-100
4	Ioff P (nA/µm)	5-100	5-100
5	Gate dielectric	Hfo2	Hfo2
6	Input frequency	2.1 GHz	2.1 GHz
7	Output frequency	2.50 GHz	2.50 GHz
9	No. of NMOS and PMOS transistors	23 NMOS, 23 PMOS	21 NMOS, 21 PMOS

Table 1 comparison summary

CONCLUSION

Conclusion must be short and precise and should reflect the work or research work you have gone through. It must have same as above in introduction paper adjustment

REFERENCES:

[1] MS. A. V. Manwatkar and Prof. V. B. Padole, " Design of 2.5 GHz Phase locked loop using 32nm CMOS technology," International journal of engineering and computer science, Volume 3, Issue 6 June 2014

[2] N. Fatahi and H. Nabovati, "Design of low power fractional-N frequency synthesizer using sigma delta Modulation technique," 27th International Conference of Microelectronics, IEEE, 2010.

[3] Aamna Anil and Ravi Kumar Sharma, "A high efficiency charge pump for low voltage devices," International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.3, June 2012.

[4] Ms. Ujwala A. Belorkar and Dr. S. A. Ladhake,"Design of low power phase lock loop using 45nm VLSI technology," International journal of VLSI design & Communication Systems (VLSICS), Vol.1, No.2, June 2010

[5] Kyoungho Woo, Yong Liu, Eunsoo Nam, and Donhee Ham, "Fast-Lock Hybrid PLL Combining Fractional-N and Integer-N Modes of Differing Bandwidths," IEEE journal of solid-state circuits, vol. 43, NO. 2, february 2008 379.

[6] Michael H. Perrott, "Fractional-N Frequency Synthesizer Design Using PLL Design Assistant and CppSim Programs," July 2008

[7] Mohammad Sohel, "Design of low power Sigma Delta ADC," International journal of VLSI design & Communication Systems (VLSICS), Vol.3, No.4, August 2012.

[8] Amruta M. Chore, Shrikant J. Honade / "VLSI Implementation of Fractional-N Phase Locked Loop Frequency Synthesizer ", International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com Vol. 3, Issue 4, Jul-Aug 2013, pp.855-860

[9] B. K. Mishra, Sandhya Save and Swapna Patil, "Design and Analysis of Second and Third Order PLL at 450MHz," International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.1, March 2011.

[10] S. Borkar, "Obeying Moore's law beyond 0.18 micron," in Proceedings of the 13th Annual IEEE International ASIC/SOC Conference, pp. 26–31, September 2000.

[11] R. K. Krishnamurthy, A. Alvandpour, V. De, and S. Borkar, "High-performance and low-power challenges for sub-70 nm microprocessor circuits," in Proceedings of the IEEE Custom Integrated Circuits Conference, pp. 125–128, May 2002.

[12] R. Jacob Baker, CMOS Circuit Design, Layout and Simulation, IEEE Press, John Wiley & Sons, 3rd edition, 2010.