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Flit Inversion Techniques for Reducing EnergyConsumption in NoC

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Abstract— The dynamic power dissipation in the NOC is mainly due to coupling effects between on chip interconnections in deep submicron VLSI designs. Coupling effect between the interconnections not only enhances power-delay product but also decreases the signal to noise ratio and increases signal distortion due to cross talk noise obtained by capacitance and inductance.as technology shrinks the power consumption in NOC links is start compete with the NOC routers. In this paper we proposed flit inversion techniques which reduces both coupling activity in adjacent links and self-switching activity in particular data links. Before data enters into network interface we encode the data flit and decode at destination end of the NI.. From the result we get the reduction in power and energy consumption areup to 35% and 20%, without degradation of performance

Keywords— Coupling Activity, Self-Switching, Dynamic power, Interconnect, Flit, Cross Talk, Router

INTRODUCTION

The number of cores in network on chip increases, the designing of the efficient communication interface is more adequate in the next generation architectures. Involving of more sophisticated advanced on-chip protocols, routing algorithms, adaptive selection schemes, flow control and protection schemes are aimed to quality of design. But nowadays interconnection system becomes one of key metrics which characterize the architecture performance and power consumption. Network on chip is actually obtained as solution for the design of scalable and modular communication applications. The proposed encoding scheme is based on the wormhole switching architecture shown in figure:1.In the data spited into flits(adjust to link of network link).the header flit in the data will directs the flit into particular link, and remaining data flits will follow the same link in pipeline fashion. The decision whether the flit is inverting or not is completely based on previous data flit. In self-switching activity if number of transitions from 0 to 1 in two consecutive lines (the flit about to traverse, the flit just transmitted) is more than half of the link width of link, then the data is inverted to reduce number of 0 to 1 transitions. Since all data flits in the pocket will follow the same link and are not linked with adjacent flits belongs to other pockets, the decision taken at the interface node is valid all the links along the routing path. As complexity of design increases, the length of interconnections increases, the distance between the wires decreases which increases coupling capacitance resulting more power-delay product. The technique is more translucent to the NOC, since the technique doesn't affect the performance of the remaining structure of NOC. And no need to do any modification in router design in this paper we proposed three encoding schemes, in scheme I we focus to reducing type1 transitions by odd inversion.in scheme II we reduces type1 and type2 by full inversion or half inversion based on power model.in scheme III we shows different behaviours of data by odd, even and full inversion which leads highest power reduction.

PREVIOUS WORK

On the contest of designing power efficient network links, many papers are published, most of them concentrate the reducing dynamic power in different components such routers, network interfaces and links. Here we present some of those literatures briefly. These include shielding of links [7][8],increasing the link-to-link space[6]. By these all techniques the chip area gradually increased. Another technique is encoding the data flits to decrease the dynamic power dissipation. The encoding techniques are categorized into two types. In the first category the inversion technique reduce the power dissipation due to self-switching activity in the data link. These includes bus-invert coding [9], grey code technique [10], working-zone encoder [11]. But these techniques are not suitable in case of deep submicron technology, where coupling capacitance is the major metric for power dissipation. In second category the literature concentrate on reduction of coupling switching activity [21][25][26]. Among these techniques the coupling transition reduced by either extra control links. The schemes presented in [30] [29] having small number of control links, but complexity of decoder increases chip area. In the scheme [26], concentrate on the type1 type 2, if number larger than half of data link width, then data is inverted.

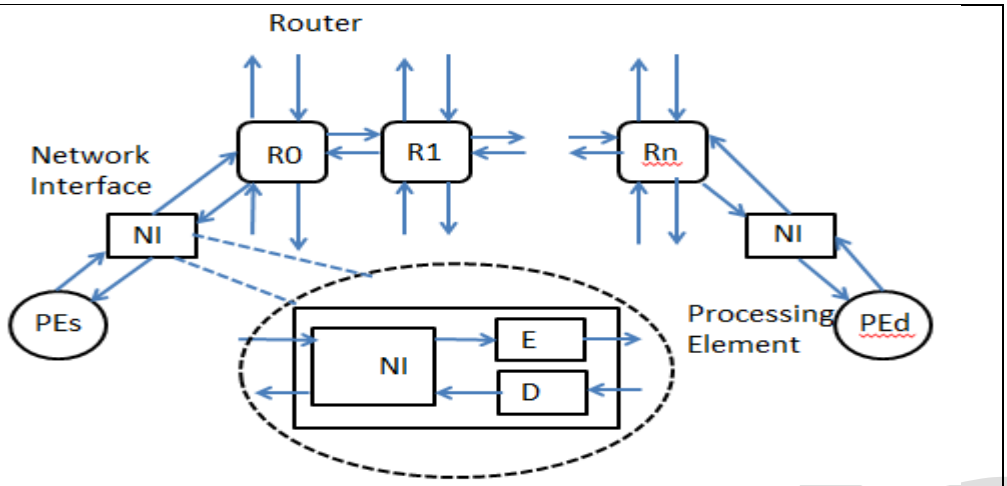

Figure1: General Architecture of Wormhole Switching

POWER MODEL

In this section we present the power model for the dynamic power consumed in the drivers and interconnect.

$$P = [T_{0\to1}(C_S + C_l) + T_c C_c]V_{dd}^2 F_{ck} \qquad (1)$$

Where C_l is the load capacitance, C_s self-switching capacitance (parallel plate capacitance and fringe capacitance), C_c is coupling capacitance, T_c, $T_{0\to1}$ are average number of transitions per clock cycle. V_{dd} Is supply voltage, F_{ck} clock frequency, $T_{0\to1}$ is number of 0→1 transitions in interconnects of two consecutive transitions. , T_c is correlated capacitance between two adjacent lines, which depends on type of transition, occurred in the lines. The total coupling capacitance changed from one type to another, therefore, T_c is the weighted sum of individual transition types (26).

$$T_c = K_1T_1 + K_2T_2 + K_3T_3 + K_4T_4 \qquad (2)$$

Where T_i,i=1,2,3,4 is the average number of type i transitions. $K_i$is the respective weight. From [26] we can use K_1=1,K_2=2 and K_3=K_4=0. K_1 Is assumed to be reference for other transition types. The effective capacitance in type2 is twice as that of type1.the probability of occurrences for random data of tye1, type2, type3,and type4 are $\frac{1}{2}, \frac{1}{8}, \frac{1}{4}, \frac{1}{4}$respectively. Hence probability of type1 is more than probability of type2.so, we concentrate on minimizing type1, thus may lead to considerable reduction in power consumption.

$$[T_{0\to1}(C_s + C_l) + (T_1 + 2T_2)C_c]V_{dd}^2 F_{ck} \qquad (3)$$

Table1 shows the relationship between the coupling transition types, if flit is transmitted as is and flit is transmitted after inversion. Consider two adjacent physical lines first bit is the value of *i*th link, second bit is the value of *i*+1 physical line. For example in first column 00→10 indicates that, in the time slot *i*lines *i* and *i*+1 have values of 0 and 0 respectively. And in next time slot this switched to 0 and 1 respectively.

Time	Normal			Odd inverted		
	Type I			Type II,III & IV		
t-1	00 11	00 11 01 10	01 10	00 11	00 11 01 10	01 10
t	10 01	01 10 00 11	11 00	11 00	00 11 01 10	10 01
	T1*	T1**	T1***	Type III	Type IV	Type II
	Type II			Type I		
t-1	01 10			01 10		
t	10 01			11 00		
	Type III			Type I		
t-1	00 11			00 11		
t	11 00			10 01		
	Type IV			Type I		
t-1	00 11 01 10			00 11 01 10		
t	00 11 10 01			01 10 00 11		

TABLE 1:Relationship Between Present Data and Previous Data in Odd inversion

Time	Normal			Even inverted		
	Type I			Type II,III & IV		
t-1	01 10	00 11 01 10	00 10	01 10	00 11 01 10	00 11
t	00 11	10 01 11 00	01 10	10 01	00 11 01 10	11 00
	T1*	T1**	T1***	Type III	Type IV	Type II
	Type II			Type I		
t-1	01 10			01 10		
t	10 01			00 11		
	Type III			Type I		
t-1	00 11			00 11		
t	11 00			01 10		
	Type IV			Type I		
t-1	00 11 01 10			00 11 01 10		
t	00 11 01 10			10 01 11 00		

TABLE 2:Relationship Between Present Data and Previous Data in Even inversion

ODD INVERSION

In this inversion scheme, we concentrate to reduce type1 transitions and type2 transitions. The scheme compares the present data with previous data to decide conversion condition. If data is odd inverted type1 transitions becomes type 3 and type4.and type2 becomes type1 transitions. Then power model is,

$$P' \alpha\ T'_{0\to1} + (K_1T'_1 + K_2T'_2 + K_3T'_3 + K_4T'_4)C_c \qquad (4)$$

Where $T'_{0\to1}$ is self-switching transition activity,T'_1,T'_2,T'_3,T'_4 are coupling transition activities of T_1,T_2,T_3,T_4 respectively. The table1 shows the relationship between the transitions when data odd inverted or if it transmitted as is.If $P>P'$.then odd invert the flit before transmit it. Using [26] we may write,

$$\frac{1}{4}T_{0\to1(odd)} + T_1 + 2T_2 > \frac{1}{4}T_{0\to0(odd)} + T_2 + T_3 + T_4 + 2T_1^{***} \qquad (5)$$

This is the condition is decide whether the data is going to be invert or not. The terms $T_{0\to0(odd)}$ and $T_{0\to1(odd)}$ are weighted factor of ¼, for the link width more than 16, the self-switching part will not affect more. By simplifying this

$$T_1 + 2T_2 > T_2 + T_3 + T_4 + 2T_1^{***} \qquad (6)$$

$$T_x = T_3 + T_4 + T_1^{***} \qquad (7)$$

$$T_y = T_2 + T_1 - T_1^{***} \qquad (8)$$

This is the simplified condition for determine whether data is going to be invert or not.

Encoding architecture:

The figure2 shows the encoder architecture based on odd inversion condition. Consider the link width w ,where one bit is used for inversion bit, which indicates that the traversed flit is inverted or not. If data is not encoded the flits are transmitted as is, by making inversion bit 0.if data inverted, the inversion bit makes 1.the w-1 bits of previous encoded data is compared with present to decide inversion condition.in the encoding logic Tx and Ty blocks takes the two adjacent bits of input lines as$X_1X_2Y_1Y_2$,$X_2X_3Y_2Y_3$,$X_3X_4Y_3Y_4$.where X_i indicates the present data and Y_i indicates the previous data. Theoutputs of T_x and T_x blocks

are 1 if detects any types. The majority voter block decides the condition (Eqn.6).If the condition is satisfied, the inversion is performed on the odd number positioned bits

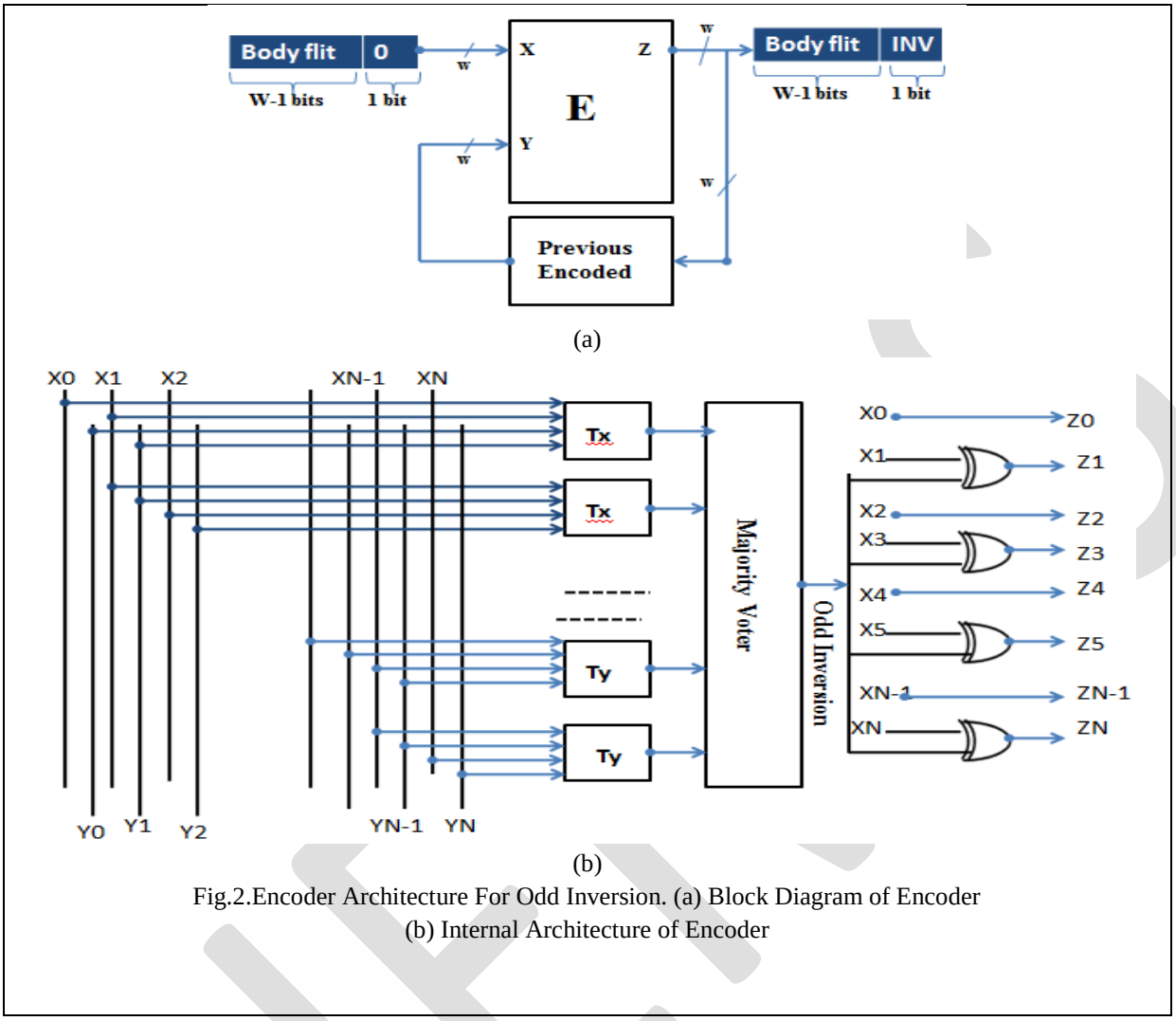

Fig.2.Encoder Architecture For Odd Inversion. (a) Block Diagram of Encoder
(b) Internal Architecture of Encoder

FULL INVERSION

Infull inversion we concentrate on both type1 and type2 transitions by use of both odd and full inversions. Type1 transitions convert to type3 and type4 transitions.type2 transitions converts to type4. Similar to previous scheme present data is compared to previous data to decide whether full, odd or no inversion. From [23] we may write

$$P'' \propto T_1 + 2T_4^{**} \qquad (9)$$

Where P'' power dissipated by the link when makes full inversion. From equations (9) and (5),

$$T_1 + 2T_4^{**} > T_2 + T_3 + T_4 + 2T_1^{***} \qquad (10)$$

Odd inversion condition is obtained as,

$$2(T_2 - T_4^{**}) < 2T_y - w + 1T_y > \frac{w-1}{2} \qquad (11)$$

Similarly condition for full inversion is from $P'' < P'$, $P'' < P$ and $T_2 > T_4^{**}$ is given by

$2(T_2 - T_4^{**}) > 2T_y - w + 1T_2 > T_4^{**}$ (12)

If none of (12) and (11) are satisfied, then no inversion is performed.

Encoding architecture:

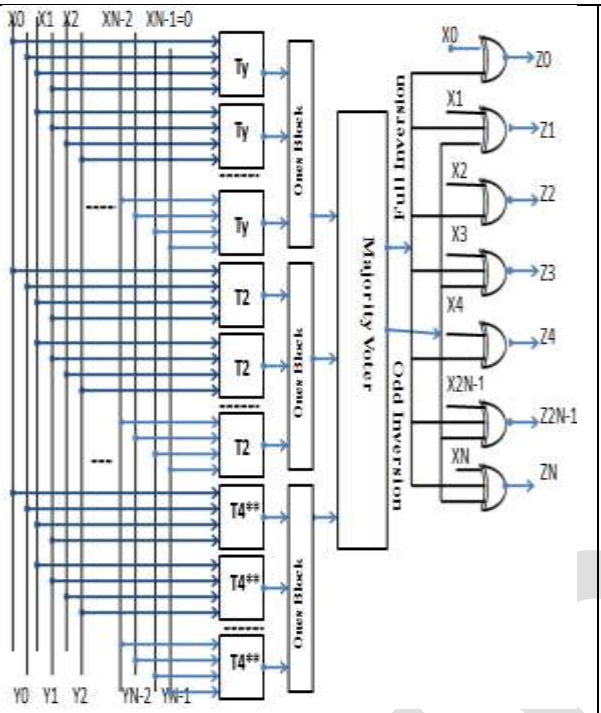

Fig 3. Encoding architecture for full inversion

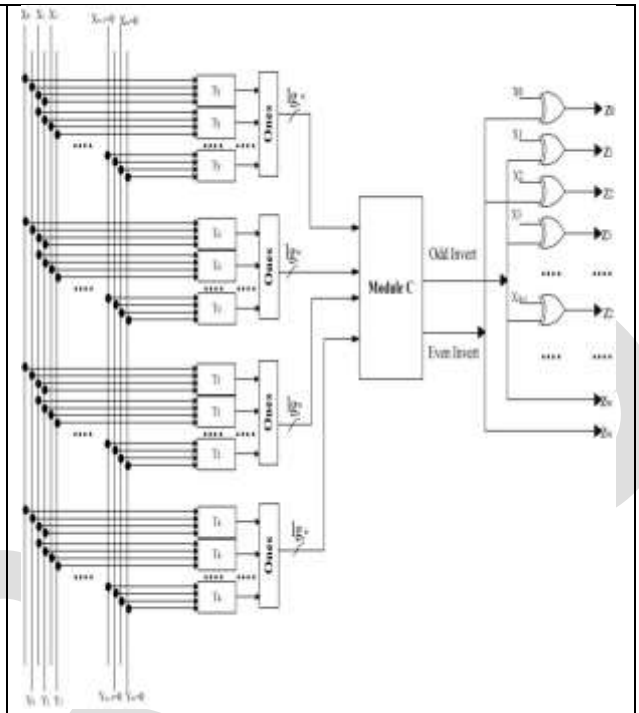

Fig 4. Encoding architecture for Even inversion

The figure3 shows the encoder architecture based on odd inversion and full inversion condition. Similar to previous encoder the link width w ,where one bit is used for inversion bit, which indicates that the traversed flit is inverted or not. If data is not encoded the flits are transmitted as is, by making inversion bit 0.if data inverted(odd/full), the inversion bit makes 1.the w-1 bits of previous encoded data is compared with present to decide inversion condition.in the encoding logic T_x,,T_2 ,T_4^{**} and Ty blocks takes the two adjacent bits of input lines as$X_1X_2Y_1Y_2$,$X_2X_3Y_2Y_3$,$X_3X_4Y_3Y_4$.where X_i indicates the present data and Y_i indicates the previous data. The outputs of T_x,T_2 ,$T_4^{**}$and T_x blocks are 1 if detects any types. The ones block counts the number of each transition by using the full adder circuit. Majority voter block decides (by using comparator block) whether odd or full inversion should be taken for link power reduction. If the condition in equation (12) or equation (11) is satisfied then output of majority voter block is '1'.the logic blocks are used to invert the flits based on the condition.

EVEN INVERSION

Here we add even inversion with the previous odd and full inversions. Since, the odd inversion converts some of type1 transitions to type2.so.if we do even inversion these type1 (T_1^{***}/T_1^{**}) transitions becomes type3 and type4.so.even inversion may leads reduce further link power consumption.table2 shows the relationship between present data and previous flit when data even inverted. Similar to previous schemes, present data is compared to previous data to decide whether even, odd or no inversion performed. Based on the analysis from odd inversion, we may write

$$T_1 + 2T_2 > T_2 + T_3 + T_4 + 2T_1^* \quad (13), \text{ defining } T_e$$

$$T_e = T_2 + T_1 - T_1^* \quad (14)$$

Similarly analysis given in full inversion, we may write the condition $P''' < P'$, $P''' < P''$ as,

$$T_2 + T_3 + T_4 + 2T_1^* < T_2 + T_3 + T_4 + 2T_1^{***} \quad (15)$$

$$T_1 + 2T_4^{**} > T_2 + T_3 + T_4 + 2T_1^* \quad (16)$$

Now define, $T_e = T_2 + T_1 - T_1^*, T_e + T_r = w - 1$ (17), where w is link width.

The full inversion leads to power reduction when $P'' < P', P'' < P, P'' < P'''$therefore condition for full inversion is obtained as,

$2(T_2 - T_4^{**}) > 2T_y - w + 1$, $2(T_2 - T_4^{**}) > 2T_e - w + 1$, $T_2 > T_4^{**}$ (18)

Condition for even inversion is obtained from $P''' < P', P''' < P$,$P''' < P''$,

$T_e > \frac{w-1}{2}$, $T_e > T_y$, $2(T_2 - T_4^{**}) < 2T_e - w + 1$ (19)

similarly condition for odd inversion is obtained as,

$2(T_2 - T_4^{**}) < 2T_y - w + 1$, $T_y > \frac{w-1}{2}, T_e < T_y$ (20)

If none of (20),(19),(18) is satisfied, no inversion is performed.

RESULTS AND DISCUSSION

Overheads due to encoder:

The encoder and the decoder were planned in Verilog HDL portrayed at the RTL level, blended with Cadence RC-compiler and mapped onto an 45-nm innovation library. In our study, the power and area of the proposed encoding Odd (O), Full (OF), and even(EOF) are looked at against SC and SCS [2], the BI coding [6], the coupling driven BI (CDBI) coding [7], and the forbidden pattern condition (FPC) codes [5],scheme I(H),scheme II (HF) and scheme III (OEF). The power and areaoverheads of the NI contrasted with the pattern NI are indicated in Fig. 5and Fig.6.here we consider the 32 bit data with 5*5 mesh structure.

Power analysis

To get the outcomes for total power and energy sparing indicated in Fig. 7, we have considered all the interconnect NoC parts, including connection, switch, encoder, link, also, NI. This a piece of NoCpower/energy utilization constitutes an imperative division of the general power financial plan of the total system.

Fig.8 demonstrates the lessening in the switching moves of type II, and coupling exchanging action for diverse information encoding plans contrasted with those of no information encoding. It demonstrates that the proposed encoding plans diminish type II. In the instances of past encoding plans (SCS, SC, BI, CDBI,H,HF,OEFand FPC) just Type II declines. Compared to previous encoding techniques the proposed Odd (O), Full (OF), and even(EOF) we get less percentage of toggle rate.

CONCLUSION

In this paper, we have displayed an arrangement of new information encoding plans went for lessening the power scattered by the connections of a NoC. Actually, connections are in charge of a huge portion of the general force dispersed by the correspondence system. What's more, their commitment is required to increment in future innovation hubs. When contrasted with the past encoding plans proposed in the writing, the basis behind the proposed plans is to minimize not just the switching action, additionally the coupling exchanging action which is principally in charge of connection powerdissemination in the profound submicronmeter innovation administration. The proposed encoding plans are matched with deference to the fundamental NoC building design as in their application does not require any alteration neither in the switches nor in the connections. The utilization of the proposed encoding plans permits investment funds up to 35% of power scattering and 17% of energy utilization with no huge execution debasement and with under 15% region overhead in the NI

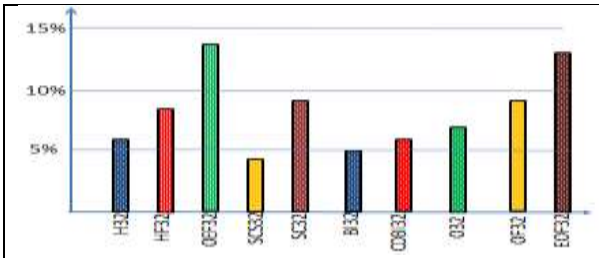

Fig 5:Percentage impact on power dissipation of the network interface due to the data encoding logic

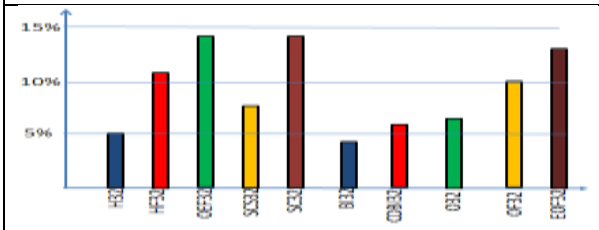

Fig 6:Percentage impact on silicon area of the network interface due to the data encoding logic

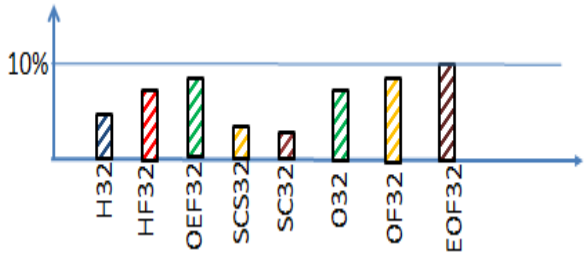

Fig7:Total power savings using different data encoding techniques

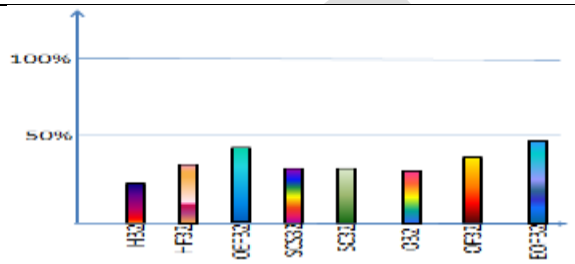

Fig 8:percentage decrease in type II transitions

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