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G_m/I_D based Three stage Operational Amplifier Design

Rishabh Shukla
SVNIT, Surat
shuklarishabh31081988@gmail.com

Abstract— A nested Gm-C compensated three stage Operational Amplifier is reviewed using g_m/I_D based approach. With the given specifications such as Gain, Phase Margin, Input common mode range and Unity gain frequency, operational amplifier has been designed in such a way that all the transistors are biased in moderate inversion. Spice simulations are carried out using TSMC 180 nm technology. The simulated results show agreement with the specification for 1.8 V supply.

Keywords— CMOS Integrated Circuit, Low power, Stability, Compensation, Nested G_m-C compensation, Gain margin, Phase margin, Pole, Zero.

INTRODUCTION

The operational amplifiers (Op-amp) are most important building block of many analog and mixed signal circuits like amplifiers, filters, comparators etc. With the scaling of transistors and supply, now a day's multistage amplifiers are often used. In low voltage designing cascoding can't be used because of headroom limitations. Hence designer has been moved towards cascading, because it avoids vertical stacking of transistors hence removes the headroom problem. In order to achieve a high voltage gain, it is advantageous to used more than two stages. But to design such a multistage operational amplifier is a challenging task since high impedance nodes lead instability issues. To stabilize the op-amp several compensation techniques has been proposed [1]. The Nested miller compensation (NMC) technique suffers from bandwidth reduction, issue while NMC with nulling resistor suffers from right half plane zero problems [2,3]. The multipath NMC (MNMC) increases the bandwidth by cancelling the non-dominant pole with zero. Major drawback of this technique is that slight variation in temperature or any other parameter may change the location of zero, which leads improper cancellation [4]. The reversed NMC (RNMC) introduces the right half plane zero, hence decreases the bandwidth and phase margin [5]. The nested G_m-C compensation technique is much easier to analyze as compare to MNMC. The power consumption by feed-forward stages can be controlled by proper implementations [6,7]. In this paper nested G_m-C compensation technique has been adopted for three stage op-amp designing.

DESIGN APPROACH

The G_m/I_D based technique has been adopted to bias all the transistors in moderate inversion in order to achieve best trade-off among gain, bandwidth and power. In this methodology transistors are characterized under same environment to plot the intrinsic gain and $I_D/(W/L)$ as a function of G_m/I_D. G_m/I_D is a ratio which measures the efficiency to translate current into transconductance, i.e. large transconductance can be achieved by making the ration large [8,9]. Since the above plots are independent to size hence it becomes quite easy to size each transistor for a given current. The required current can be obtained from specifications. The transfer function of three stage op-amp can be written as,

$$A(s) = -\frac{A_o}{\left[\left(1+\frac{A_O s}{\omega_1}\right)\left(1+\frac{s}{\omega_2}+\frac{s}{\omega_2\omega_3}\right)\right]}$$

In this expression A_o is open loop gain and ω_1 is unity gain frequency. In order to make op-amp as single pole system it is necessary that both second and third pole must be far from UGB. Hence in this way op-amp can be stabilize but it consumes large power [7].

[1] SPECIFICATIONS

In order to design three stage op-amp following specification has been used,

1. Supply, V_{DD} = 1.8V and V_{SS} = 0V.
2. Gain > 80 dB
3. GBW > 20 MHz
4. ICMR = 0 to 1.5V
5. Phase Margin = 50^o to 60^0

[2] DESIGN EQUATIONS

Following relations has been adopted,

1. $\mathrm{UGB} = \frac{G_{m1}}{2\pi C_{m1}}$

2. $P_1 = \frac{G_{m2}}{2\pi C_{m2}}$, $P_2 = \frac{G_{m3}}{2\pi C_L}$

3. $G_{mfi} = G_{mi}$ for i = 1 to 3

4. $V_{cm}(+) = -|V_{Tpmax}| - V_{SDsat1} + V_{DD}$

5. $V_{cm}(-) = -|V_{Tpmax}| + V_{SDsat2} + V_{DSsat4}$

6. $\mathrm{PM} = 90^{0} - \tan^{-1}\{\frac{\frac{\omega_1}{\omega_2}}{1-\frac{\omega_1^2}{\omega_2\omega_3}}\}$

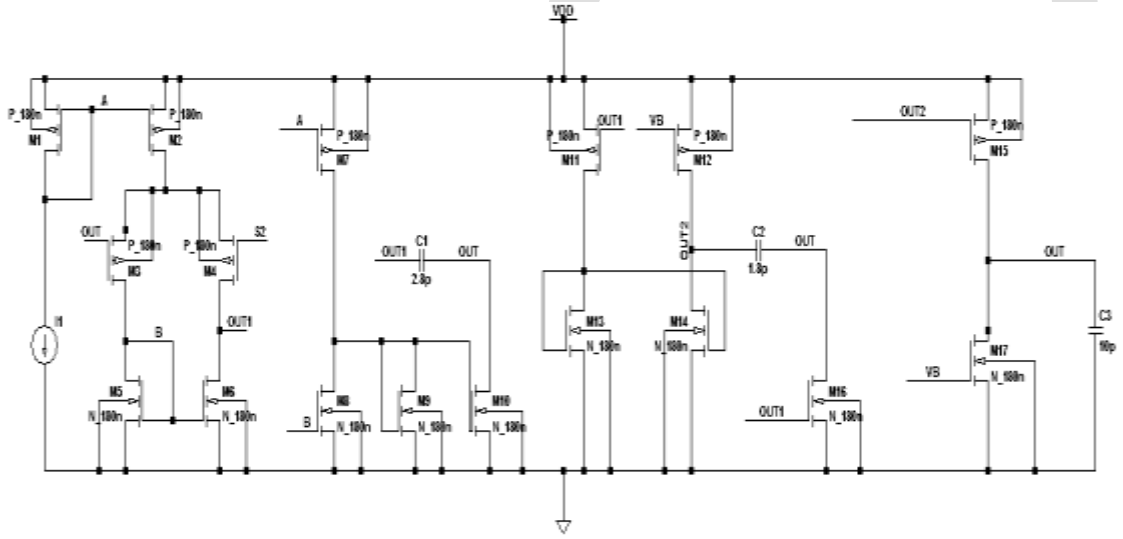

Figure 1: Three stage NGCC Op-amp [7]

[3] DESIGN PARAMETERS AND TRANSISTORS SIZE

With the help of above specifications, design equations and G_m/I_D plots aspect ratios of all the transistors has been calculated and simulated results for size of transistors belong to core block has been summarized in Table 1.

Table1: Summary of size of transistors after simulation

Transistors	W/L ratio (Simulated value)
M_3,M_4	31.66/0.5
M_5,M_6	7/0.5
M_{11},M_{12}	22/0.5
M_{13},M_{14}	7/0.5
M_{15}	58/0.36
M_{17}	30/0.5

The bias current for first stage current mirror has been chosen as 10 µA.

SIMULATION RESULTS

The SPICE simulation has been carried out using TSMC 180nm technology. The supply has been chosen as 1.8V and the simulated results have been summarized in Table 2.

1. FREQUENCY RESPONSE

The simulated result shows that op-amp has an open loop gain of 94.23 dB, UGB is 27 MHz and phase margin is 60^{o} for 10 pF capacitive load.

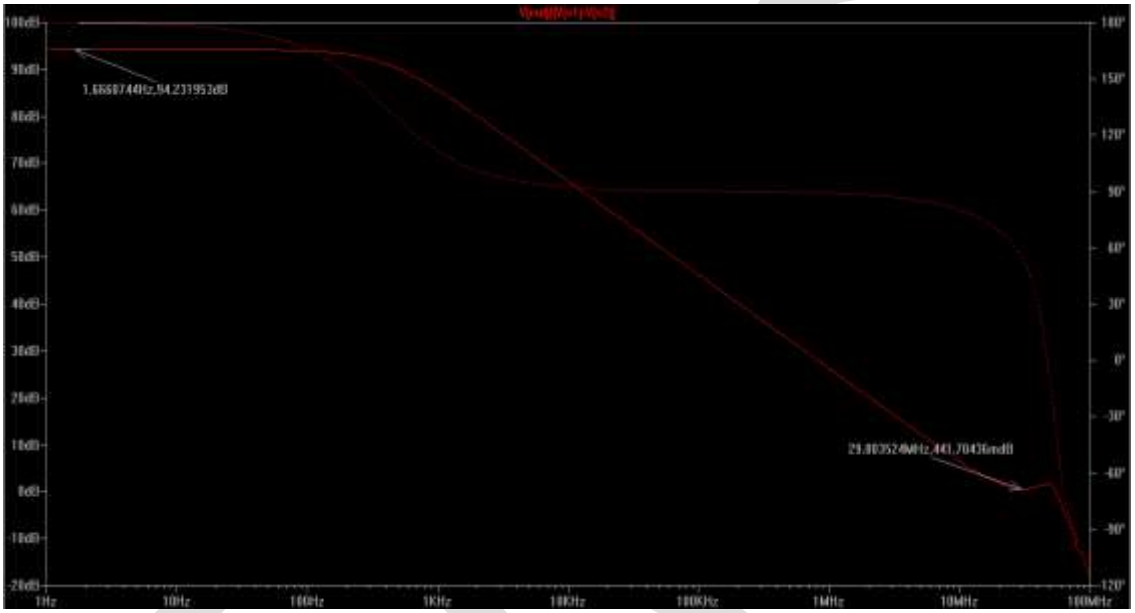

Figure 2: Frequency Response of Three stage Op-amp for a 10 pF capacitive load

2. Input Common mode range

The simulated result shows that designed op-amp has ICMR in the range of 64 mV to 1.78 mV.

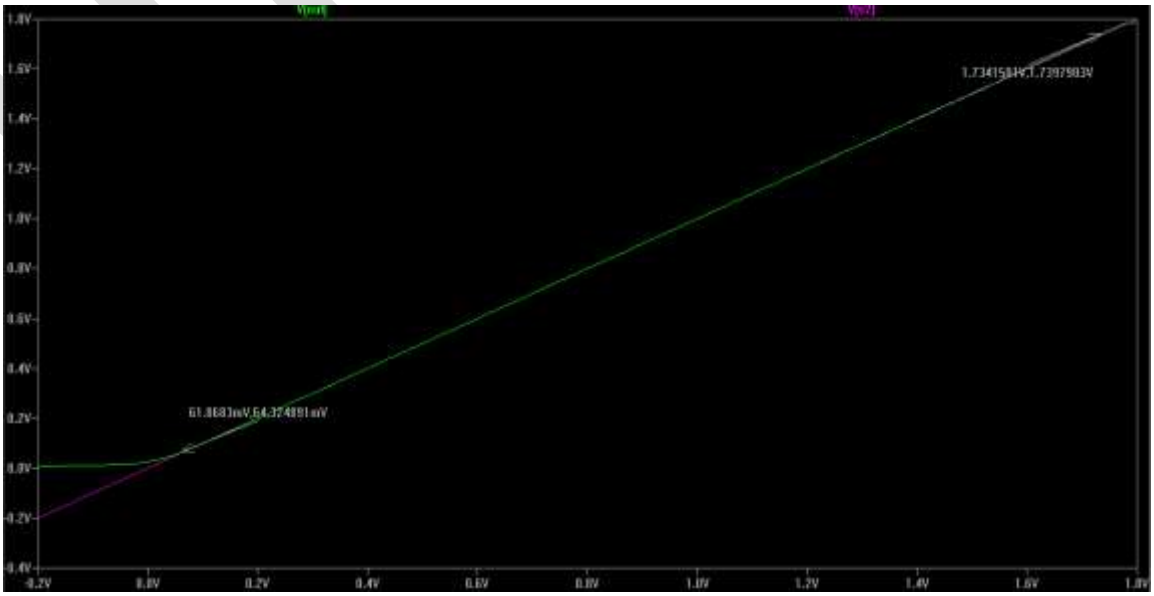

Figure 3: Frequency Response of Three stage Op-amp for a 10 pF capacitive load

3. Step Response: An step of 0V to 1.2V is applied across unity gain opamp and output has been plotted as sjown in Figure 3.

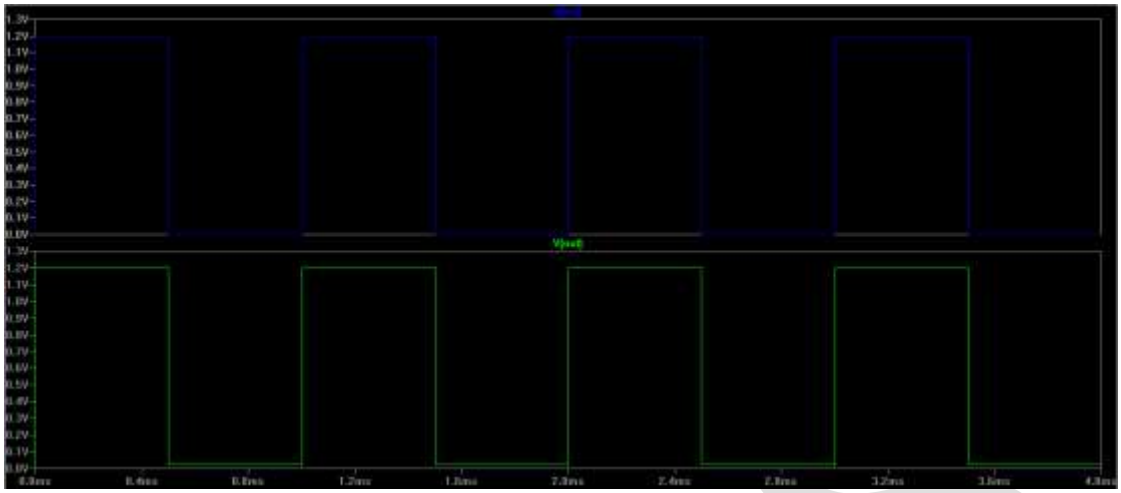

Figure 4: Step Response of unity gain op-amp

4. Slew Rate and offset voltage of Op-amp

Slew rate of simulated op-amp has been found as 15 V/μs and off-set voltage is almost 26 mV.

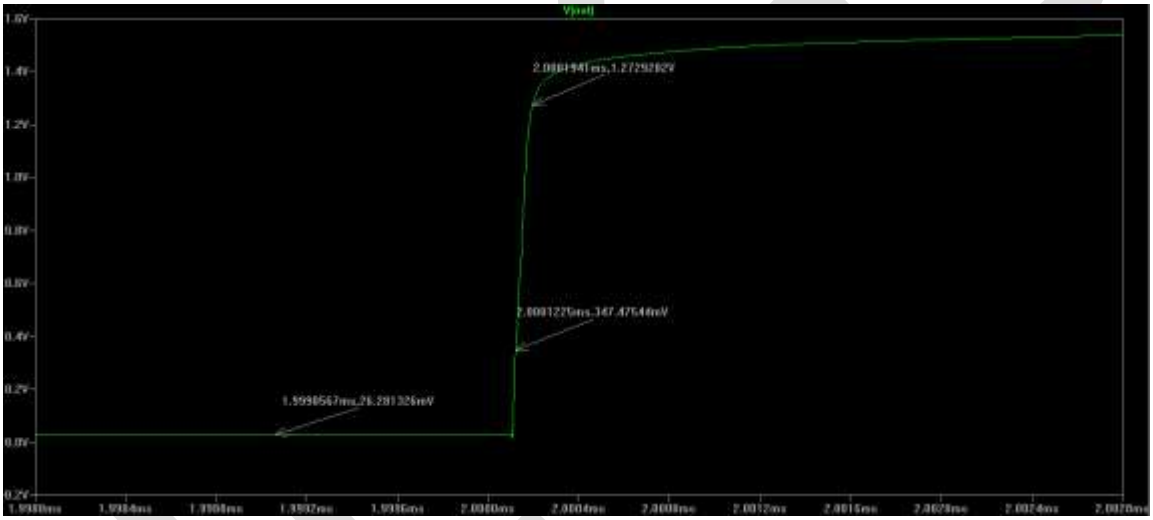

Figure 5: Large signal step response of unity gain opamp for offset voltage and slew rate calculation

The simulated results have been summarized in Table 2.

Table 2: Comparison of parameters for 5pF and 10pF load

Parameter	Simulated Value	
	C_L = 5 pF	C_L = 10 pF
Gain	94.23 dB	94.23 dB
UGB	23.94 MHz	29.8 MHz
Phase Margin	69^o	52.55^o
Slew Rate	15.6 V/μs	14.5 V/μs
ICMR	64 mV- 1.73mV	64 mV - 1.74mV
Offset Voltage	26 mV	26 mV
Settling Time	80 ns	85 ns
Power Consumed (I_{VDD}x V_{DD})	2.86 mW	2.86 mW

CONCLUSION

In this paper a three stage nested G_m-C compensated operational amplifier has been designed using G_m/I_D methodology and 180 nm technology. All the transistors are biased in moderate inversion region in order to achieve best tradeoff among gain, area, and bandwidth. The simulated results show that op-amp is capable to give an open loop gain of 94.23 dB at a phase margin of 69^0 and UGB of 23.94 MHz for 5 pF load and 52.55^0, 29.8 MHz for 10 pF capacitive loads. Hence simulated result shows excellent agreement

with specifications.

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