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Review on Sigma-Delta Modulator

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Abstract— In this paper detailed study of Sigma- Delta (Σ-Δ) modulator has been discussed and analyzed. Low power Σ-Δ ADC for various applications has been discussed. Use of oversampling ratio in designing of Σ-Δ ADC for reduction of noise as well as for better resolution has been analyzed theoretically and practically.

Keywords— Sigma- Delta (Σ-Δ) modulator, Oversampled ADC, Resolution.

INTRODUCTION

Emergence of powerful digital signal processors implemented in CMOS VLSI technology creates the need for high-resolution analog-to-digital converters that can be integrated in fabrication technologies optimized for digital circuits and systems. Depending on the ratio of sampling, the analog to digital converters can be divided into two categories. The first category is the Nyquist rate ADCs in which the input data is sampled at the Nyquist rate and the other type called oversampling ADCs, samples the signal at a rate much higher than the Nyquist rate.[1] The Block diagram of the Oversampling ADC is shown below.

Building Blocks of Oversampling ADC

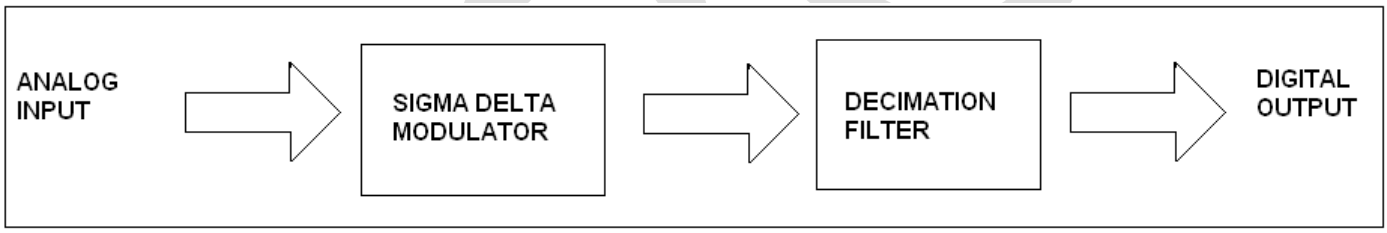

Fig. 1: Block Diagram of Oversampling ADC

OVERSAMPLING ADC

ADC can be separated into categories depending on the rate of sampling. The first category samples the input at the Nyquist rate,or fN =2F, where F is the bandwidth of the signal and fN is the sampling rate. The second type samples the signal at a rate much higher than the signal bandwidth. This type of converter is called an oversampling converter. Traditionally, successive approximation or dual slope converters are used when high resolution is desired. However, trimming is required when attempting to achieve higher accuracy. Dual slope converters require high speed, high accuracy integrators. That is only available using a high fT bipolar process. To design a high-precision sample and hold is another factor that limits the realization of a high resolution ADC using these architectures. The oversampling ADC is able to achieve much higher resolution than the Nyquist rate converters. This is because digital signal processing techniques are used in place of complex and precise analog components. The accuracy of the converter does not depend on the component matching, precise sample –and –hold circuitry, or trimming, and only a small amount of analog circuitry is required. Switched capacitor implementations are easily achieved, and as a result of the high sampling rate, only simplistic anti-aliasing circuitry needs to be used. However because of the amount of time required to sample the input signal, the throughput is considerably less than the Nuquist rate ADCs.[1]

BLOCK DIAGRAM

The block diagram of Low power Sigma-Delta Modulator ADC is given below.

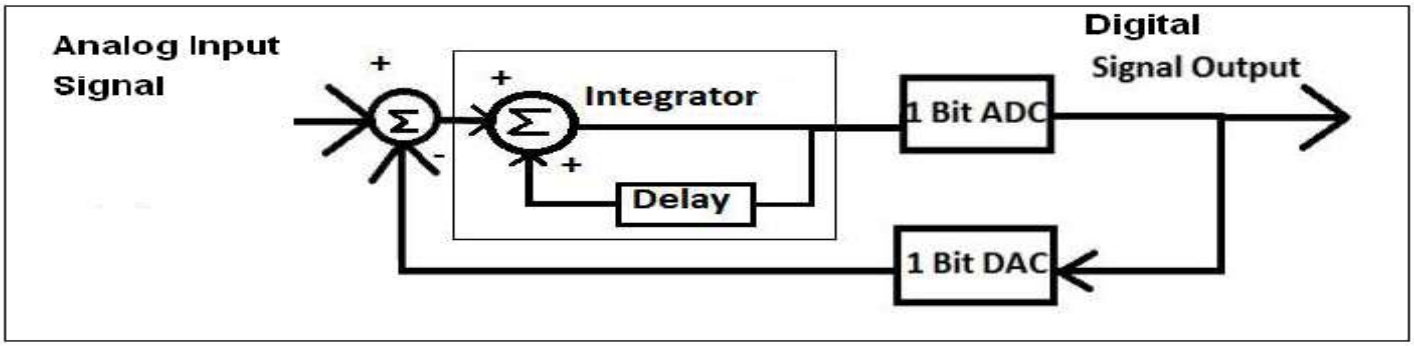

Fig 2. First-order Sigma-Delta Modulator.

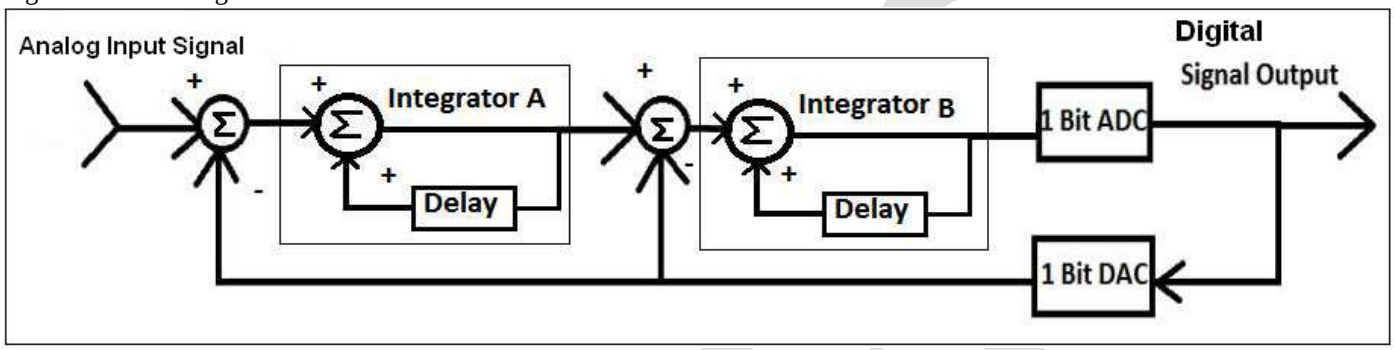

Fig 3. Second-order Sigma-Delta Modulator.

A comparative study of different Sigma-Delta modulator used for different applications designed and developed by different authors is shown below.

Paper Name	A 15 Bit 95 dB Low Power Discrete Time Sigma Delta Modulator	Bandpass Sigma-Delta Modulator for Sensor Signal Processing	First-Order Continuous-Time Sigma-Delta Modulator
Authors	1. Mohammed ArifuddinSohel 2. K. ChennaKeshava Reddy 3. Syed Abdul Sattar 4. Salma Jabeen	1. Lukáš Fujcik 2. Radimír Vrba	1. Yamei Li , San Jose State University, USA 2. Lili He , San Jose State University, USA
Abstract	In this paper high resolution low power sigma delta modulator over 5MHz at a sampling frequency of 1Ghz has been developed in which Signal to Quantization Noise Ratio (SQNR) of 95.3dB, leading to a 15 bit resolution of the ADC. A very low power consumption of 2.3mW at a supply voltage of 1.8V is achieved in 0.18micron CMOS technology. The 60 meter band or 5 MHz band is a relatively new amateur radio band that is useful for disaster management and this paper presents an ADC that can be used for this band.	Here, system architecture for sensor signal digitization utilizing a band pass sigma-delta modulator in 5V 0.7µm CMOS technology has been implemented for impedance spectroscopy, capacitive pressure sensor measurement and wireless applications.	In this paper first-order continuous-time sigma-delta modulator in 0.18 um CMOS technology that achieves a level of 60 dB SNR has been designed which operates at 1.8 V supply voltage. It can accept input signal bandwidth of 10 kHz with oversampling ratio of 250.
Paper Name	Sigma delta and multi-stage sigma delta modulation with inside loop dithering	Modeling and design of novel architecture of multibit switched-capacitor sigma-delta converter with two-step quantization process	A Mixed-Signal Architecture of Channel Select Filtering with Oversampled ADC for Multi-Standard RFID Reader Receiver
Authors	1.W. Chou , AT&T Bell Lab. 2.Murray Hill, NJ, USA	1.Lukas Fujcik , BUT FEEC, Udolni 53, CZ-602 00 Brno, Czech Republic 2.Jiri Haze , BUT FEEC, Udolni 53, CZ-602 00 Brno, Czech Republic RadimirVrba , BUT FEEC, Udolni 53, CZ-602 00 Brno, Czech Republic 3.ThibaultMougel , South Queensferry, Edinburgh EH30 9TG, Scotland	1.Hin-Tat Chan 2.Hong Kong Univ. of Sci. & Technol., Hong Kong 3.Wenting Wang ; Chi Fung Lok ; Lau, V.K. ; Chi-yingTsui ;

Abstract	In this paper dithering inside the loop of sigma-delta and multistage sigma-delta modulators is studied. For a multistage sigma-delta modulation system, inside-the-loop dithering makes the quantization error white for a system with three stages.	The two-step quantization technique was utilized to design of sigma-delta modulator. Parameters of decimation filter are derived from the specifications of the overall sigma-delta modulator. The architecture of switched-capacitor (SC) sigma -delta modulator was designed with sampling jitter, noise, and operational amplifier parameters such as white noise, finite dc gain, finite bandwidth, slew rate and saturation voltages.	In this paper a highly reconfigurable mixed-signal architecture for channel select filtering with the help of oversampled delta-sigma modulator is implemented which allows the RFID reader to support multi-standard operating environment with low power consumption and silicon area for single-chip implementation compared with pure analog or digital channel select filtering approach.
Paper Name	Oversampled ADC based on pulse frequency modulator and TDC	24-bit Low-Power Low-Cost Digital Audio Sigma-Delta DAC	A Continuous Time Sigma Delta Modulator With Operational Floating Integrator
Authors	1. Hernandez, L. Electron. Technol. Dept., Carlos III Univ., Madrid, Spain 2. Gutierrez, E.	1.LIU Yuyu 2.GAO Jun 3.YANG Xiaodong	1.DragosDucu*, 2.AncaManolescu** *Microchip Technology, Bucharest Romania E-mail: dragos.ducu@microchip.com **"POLITEHNICA" University of Bucharest E-mail: ammanolescu@yahoo.com
Abstract	In this paper the ring oscillator is replaced by a pulse frequency modulator (PFM) that provides improved linearity at the expense of feedback and analogue amplification is proposed. Compared to the equivalent continuous time sigma-delta modulators, the PFM may be more tolerant to circuit impairments. In addition, the output data of the proposed architecture is a multibit sequence through the use of a time-to-digital converter TDC instead of a Flash quantiser or a multibit digital-to-analogue converter. A high dynamic range can be achieved without severe constraints on analogue mismatch or clock jitter.	This paper presents a low-power low-cost 24-bit Σ-Δ digital-to-analog converter (DAC) in which a 15-level quantizer, third-order, single-stage Σ-Δ modulator is employed to reduce the passband quantization noise, relax the out-of-band filtering requirements, and enhance immunity to clock jitter for portable digital audio applications. A direct charge transfer switched-capacitor low-pass filter (DCT-SC LPF) is used to reconstruct the analog signal to reduce the kT/C noise and capacitor mismatch effect with a small increase of the power dissipation. The chip was fabricated in the SMIC 0.13 μm 1P5M CMOS process. The cell area of the digital part is 0.056 mm2 and the total area of the analog part is 0.34 mm2. The supply voltage is 1.2 V for the digital circuit and 3.3 V for the analog circuit. The power consumption of the analog part is 3.5 mW. The audio DAC achieves a 100 dB dynamic range and an 84 dB peak signal-to-noise-plus-distortion ratio over a 20 kHz passband.	In this sigma delta convertor for implementation of integrators in loop filter, operational floating conveyors are employed. The modulator is designed in 0.18um TSMC CMOS technology and features low power consumption (<3mW), low supply voltage (±1.8), and wide dynamic range (>70db).
Paper Name	A high-performance accelerometer with a fifth-order sigma–delta modulator	First Order Sigma-Delta Modulator Of An Oversampling Adc Design In Cmos Using Floating Gate MOSFETS	Design Of First Order And Second Order Sigma Delta Analog To Digital Converter
Authors	1.Yufeng Dong, 2.Michael Kraft, 3.Carsten Gollasch and 4.William Redman-White	1.Syam Prasad SBS Kommana Bachelor of Technology, Nagarjuna University, 2001 December 2004	1.Vineeta Upadhyay and 2.Aditi Patwa Department of ECE, Amrita School of Engineering, Bangalore, Karnataka, India.
Abstract	a micromachined accelerometer fabrication is mentioned. The in-plane sensor with fully differential structure has a mechanical noise floor below 1 μg $Hz^{-1/2}$, static sensitivity 16 pF g^{-1} and resonant frequency 325 Hz. FEM analyses are performed to verify these key parameters. The silicon-on-glass sensor is fabricated by deep reactive ion etching (DRIE) and anodic bonding. Compared with a second-order electromechanical ΣΔM, which only uses the sensing element as a loop filter, here it is cascaded with additional electronic integrators to form a fifth-order electromechanical ΣΔM, which leads to better signal to quantization noise ratio (SQNR). This novel approach is analysed	A new architecture for a sigma-delta oversampling ADC in which the first order modulator is realized using the floating gate MOSFETs at the input stage of an integrator and the comparator has been implemented. The first order modulator is designed using an 8 MHz sampling clock frequency and implemented in a standard 1.5μm n-well CMOS process. The decimator is an off-chip sinc-filter and is programmed using the VERILOG and tested with Altera Flex EPF10K70RC240 FPGA board. The ADC gives an 8-bit resolution with a 65 kHz bandwidth.	This paper presents the design of a first order and second order single bit Sigma-Delta Analog-to-Digital Converter (ADC) which is realized using CMOS technology. In this paper, a first Order and Second order Sigma-Delta ADC is designed which accepts an input signal of frequency 1 KHz, an OSR of128, and 256 KHz sampling frequency .It is implemented in a standard 90nm CMOS technology. The ADC operates at 0.5V reference voltage. The Design and Simulation of the Modulator is done using H-spice. This paper firstly elaborates Summer, Integrator, Comparator, D-Latch and DAC which is integrated together to form.

	and system level simulations are presented. A printed circuit board (PCB) prototype of this high-order ΣΔM loop was built and tested.		
Paper Name	A 1.8-V digital-audio sigma-delta modulator in 0.8-µm CMOS (1997)	Design of Low Power Sigma Delta ADC	Digital Power Amplification Using Sigma-Delta Modulation and Bit Flipping
Authors	1.Shahriar Rabii , 2.Shahriar Rabii , 3.Bruce A. Wooley , 4.Shahriar Rabii , 5.Shahriar Rabii , 6.Bruce A. Wooley	1Mohammed Arifuddin Sohel, 2.Chenna Kesava Reddy, 3.Syed Abdul Sattar	1. Anthony J Macgrath, 2.Mark B. Sandler
Abstract	Oversampling techniques based on sigma-delta (ΣΔ) modulation offer numerous advantages for the realization of high-resolution analog-to-digital (A/D) converters in a low-voltage environment. This paper examines the design and implementation of a CMOS ΣΔ modulator for digital-audio A/D conversion that operates from a single 1.8-V power supply. A cascaded modulator that maintains a large full-scale input range while avoiding signal clipping at internal nodes is intduced. The experimental modulator has been designed with fully-differential (ΣΔ)switched-capacitor integrators employing different input and output common-mode levels and boosted clock drivers in order to facilitate low voltage operation. Precise control of common-mode levels, high power supply noise rejection, and low power dissipation are obtained through the use of two-stage, class A/AB operational amplifiers. At a sampling rate of 4 MHz and an oversampling ratio of 80, an implementation of the modulator in a 0.8-µm CMOS technology with metal-to-polycide capacitors and NMOS and PMOS threshold voltages of +0.65-V and –0.75-V, respectively, achieves a dynamic range of 99 dB at a Nyquist conversion rate of 50 kHz. The modulator can operate from supply voltages ranging from 1.5 V to 2.5 V, occupies an active area of 1.5 mm 2, and dissipates 2.5 mW from a 1.8-V supply.	A Low power discrete time sigma delta ADC consisting of a second order sigma delta modulator and third order Cascaded Integrated Comb (CIC) filter is proposed. The second order modulator is designed to work at a signal band of 20K Hz at an oversampling ratio of 64 with a sampling frequency of 2.56 MHz. It achieves a signal to noise ratio of 85.2dB and a resolution of 14 bits. The CIC digital filter is designed to implement a decimation factor of 64, operating at a maximum sampling frequency of 2.56 MHz. A second order sigma delta modulator is implemented in 0.18micron CMOS technology using full custom design and the third order digital CIC decimation filter is implemented in verilog HDL. The complete Sigma Delta ADC, consisting of analog block of second order modulator and digital block of decimator consumes a total power 1.96mW.	A data conversion technique suitable for digital power amplifiers (DPAs) is described, based on a modified sigma-delta modulator. The pulse-repetition frequency (PRF) in the bit stream is reduced in order to increase the efficiency in the power output switching stage. The system offers PRFs comparable to pulse-width-modulation (PWM)-based DPAs, but with higher linearity and more than a thirty-fold reduction in bit-clock frequency.

Paper Name	Design and Development of Sigma-Delta Modulator	Linearization of Thermocouple Signals by ADC	Second Order Sigma-Delta Modulator-a Linearizing unit of Thermocouple

Authors	1Lalita Yadav, 2Vedanta Kuri, 3Abir Chattopadhyay	Vedanta Kuri Abir Chattopadhyay	Vedanta Kuri, Abir Chattopadhyay
Abstract	A low cost, highly resolution analog to digital converter is being designed and developed in our laboratory. Based on characteristics, a comparative study of different ADC is being made. Sigma delta modulator has been chosen for its better latency and throughput.	A novel linearizing circuit for linearization of thermocouple signals by ADC has been designed and developed. Sigma-Delta ADC has been considered in this proposed simpler circuit. Computational studies carried on material gives satisfactory results for the thermocouple.	Linearization is necessary when sensors produce voltage signal that are not linearly related to the physical measurement. It is the process of interpreting the signals from the transducer and can be done either with signal conditioning orthrough software. Different linearization mechanisms are available. In this paper a sigma delta ADC [1-3] is used for linearization of thermocouple signals. Thermocouple signal are of Non-linear type. To convert Non-linear form to linear form, a second order sigma-delta ADC has been introduced and developed for much better accuracy. Computational analysis has been fulfilled for J and K type thermocouple.
Paper Name	A low power Delta-Sigma Modulator Using a Charge-Pump Integrator	Incremental Data Converters at Low Oversampling Ratios	A 12-bit 3.125 MHz Bandwidth 0–3 MASH Delta-Sigma Modulator
Authors	Alireza Nilchi, Student Member, David A Johns, Fellow, IEEE	Trevor C. Caldwell, *Student Member, IEEE*, and David A. Johns, *Fellow, IEEE*	Ahmed Gharbiya, *Member, IEEE*, and David A. Johns, *Fellow, IEEE*
Abstract	In this paper a low-power switched-capacitor integrator based on a capacitive charge-pump (CP) is presented. The 0.13 m CMOS prototype of the CP based ADC achieves the same performance as a conventional ADC while consuming 66% lower OTA power in the front-end integrator. The CP based modulator realizes 87.8 dB SNDR, 89.2 dB SNR and 90 dB DR over a 10 kHz bandwidth with 148 W power consumption. The conventional ADC has similar performance but dissipates 241 W. The energy required per conversion-step for the CP based ADC (0.369 pJ/step) is almost 40% lower than that of the conventional ADC (0.607 pJ/step).	In this paper the use of incremental A/D converters with low oversampling ratios is proposed. Incremental A/D converters are able to achieve a higher SQNR than delta-sigma modulators at oversampling ratios below 4, allowing them to operate as higher bandwidth converters with medium resolution. The impact of removing the input S/H, as well as analyzing their behaviour at an OSR as low as 1 is explored. An eighth-order cascaded incremental A/D converter is analyzed and shown as an example.	In this paper a 12-bit 0–3MASHdelta-sigma modulator with a 3.125 MHz bandwidth in a 0.18 m CMOS technology is implemented. The modulator has an oversampling ratio of 8 (clock frequency of 50 MHz) and achieves a peak SNDR of 73.9 dB (77.2 dB peak SNR) and consumes 24mWfrom a 1.8 V supply. For comparison purposes, the modulator can be re-configured as a single-loop topology where a peak SNDR of 64.5 dB (66.3 dB peak SNR) is obtained with 22 mW power consumption. The energy required per conversion step for the 0–3MASHarchitecture (0.95 pJ/step) is less than half of that required by the feedback topology (2.57 pJ/step).
Paper Name	Combining Multipath and Single-Path Time-Interleaved Delta-Sigma Modulators	On The Implementation of Input-Feedforward Delta–Sigma Modulators	A Time-Interleaved Continuous-Time ΔΣ Modulator With 20-MHz Signal Bandwidth
Authors	Ahmed Gharbiya and David A. Johns	Ahmed Gharbiya, *Student Member, IEEE*, and D. A. Johns, *Fellow, IEEE*	Trevor C. Caldwell, *Student Member, IEEE*, and David A. Johns, *Fellow, IEEE*

Abstract	Here single-path time-interleaved delta-sigma modulators are analyzed and evaluated. It is found that finite opamp gain and bandwidth result in a mismatch between the noise transfer functions of the internal quantizers which degrades the performance of the architecture. A hybrid topology where the first stage uses multiple integrators while the rest of the modulator uses a single path of integrators is proposed to mitigate the mismatch problem.	Here some practical issues on the implementation of the input-feedforward delta–sigma modulators has been proposed. First, the timing constraint imposed by the input-feedforward path is identified and a possible method to relax the constraint is proposed. Second, the drawbacks of the analog adder needed before the quantizer are explained and a method to eliminate the adder is proposed.	In this paper the first implementation results for a time-interleaved continuous-time $\Delta\sum$modulator is implemented. The derivation of the time-interleaved continuous-time $\Delta\sum$ modulator from a discrete-time $\Delta\sum$ modulator is presented. With various simplifications, the resulting modulator has only a single path of integrators, making it robust to DC offsets. A time-interleaved by 2 continuous-time third-order low-pass $\Delta\sum$ modulator is designed in a 0.18- m CMOS technology with an oversampling ratio of 5 at sampling frequencies of 100 and 200 MHz. Experimental results show that a signal-to-noise-plus-distortion ratio (SNDR) of 57 dB and a dynamic range of 60 dB are obtained with an input bandwidth of 10 MHz, and an SNDR of 49 dB with a dynamic range of 55 dB is attained with an input bandwidth of 20 MHz. The power consumption is 101 and 103 mW, respectively.
Paper Name	High-Speed Oversampling Analog-To-Digital Converters	Time-Interleaved Oversampling A/D Converters: Theory and Practice	Design and Analysis of Delta-Sigma Based IIR Filters
Authors	Ahmed Gharbiya, Trevor C. Caldwell, And D. A. Johns Department of Electrical and Computer Engineering, University of Toronto 10 King's College Rd., Toronto, Ontario, CANADA, M5S 3G4	Ramin Khoini-Poorfard, *Member, IEEE*, Lysander B. Lim, *Member, IEEE*, and David A. Johns, *Senior Member, IEEE*	David A. Johns, and David M. Lewis, Member IEEE
Abstract	This paper is mainly tutorial in nature and discusses architectures for oversampling converters with a particular emphasis on those which are well suited for high frequency input signal bandwidths. The first part of the paper looks at various architectures for discrete-time modulators and looks at their performance when attempting high speed operation. The second part of this paper presents some recent advancement in time-interleaved oversampling converters. The next section describes the design and challenges in continuous-time modulators. Finally, conclusions are made and a brief summary of the recent state of the art of high-speed converters is presented.	In this paper, the design procedure and practical issues regarding the realization of time-interleaved oversampling converters are presented. Using the concept of block digital filtering, it is shown that arbitrary $\Delta\sum$ topologies can be converted into corresponding time-interleaved structures. Practical issues such as finite op amp gain, mismatching, and dc offsets are addressed, analyzed and practical solutions to overcome some of these problems are discussed. To verify the theoretical results, a discrete-component prototype of a second-order time-interleaved $\Delta\sum$ analog/digital (A/D) converter has been implemented and the design details as well as experimental results are presented.	This paper presents design techniques for IIR filters operating on oversampled delta-sigma ($\Delta\sum$) modulated signals. It is shown that $\Delta\sum$ -based IIR filters can be efficiently realized by eliminating all multibit multipliers through the use of re-modulating internal filter states. As well, noise results are presented showing that linear noise analysis gives excellent predictions of the noise performance over the frequency band of interest. Finally it is shown that latency and computational complexity can be reduced in some VLSI applications where digital representations of analog signals exists using oversampled $\Delta\sum$ converters.
Paper Name	Analysis of a sigma delta modulator with a multi-level quantizer and single-bit feedback.	A low power continuous time band pass sigma delta modulator using linearity enhanced OTA	Stable Delta-Sigma Modulator with Signal Dependent Forward Path Gain for Industrial Applications
Authors	1.S.J. Park , Dept. of Electr. Eng., Stanford Univ., CA, USA 2.R.M. Gray , Dept. of Electr. Eng., Stanford Univ., CA, USA 3.W. Chou , Electron. Res. Lab., Salisbury, SA, Australia	1.Sohel, M.A. ; 2.Keshava Reddy, K.C. ; 3. Naaz, M. ; 4. Naseeb, M.A.	1. K. Diwakar, 2. K. Aanandha Saravanan, 3. C. Senthilpari

Abstract	Quantization error of the single-loop single-stage sigma-delta modulator with a multilevel quantizer and single-bit feedback has been analysed.	In this paper a low power continuous-time bandpass fourth order sigma delta modulator over 5 MHz band has been implemented which is operating at a Sampling Frequency of 280MHz. Source degeneration technique is used to linearized the operational transconductance amplifier (OTA) . It is observed that Signal to Quantization Noise Ratio (SQNR) with a non-linear OTA is of 46.6dB and it is 55.07dB with a Source degenerated OTA showing a marked increase of 1.5 bits(9 dB) in resolution of modulator. Further, optimum transistor sizing leads to a very low power consumption of 10.9mW and a figure of merit of 2.445pJ/bit.	In this paper stable Delta-Sigma Modulator with Signal Dependent Forward Path Gain has been discussed. The existing second order, single stage, single bit, unity feedback gain , discrete DSM cannot be used for the normalized full range (-1 to +1) of an input signal since the DSM becomes unstable when the input signal is above ±0.55. The stability is also not guaranteed for input signals of amplitude less than ±0.55. In the present paper, the above mentioned second order DSM is modified with input signal dependent forward path gain. The proposed DSM is suitable for industrial applications where one needs the digital representation of the analog input signal, during each sampling period. The proposed DSM can operate almost for the full range of input signals (-0.95 to +0.95) without causing instability, assuming that the second integrator output should not exceed the circuit supply voltage, ±15 Volts.

CONCLUSION

Sigma-delta ADCs and DACs have proliferated into many modern applications including measurement, voice band, audio, etc. The technique takes full advantage of low cost CMOS processes and therefore makes integration with highly digital functions such as practical applications in DSP. Modern techniques such as the multi-bit data scrambled architecture minimize problems with idle tones which plagued early Σ-Δ products. Resolutions up to 24-bits are currently available and the requirements on analog anti-aliasing /anti-imaging filters are greatly relaxed due to oversampling. The internal digital filter in audio Σ-Δ ADCs can be designed for linear phase, which is a major requirement in those applications. High resolution Σ-Δ ADCs designed for measurement applications, the digital filter is generally designed so that zeros occur at the mains frequencies of 50 Hz and 60 Hz.

Many Σ-Δ converters offer a high level of user programmability with respect to output data rate, digital filter characteristics, and self-calibration modes. Multichannel Σ-Δ ADCs are now available for data acquisition systems, and most users are well-educated with respect to the settling time requirements of the internal digital filter in these applications.[1]

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