International Journal of Engineering Research and General Science Volume 3, Issue 5, September-October, 2015
ISSN 2091-2730

FPGA BASED DIGITAL BEAM FORMING FOR PHASED ARRAY RADAR

YOGESH P SAJJAN[1], KRISHNA R[2], SHAHUL H[3]
[1]Research Scholar (MTech), Department of ECE, Bangalore Institute of Technology, Bengaluru, India
[2]Assistant Professor, Department of ECE, Bangalore Institute of Technology, Bengaluru, India
[3]Sci/Eng.-SD, RDA, ISTRAC, ISRO, Bengaluru, India
Email: *yogeshpsajjan@gmail.com*

Abstract— with the widespread use of digital techniques in modern communication systems, Digital Beam Forming (DBF) technique can be used for radar transmitter Beam Steering. Beam forming is a signal processing technique used for directional signal transmission or reception in antenna arrays and is achieved by controlling the phase and amplitude of each antenna element. The functions of a Timing Signal Generator (TSG) of a radar system is been implemented using VHDL programming and targeting it on to a FPGA. TSG works directly under the control of Radar Controller (RC) implemented using MATLAB and interfaced through Ethernet. Multiple DDS chips is used to generate multichannel radar waveforms and FPGA is used to send data and control signals to these DDS chips via SPI to achieve DBF. DDS (Direct Digital Synthesis) is a digitally controlled method of generating signals whose frequency, phase and amplitude are controlled by the respective description words.

A sixteen channel direct-digital waveform synthesizer has been developed to enable Digital Beam Steering of the transmitting side for a 4x4 array Patch Antenna. Each antenna element has separate beam forming exciter. The RC communicates to the TSG unit implemented in FPGA and sends commands to TSG. Through the RC GUI, the control parameters like frequency and phase shift values are sent to the TSG. Based on the control signals, data has to be sent to internal registers of each DDS. Xilinx FPGA is used to program sixteen AD9957 DDS and output of FPGA and DDS devices are analyzed.

Keywords — Radar Controller, FPGA, dsPIC Microcontroller, Direct Digital Synthesizer, Digital Beam Forming, Frequency Tuning Word, Phase Offset Word.

1. INTRODUCTION

Phased arrays have been used widely in both civilian and military applications. In civilian applications, they can be found in areas such as air traffic control, smart antennas and satellite communications. As for the military applications, phased arrays have been used in areas such as radar, communications, electronic warfare (EW) and missile guidance. Currently, phased array systems play an important role in defining the type of radar and communications system that will be installed on the next generation military platforms.

An approach in the design of a phased array antenna is to use digital beam forming. Digital beam forming consists of the spatial filtering of a signal where the phase shifting, amplitude scaling, and adding are implemented digitally. The idea is to use a computational and programmable environment which processes a signal in the digital domain to control the progressive phase shift between each antenna element in the array. Digital beam forming has many of the advantages a digital computational environment has over its analog counterpart. In most cases, less power is needed to perform the beam steering of the phased array antenna. Another advantage is the reduction of variations associated with time, temperature, and other environmental changes found in analog devices. The phased array antenna will still contain analog components such as Low Noise Amplifiers (LNAs) and Power Amplifiers (PA) found in the RF stages, but the number of analog components in general can be greatly reduced for large antenna arrays. Digital beam formers can accomplish minimization of side-lobe levels, interference canceling and multiple beam operation without changing the physical architecture of the phased array antenna. Every mode of operation of the digital beam former is created and controlled by means of code written on a programmable device of the digital beam former.

The advances in digital circuit technology made possible and feasible the idea of implementing the beam forming networks through digital signal processing. Digital Beam forming (DBF) offers advantages in terms of power consumption, flexibility, and accuracy. In general, digital systems tend to consume less power. Phased array antenna designs based on DBF implementation are currently being devised for radar applications.

1.1 RADAR WAVEFORM GENERATOR

Generally for any equipment, it is important to readily produce and control accurate waveforms of different frequencies. Some of the examples include agile frequency sources with low spurious signal content and less phase noise for communications, which will be used for industrial and biomedical applications. For those applications, we should be capable of generating an adjustable waveform cost effectively and conveniently which is a key design consideration. Several approaches are available for generating the signal but among those Direct Digital Synthesis (DDS) is most flexible one because DDS is a digital method to generate arbitrary waveforms with control of Frequency, Phase and Amplitude. [3]

2. PROPOSED SYSTEM ARCHITECTURE

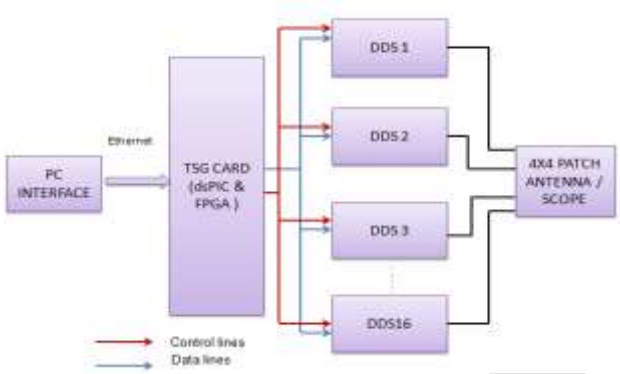

Figure 1.1 Proposed System Block Diagram

PC INTERFACE:- A Graphical User Interface, for inputs from the user. Calculations are done based on input and data frame to be forwarded to TSG is generated and sent via Ethernet.

TSG CARD:- mainly has a Xilinx FPGA, Microcontroller and buffers. The data is accepted by dsPIC and sent to FPGA for data processing. The data and control signal is sent to DDS from FPGA.

DDS BOARD:- DBF is accomplished in DDS board. 16 DDS are used to produce sine waves to 16 channel inputs with needed Phase, Frequency and amplitude, fed to 4x4 patch antenna.

2.1 SYSTEM SPECIFICATIONS

	PARAMETERS	SPECIFICATIONS
1	Output frequency	30MHz – 50MHz
2	Frequency tuning resolution	0.5Hz
3	Output waveform shape	Sine wave
4	No of channels	16
5	Input Clock	10MHz
6	Phase Tuning	0 to 360 degree, 0.05 degree steps

3. DDS TECHNOLOGY

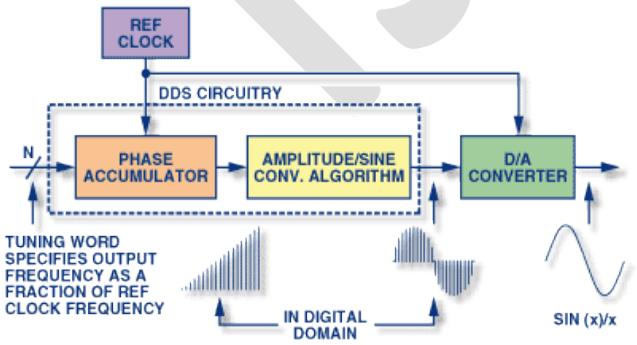

Figure 3.1: DDS Architecture

Direct digital synthesis (DDS) is a method of generating an analog waveform such as sine wave by using time varying signal in digital form. Then using digital to analog converter we can generate an analog signal. It has an ability to control and generate a signal with accurate signal parameters with low cost and low power consumption. DDS principle of operation can be easily understood by the Fig.3.1. Phase accumulator will take the Frequency Tuning Word (FTW) as input and converts into angular phase and then it is converted into the sine wave amplitudes by Amplitude/Sine Conversion Algorithm and then it is converted to analog sine wave output by D/A converter. The output frequency mainly depends on the reference-clock frequency

and tuning word. Phase accumulator is used to compute the phase (angle) address for the sine look up table, which gives the digital value of amplitude corresponding to that phase angle. The DAC will convert that digital value into corresponding analog current or voltage. To generate sine wave of fixed frequency a constant value is added to phase accumulator. If tuning word is large, the phase accumulator will step through the look up table quickly. If it is small the phase accumulator will take more steps thus generating a slower waveform.

4. IMPLEMENTATION

Figure 4.1 GUI for PC Interface

A GUI is developed in MATLAB to provide inputs. Code to calculate the Frequency Tuning Word (FTW) and Phase Offset Word (POW) is written using the required formulae. A XML is created with required parameters and their values. The data from the XML is taken to create a data frame which is sent to TSG Block via Ethernet.

The dsPIC is programmed, to receive the data frame via Ethernet from the PC INTERFACE. The Data frame is processed and sent to FPGA using SPI. Programming FPGA is done in Xilinx ISE, using VHDL code to receive data from microcontroller, store the data in a memory array. DDS Registers' initialization values are also stored in other memory arrays. According to configuration signal, FPGA will send the corresponding control signals and data to all 16 channel DDS.

In the DDS Board, for the implementation of 16 channels Phased Array Radar, 16 DDS are used. Synchronization of 16 DDS is achieved by considering one DDS chip to be Master and its SYNC_OUT signal is distributed to all the 16 DDS chips at SYNC_IN input, thus they will operate synchronously to the single internal clock.

The DDS chips are operated in the Single Tone Mode and sine wave is selected as the output waveform of the DDS.

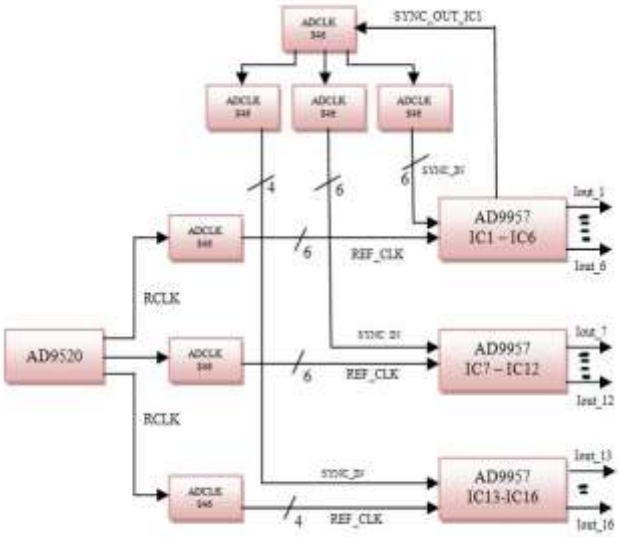

Figure 4.2 DDS Board Block Diagram

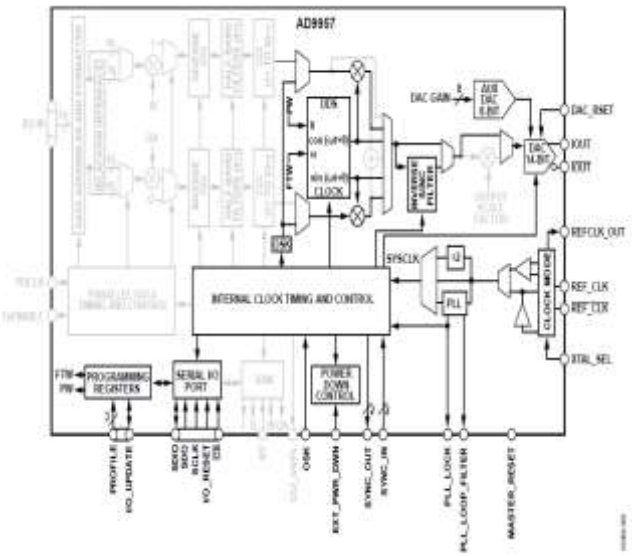

Figure 4.3 Single Tone Mode of AD9957 (From Analog Devices)

FPGA sends control signals to these DDS chips via SPI. FPGA is connected to PC through SPI. The DDS chips have some common control lines, and some that are individual per channel. Sysclk and sclk signal are provided from FPGA and are

distributed to all DDS chips using AD9520 and ADCLK846. An external clock of 10 MHz is provided from an external source which is fed to the AD 9520 clock divider.

5. EXPERIMENTAL RESULTS

The Device Utilization Summary obtained in Xilinx ISE after the synthesis of the VHDL code is given below,

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	1,295	9,312	13%
Number of 4 input LUTs	945	9,312	10%
Number of occupied Slices	1,084	4,656	23%
Number of Slices containing only related logic	1,084	1,084	100%
Number of Slices containing unrelated logic	0	1,084	0%
Total Number of 4 input LUTs	1,016	9,312	10%
Number used as logic	945		
Number used as a route-thru	71		
Number of bonded IOBs	37	232	15%
Number of RAMB16s	2	20	10%
Number of BUFGMUXs	3	24	12%
Number of DCMs	1	4	25%

Figure 5.1Device Utilization Summary

The On-chip power is analyzed using Xilinx XPower Analyzer, and the values obtained are shown below,

Table 13 On-chip Power Values

On-Chip	Clocks	Signals	DCMs	IO	Leakage	Total
Power(W)	0.037	0.014	0.019	0.127	0.085	0.283

The FPGA outputs are connected to a digital Oscilloscope and the CRO screen shots are shown below,

The signal channels are:- Channel 3 – 100 MHz System Clock, Channel 1 – IO_Update, Channel 2 – IO_Reset, Channel 0 – 12.5 MHz sclk for Data transfer, Channel 4 – Master_Reset, Channel 5 – Profile, Channel 6 to 14 – DDS1 to DDS9

When the Master_Reset and IO_Reset are low, Data Transmission starts and the data is forwarded with the rising edge of sclk. The IO_Update signal becomes high when the transmission is complete and then the sclk is halted.

Figure 5.2 Outputs generated for Initialization of DDS Registers

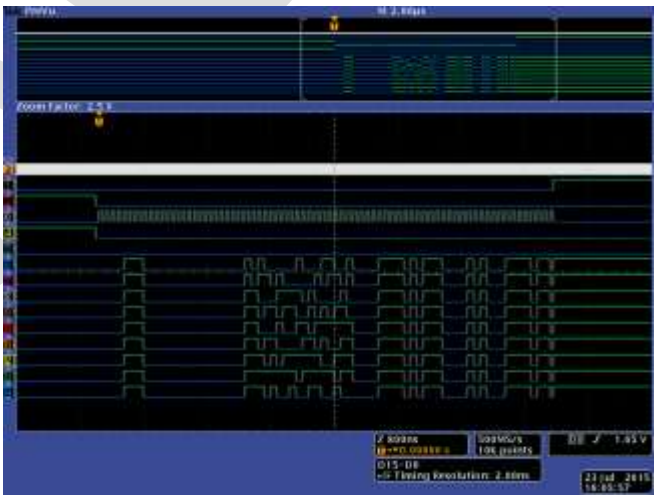

Figure 5.3 Outputs generated for Configuration of DDS Profile Register

DDS Board Simulation Outputs obtained in Simulink is shown below,

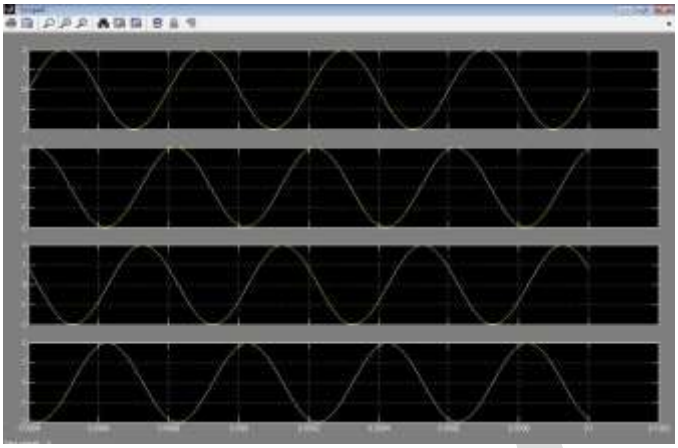

Figure 5.4 Phase Shifted Sine Waveforms of different DDS w.r.t 1st DDS Sine Wave as Reference

ACKNOWLEDGMENT

I'm indebted to Supreme Almighty for his beloved blessings on me with his grace. I would like to thank Mr. K V Prasad, Mr. VijayaPrakash from BIT, Mr. Pradeep Kumar, Mr. Arjun S, Mr. Chinni P and Mr. Shivakumara Swamy from ISTRAC for their Valuable Guidance and support for the work. I would mention my sincere and heartfelt gratitude to my Parents and all my Family members for their wholehearted constant support. I would also thank all the persons who have directly and indirectly supported me in this work.

CONCLUSION

In this work, we propose a method to achieve Digital Beam Forming in Transmitter section of 16 channel Phased Array Radar using Direct Digital Synthesizer chips to generate a multi channel VHF radar frequencies. Timing Signal Generator and Configuration Card was designed and developed as an intermediate device between PC and DDS board, which based on control signals, performs the data handling and forwards the required data to DDS, for the operation of MPAR. With the idea of implementing an advanced technology, design of DDS based RF waveform generator is demonstrated using the XILINX FPGA and dsPIC33F Micro Controller that results in a more stable and durable RF signal generator. The 16 channel DDS board is been simulated. The design has fine tunable resolution, sub-degree phase tuning capability, extremely fast hopping speed, fast settling & switching time and low spurious noise. Thus the DDS based DBF developed has enormous potential to be used for Multifunctional Phased Array Radar(MPAR), launch vehicles traffic controller, climate monitoring and in providing wind velocity data for aircrafts.

REFERENCES:

[1] Anudeepa S. Kholapure, Dr. Arvind Agarwal, ― Design of a Timing Signal generator for RADAR using FPGA ‖, Institute of Communications and Navigation, VOL. 19, NO. 2, 2009

[2] B.Suresh, M.V.Srikanth, ― Radar waveform generator based on DDS, International journal for advanced research in computer and communication engineering, September 2013

[3] Lathasree.G, Pradeep Kumar, - DDS technique based RF-excited card, International Journal combined research and development, October 2013

[4] Sanjay M Trivedi1, B. S. Raman, - FPGA based control signal generator for pulsed radar, Proc. IEEE, vol. 95, no. 7, pp. 1430-1469, September 2012.

[5] P Srinivasulu, P. Kamaraj, ― Control system for VHF phased array radar, Tech. Rep. GDD-05-04, NSF, 2005

[6] Henrik Ohlsson, Lars Wanhammar, ― Implementation of a digital beam former in an FPGA using distributed arithmetic, SE 581 83,

2010.

[7] Dr.A.Jhansi rani,Dr.A.Jaya Lakshmi, - Phased Array Antenna & Beam forming Subsystems in Phased Array Radar

[8] Okorogu V.N, Nwalozie G.C, Okoli K.C, Okoye E.D, - Design and Simulation of a Low Cost Digital Beamforming (DBF) Receiver for Wireless Communication

[9] Dr.Jeffrey S.Herd, ― Multifunction phased array radar panel, ACM/ Springer Wireless Networks, vol. 18, no. 2, pp. 215-226, February 2011.

[10] H. Aliakbarian, V. Volski , ― Analogue versus digital for baseband beam steerable array used for LEO satellite application, Stellanbosch University, February 2011.

[11] Wenfeng Dong; Quan Liu; Shirui Peng; Haihong Li "Design and realization of arbitrary radar waveform generator based on DDS technology", Radar Handbook Edition 3, Publication Year: 2010,

[12] Chao Huang, Li-xiang Ren, Er-ke Mao, "A Systematic Frequency Planning Method in Direct Digital Synthesizer Design",

International Conference on Wireless Communication, 2009