International Journal of Engineering Research and General Science Volume 3, Issue 4, Part-2, July-August, 2015
ISSN 2091-2730

Double Boost SEPIC AC-DC Converter

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Abstract- In this paper, a new single phase dual output ac-dc bridgeless double boost SEPIC (IDBS) converter is proposed which is a high step up converter. The absence of bridge rectifier in the proposed rectifier and the conduction of one semiconductor switch in the current flowing path during each switching cycle result in less conduction losses and improves efficiency. The proposed topology is designed to operate to achieve nearly a unity power factor and low total harmonic distortion (THD) of the input current. The DCM operation gives advantages such as zero-current turn-on in the power switches and simple control circuitry. The proposed topology gives better performance than modified bridgeless SEPIC rectifier in terms of efficiency, total harmonic distortion (THD), and power factor.. A design example for a 500-W/600 V dc with 120 V input voltage is provided. The proposed circuit is simulated in Matlab 2010a which ensures the feasibility of the converter

Key Words: AC - DC power converter, PFC Correction, High step-up converter, SEPIC Converter, Switched Capacitor, DCM, Double boost converter

1. INTRODUCTION

The demand for clean energy is increasing day by day and thus power supplies with active power factor correction (PFC) techniques are becoming necessary for many types of electronic equipment. They are designed to meet harmonic regulations and standards, such as the IEC 61000-3-2 [1]. Full bridge power supplies with active power factor correction (PFC) techniques cannot provide a high voltage gain and also they suffers from the fact that three semiconductor switches conducts at any instant of time.

In response to these concerns, considerable research efforts have been directed toward the development of efficient bridgeless PFC circuit topologies. A bridgeless PFC circuit allows the current to flow through a minimum number of switching devices compared to the conventional PFC circuit. The bridgeless boost rectifier has the drawbacks that the input–output isolation cannot easily be implemented, the startup inrush current is high, and there is a lack of current limiting during overload conditions. The boost converter operating in discontinuous current mode (DCM) can offer a number of advantages such as inherent PFC function, simple control, soft turn-on of the main switch, and reduced diode reversed-recovery losses. However, the DCM operation requires a boost inductor since it must switch extremely high peak ripple currents and voltages. As a result, a more robust input filter must be employed to suppress the high-frequency components of the pulsating input current, which increases the overall weight and cost of the rectifier.

A SEPIC converter is a less popular topology for PFC converter design because the control can be complex, due to its 2 pairs of un-damped complex poles, compared with other FC converters, such as the boost converter, fly-back converter. The advantage of the SEPIC converter is that its output voltage is not necessarily limited by its input voltage range. This property means that the output voltage can be higher or lower than input voltage. SEPIC converter offers easy implementation of magnetic coupling which results in reduction of input current ripple and low inrush current [3]. But Sepic converters suffer from higher switch voltage stresses. This increases the cost and conduction losses of the converter]. Converters uses switched-capacitor and voltage multiplier cell technique

which results in increase in the voltage gain as well as reduce the voltage stress across the power switch [10-12]. The use of switched capacitors can significantly extend the voltage gain, minimize the input current ripple and doubles the transferable power.

In this paper, a bridgeless dual output double boost AC - DC converter utilizing switched capacitor technology without extreme duty-cycle operation is introduced. This is achieved by integrating a Double boost Sepic DC - DC converter with a PFC correction circuit. We can have two outputs from the converter, actual output and the capacitor of the modified circuit provides another output. The Double Boost converter is selected due to its high step-up capability and the Sepic converter is selected due to its capability of providing low input current ripple. Hence, the Double Boost Sepic ac -dc converter allows the duty cycle to be extended further and makes the proposed converter more suitable for high step-up voltage applications. In addition, the proposed converter maintains the key advantages of the conventional boost and Sepic converters.

2. DOUBLE BOOST SEPIC AC-DC PFC CONVERTER

The basic circuit diagram of a bridgeless SEPIC double boost PFC Rectifier with voltage multiplier is illustrated in the figure 1. The bridgeless configuration will reduce the conduction losses since the diode bridge is removed, as a result the overall efficiency will increase. The voltage multiplier will result in high gain. The proposed circuit consists of two SEPIC circuits with switched capacitor configuration that consists of diodes and capacitors connected in a symmetrical configuration. Each configuration will operate in a half-line cycle. Moreover, the symmetrical operation of the converter simplifies the control signals for switches Q_1 and Q_2 which drives the circuitry.

The proposed topology shown in Figure 1 has a practical drawbacks of lack of limiting large inrush current flowing through inductors and switches. Therefore, special measures are taken to limit inrush current in the circuit and it should be necessary to ensure soft start of the system and to protect the circuit components from damage.

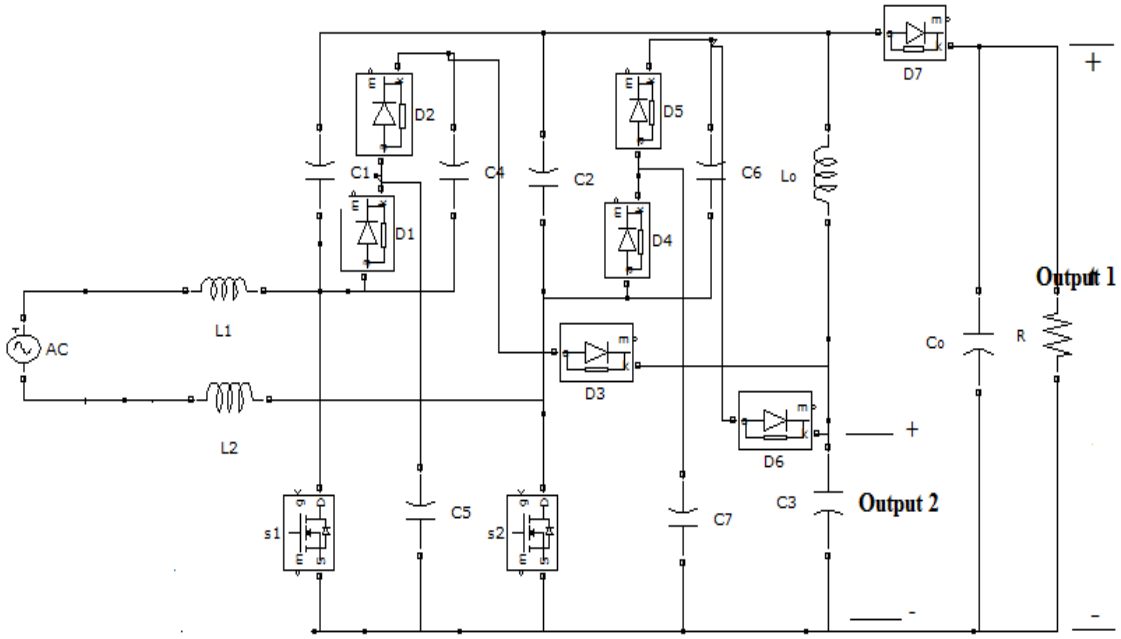
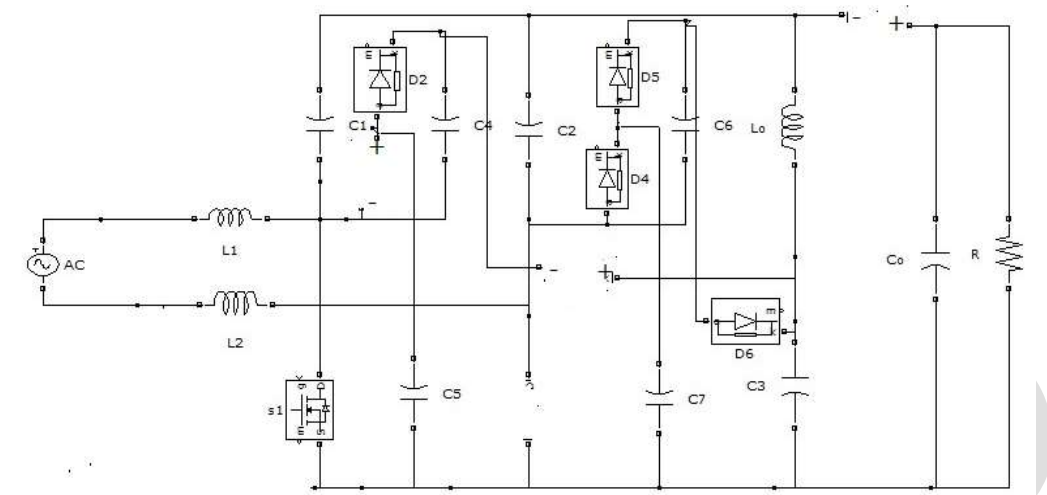


Fig. 1: Circuit diagram of the double boost SEPIC AC – DC PFC converter

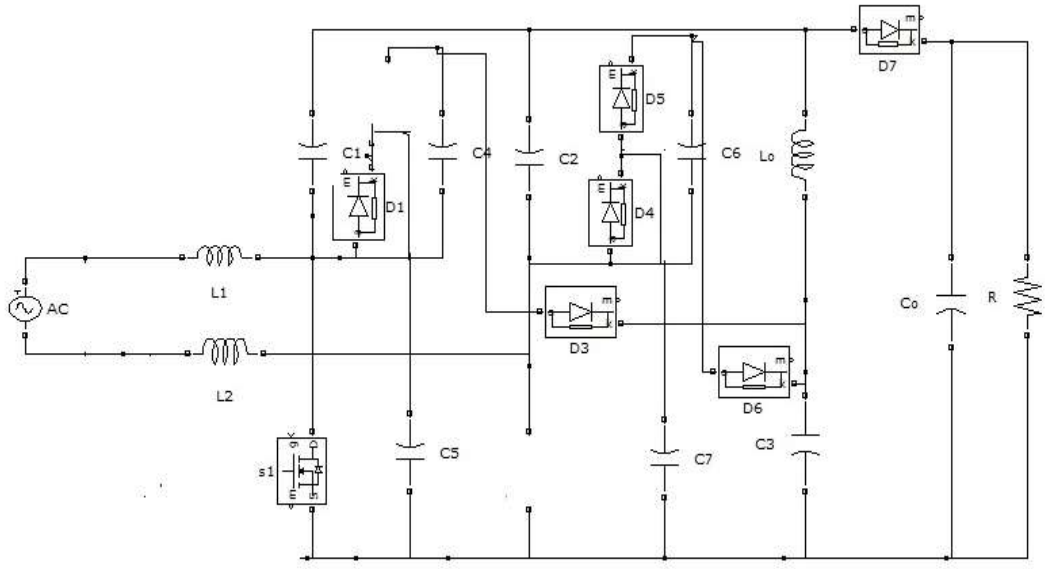
2.1 Principle of Operation and Analysis

The proposed circuit consists of two symmetrical configurations as illustrated in figure 2. The circuit is analysed for the positive half line cycle and negative half line cycle. Accordingly, the circuit operation in one T_s can be divided into two stages as shown in

Figure 2(a) and (b). The circuit operation during one switching period T_s in a positive half-line period can be divided into two distinct operating modes, as shown in Figure 4 and figure 5, and it can be described as follows. Figure 3 shows its ideal key waveforms. The operational modes are described briefly as follows.



(a)



(b)

Fig 2: Topological stages of the converter of fig 1. (a)Switch ON topology, (b) Switch OFF topology

Mode 1

During the positive half cycle, the power switch Q_1 operates. When it is turned on, inductor L_1 stores energy and simultaneously diode D_2 is turned on. Diode D_1 is reversed-biased by the capacitor voltage V_{C1}, while diodes D_3 and D_7 are turned off by the negative voltage (V_{C1} - V_{C3}) and (V_{C4} - V_O) across them, respectively. In this stage, the currents through the two inductors increases linearly at a rate proportional to the input voltage V_{in}. Capacitor C_4 charges capacitor C_5 while capacitor C_1 is being charged by inductor L_o(i_{Lo}). This mode lasts till the voltage across capacitor C_4 and C_5 are equal, while the difference between the capacitors' voltages V_{C1} and V_{C3} must equal to the input voltage, i.e.,

$$V_{C4} = V_{C5} \quad \text{----------(1)}$$

$$V_{in} = V_{C1} - V_{C3} \text{----------(2)}$$

At the end of this interval, the switch is turned-off initiating the next subinterval.

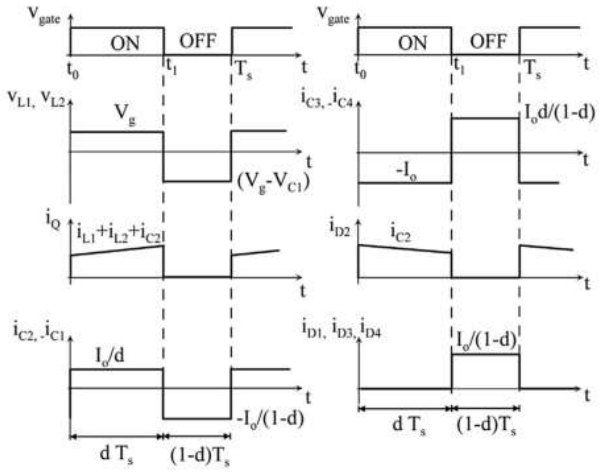


Fig 3: Theoretical Waveforms

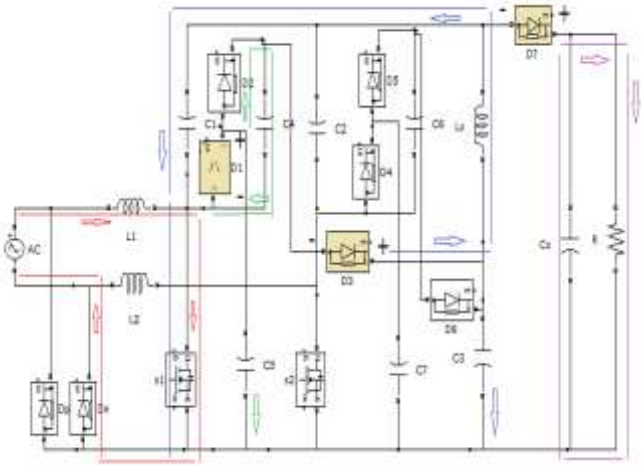


Fig. 4: Current flow path of the double boost SEPIC AC – DC PFC converter during Mode 1

Mode 2

When the switch Q_1 is turned off, Diodes D_1, D_3, D_7 are turned on simultaneously providing a path for the input and output inductor currents. Diode D_2 is reverse biased by the voltage V_{C4}. In this stage, the inductors currents i_{L1} and i_{Lo} decreases linearly at a rate proportional to the voltage (V_{in} - V_{C5}) and (V_{C3}-V_o), respectively. Capacitors C_1 and C_3 are being charged by the currents (i_{L1} + i_{C4} + i_{C1}) and (i_{D3} - i_{L2}), respectively. During this stage, the output Capacitor C_o and the load R_L are being charged by the current (i_{L0} + i_{C1}). Referring to Figure 5, the following relations must hold:

$$V_O = V_{C3} + V_{C1} - V_{C4} \text{ ----------(3)}$$

$$V_{C3} = 2V_{C5} \text{ ----------(4)}$$

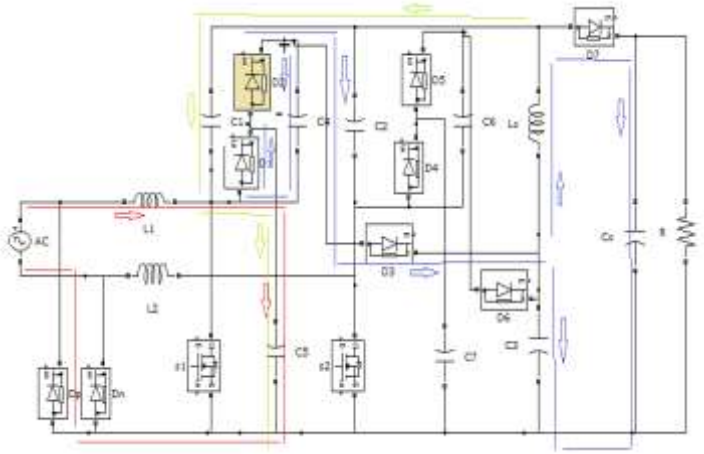


Fig. 5: Current flow path of the double boost SEPIC AC – DC PFC converter during Mode 2

The design considerations are

- Input voltage = 120V
- Output voltage = 600V
- Switching frequency = 50kHz
- Maximum input current ripple, Δi_L = 3 % of input current
- Output voltage ripple, ΔV_C = 5 % of V_o

During Mode 1

$$V_{L1} = V_{L2} = V_i \text{ ----------(5)}$$
$$L\, di/dt = V_i \text{ ----------(6)}$$

Assuming max. input current ripple be 3% of input current. Solving we get,

$$\Delta i_{L1} = V_i\, D/ L_1\, f \text{ ----------(7)}$$

$$\Delta i_{L2} = V_i\, D/ L_2\, f \text{ ----------(8)}$$

Solving we get $L_1 = L_2$ =10mH

Capacitor Design

During mode 1, the relationship between the V_i , V_{C1} and V_{C4} are

$$V_i + V_{C4} = V_{C1} \text{ ----------(2)}$$

$$V_i = V_{C5} \text{ ----------(2)}$$

During mode 2, applying KVL rule, the relationship between the capacitor voltage V_{C2} and V_{C3} can be written as follows:

$$V_{C3} = V_{C1} \text{ ----------(9)}$$

$$V_{Lo} + V_{C3} = V_o \text{ ----------(10)}$$

The voltage of the capacitors can be derived as follows:

$$\Delta Q = i_{L3} DT \text{ ----------(11)}$$

$$\Delta V_C = i_{L3} DT/C \text{ ----------(12)}$$

Assuming 5% ripples in output voltage and $i_{L3} = i_o$

Solving we get

$$C_1 – C_7 = 22 \mu F, L_1, L_2 = 10mH$$

3. SIMULATION DIAGRAM & RESULTS

The proposed circuit “Double Boost SEPIC AC – DC PFC converter" has been modelled and simulated in Matlab/ Simulink 2010a. The components values obtained from the design equations for an input voltage of 120V are used.

Table -1: Simulation Parameters

Parameters	Value
Input voltage	120 V
Output Voltage	700V, 600V
Inductors L_1, L_2, L_3	10mH, 180uH
Capacitors $C_1 – C_7$	50µH
Output Capacitor,C_o	1000µH
Switching frequency	50kHz
Grid frequency	50Hz
Duty cycle	37%

The input voltage is set to 120V and both switches operates with a frequency of 50 kHz and duty cycle 37% . Simulation waveforms coincide with the theoretical operating waveforms.

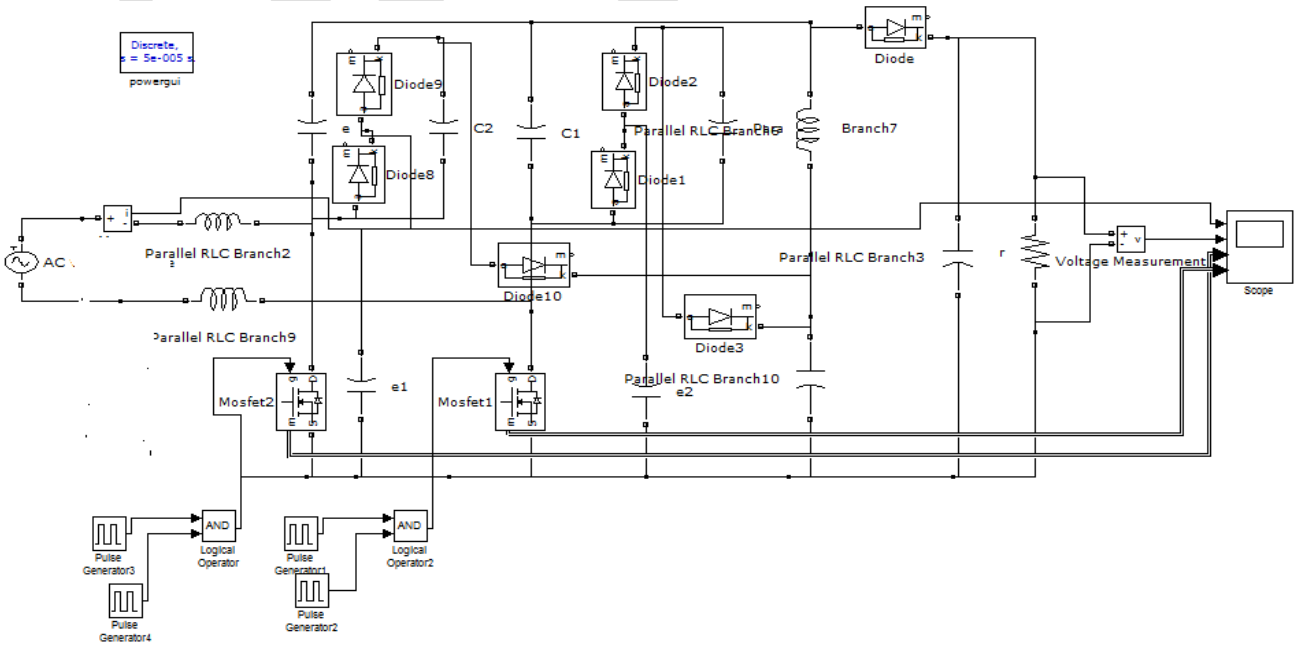
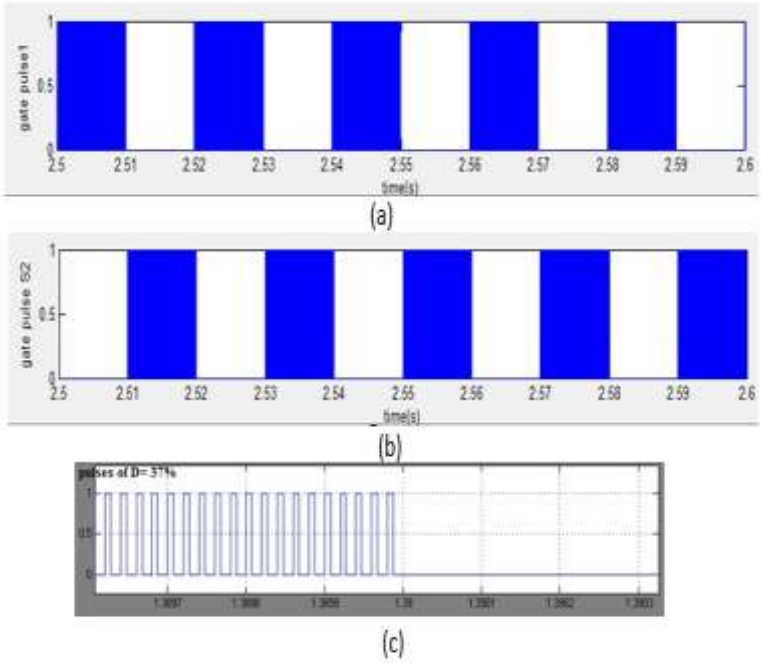


Fig 6: Simulink Diagram of bridgeless PFC Double boost SEPIC Rectifier



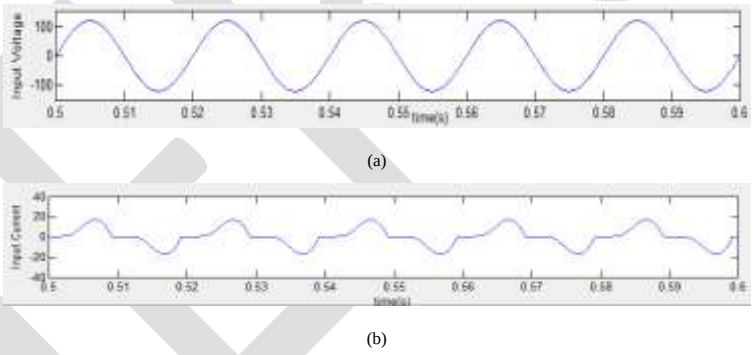
(a)

(b)

(c)

Fig 7: Simulated waveforms of (a)gate pulses for Q1 (b) gate pulses for Q2
(c) magnified portion of pulses with Duty cycle = 37%

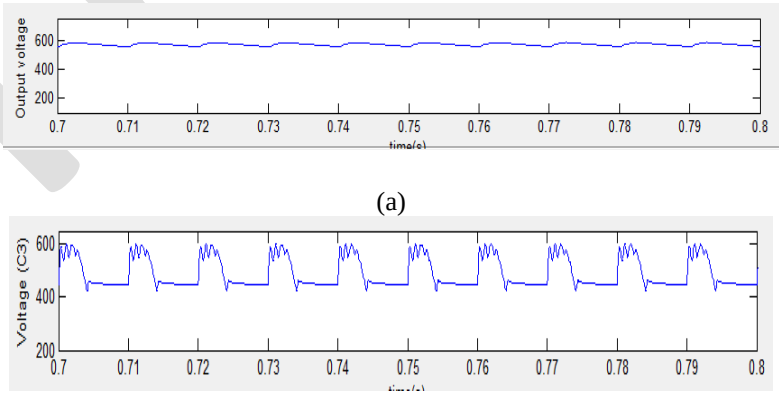
The simulated waveforms of input voltage and current and output voltage and current are shown in the fig 8 and 9 respectively.



(a)

(b)

Fig 8: Simulated waveforms (a)Input voltage (b) Input current



(a)

(b)

Fig 9: Simulated waveforms (a) Output voltage 1 (b) Output voltage 2

The current through inductors L_1 and L_2 rises and falls with respect to the switching pulses are shown in figure 7.

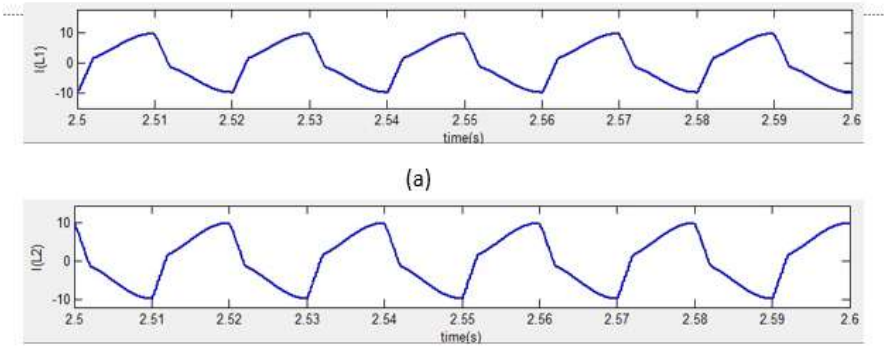
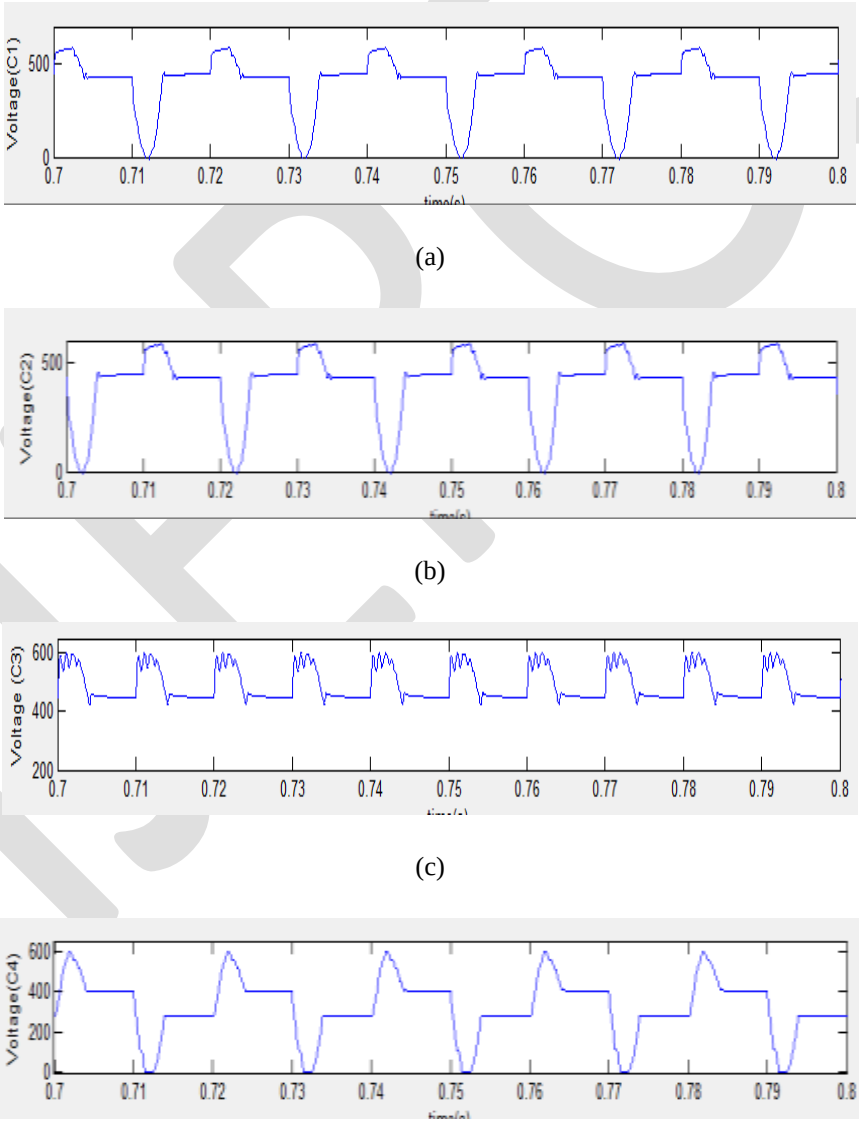
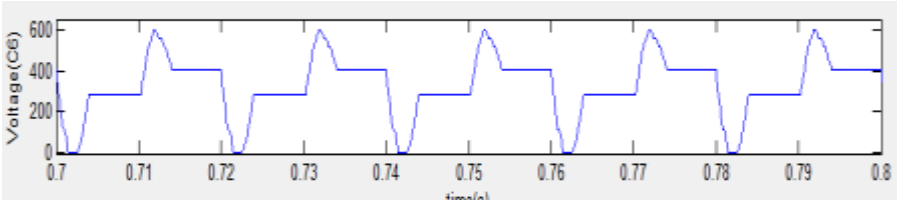
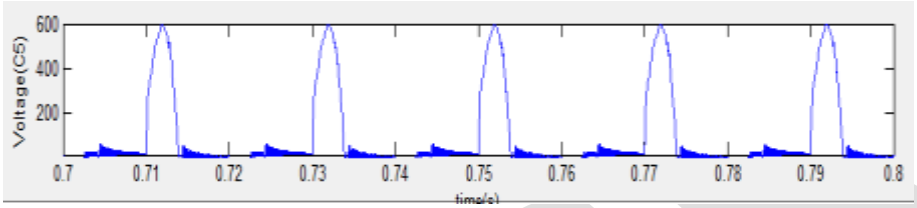


Fig 14: Simulated waveforms of (a) Inductor current L_1 (b) Inductor current L_2





(e)



(f)

(g)

Fig 14: Simulated waveforms of Voltages across (a) C_1 (b) C_2 (c) C_3 (d) C_4 (e) C_6 (f) C_5(g) C_7 (h)

4. CONCLUSIONS

A new topology based on double boost SEPIC has been presented and simulated in Matlab/Simulink 2010a which ensures the performance of the converter. The proposed topology has a higher efficiency than the full bridge topology due to its bridgeless nature**.** The proposed converter is operated at high switching frequencies to reduce input current ripple. Hence, the overall advantages will be higher efficiency, reduced size and weight, simpler structure and control. The two power switches in the proposed topology can be driven by the same control signal, which significantly simplifies the control circuitry. The THD of the converter is reduced to 10% and a 0.95 power factor is obtained by the proposed converter. The proposed integration technique can be easily extended together power converters to meet the demand for a wide range of voltages.

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