International Journal of Engineering Research and General Science Volume 3, Issue 4, Part-2, July-August, 2015
ISSN 2091-2730

Design of Low Voltage Low Dropout Regulator

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Abstract-

A low voltage low dropout regulator provides an output voltage near about 0.8V by giving input voltage of 1V, with 45nm CMOS technology. The LDO consist of Operational Transconductance Amplifier which works as error amplifier with current splitting technique to boost gain. The power MOS Mp is used for low voltage and low dropout voltage. The output variation is 12mV for current of 0-100mA.The proposed LDO operates over wide range of frequency and provides power supply rejection more than 60 dB at 100 KHz. The simulation of proposed LDO in Advance design system tool.

Keywords: low dropout regulator, fast transient response, high power supply rejection, small area etc.

INTRODUCTION

Low dropout regulators (LDOs) are widely used in power management integrated circuits and systems [1] [2]. Because it provides stable DC voltage whose input and output voltage difference is low. The dropout voltage means the input/output differential voltage where control loop starts regulating [3]. The regulator provides stable DC voltage and acceptable level particularly for product that are operated by portable battery like cameras, hand phones, and laptop. Now a day's study and research on power management technique for different application has been increases [4]. Power management improves the power efficiency of devices resulting in prolong battery life cycle and operating time for the device.

Voltage Regulator can be classified as Low Dropout (LDO) linear Regulator, switching regulator and switch capacitor regulator and each regulator has its own characteristics and application. The low dropout regulators have some good characteristics indeed, but they also have some problems in their implementations such as PSR and transient response etc.[5]. Regulating performances, quiescent current, operating voltages are the important characteristics to be considered during designing LDO. The other specifications are drop-out voltage, load regulation, line regulation, output voltage variation, output capacitor and ESR range and input/output voltage range. so to improve performance of low dropout regulator, a new technique is presented to design a high performance LDO with fast load transient response, high power supply rejection ratio, small quiescent current, good load Regulation and precise over current protection. Bandwidth is also another important specification in voltage regulator design. The higher the bandwidth of a regulator, the more rapidly it can react to changes in input and power supply and stay the output voltage constant. High bandwidth improves the power supply rejection ratio (PSRR) of the regulator, which is a measure of how well the regulator attenuates noise on the power supply. The better the power supply rejection, the less the output voltage changes in response to fluctuations in the supply.

From the precise review of related work and published literature, it is observed that many researchers has designed low dropout regulator using different technique. Some researchers focused on improving transient response [2] [6] [7] or some focused on enhancing power supply rejection ratio [8] [9] or both of the regulators. In [2] [7] they proposed regulators any a large driving current or else additional circuits which consume significant $I_{Q.}$ In [10] they proposed low dropout regulator design in 90nm which provides 0.85V output voltage by applying 1V input voltage and provides high PSRR and fast transient response.

DESIGN CONSIDERATIONS

Many factors must be considered when designing a Low dropout regulator. Reducing power consumption is for all time advantageous, specially with portable consumer electronics. Less power consumption allows the device's battery to last longer, means the user needs to charge the battery less often. Efficiency is determined by the dropout voltage. Dropout voltage means the difference among the unregulated supply voltage and regulated output voltage. Lowering the dropout voltage can lower the necessary voltage of the unregulated power supply, which lowers the power consumption of the regulator. A less power-hungry device uses a smaller battery and better portability.

Portability of regulator improves by decreasing area. the devices which consist of more than one voltage regulators has many benefits from a voltage regulator design which requires smaller area, because in house circuitry can be made smaller and easier to bring around. Because of small area more devices are fixed into one wafer, which reduces cost of manufacturing.

Bandwidth is one of the important specification of LDO design. If the bandwidth of regulator is high, it reacts more quickly to change in input voltage and power supply and keeps output voltage constant. Power supply rejection ratio (PSRR) of the regulator can be improves by keeping higher bandwidth, which attenuates noise on the power supply. The enhanced the power supply rejection,

the less the output voltage changes in response to fluctuations in the supply. The PSRR can be categorized by the magnitude of attenuation as well as the range of frequencies over which the attenuation occurs. Typically PSRR is greatest at low frequencies.

Another factor to consider in LDO regulator design is stability. The Low dropout regulator provides a constant voltage to other components, a regulator prone to oscillation is not advantageous. Stability of regulator varies with output current and load capacitance i.e. load condition, which can be partly specified or unknown, a regulator design that has good phase margin for a wide range of output loads is best. Associated with stability is load regulation, the percentage change in output voltage in response to a change in the output current.

CIRCUIT REALIZATION AND SIMULATION RESULTS

The proposed LDO regulator optimizes the four parameters i. e. low-voltage operation while achieving a fast transient response, low *IQ* and high PSR and small area. The schematic of proposed LDO shown in fig1.The Operational Transconductance Amplifier (OTA) which works as Error Amplifier (EA). EA is composed of M_{EA1}-M_{EA9}. OTA type error amplifier does not requires compensation capacitor and it operates at minimum voltage $V_{DD,\,min}=V_{th}+2V_{ov}$ ($\leq$1 V). EA contains low input offset voltage to achieve an accurate output. The Impedance at node v_X and v_Y is set low to sustain the system stability by push the non dominant pole p_X to high frequency. Full swing is achieved at node v_G using M_{EA7}, M_{EA9}. The use of M_{EA7} and M_{EA9} reduces the size of MP power transistor. Hence it reduces the circuit area and gate capacitance. MP drives on sufficient slew rate using EA output. The Gain of the EA is given as:

$$A_{EAO} = g_{m2} \times A \times (r_{O7} \| r_{O9})$$

$$\approx g_{m2} \times A \times r_{O9}$$

$$= (2I_{d2}/V_{OV2)\times} A \times 1/ (\lambda 9 \times A \times Id2)$$

$$= 2/ (V_{OV2} \times \lambda 9) \quad \ldots\ldots (1)$$

Where I_{d2}=Bias Current,V_{OV2}=Overdrive voltage of M_{EA2} A=current ration b/w first and second stage of EA. The gain of EA in eq 1 is low for fast transient response therefore there has been used the current splitting technique to increase the gain. The gain is increased using sufficient g_{m2} and increasing r_{O9}. The Power MOS Mp is used because of its low voltage and low dropout voltage requirements. The Increased gain using g_{m2} and r_{O9} increased the PSR. The replica of power noise created on gate terminal is used to cancel out the power noise at source terminal of Power MOS. There is applied two equivalent transistor M_{EA4} and M_{EA5} b/w $I_{\_EATA}$ and Ground to attenuate power supply noise at node v_X and v_Y. First stage of the EA also contains M_{ta1}-M_{ta8}which reduces the Slew time of power MOS gate terminal by increasing the charging and discharging current during the load transient. M_P,M_{ta3} and M_{ta8} are biased in cutoff region to avoid high I_Q and breaking point of perfect replication at gate terminal of these transistors. V_{out} and V_{FB} feedback voltage changes because of large load change. This Feedback voltage variation is amplified. The v_{FB} variation is then amplified by the output variation detector of the transient accelerator, generating v_{X1} and v_{Y1} as follows:

$$\begin{cases} \frac{v_{Y1}}{v_{FB}} \approx -g_{m2} \times \left(\frac{1}{g_{m5}}\right) \times g_{m,ta2} \times \left(r_{O,ta1} \| r_{O,ta2}\right) \\ \frac{v_{X1}}{v_{FB}} \approx -g_{m2} \times \left(\frac{1}{g_{m4}}\right) \times g_{m,ta6} \times \frac{(W/L)_{M_{ta5}}}{(W/L)_{M_{ta4}}} \times \left(r_{O,ta5} \| r_{O,ta7}\right) \end{cases} \quad (2)$$

Where $g_{m,\,i|i}$=t_{a6},t_{a2}, $r_{O,\,i|i}$=t_{a1},t_{a2},t_{a5},t_{a7}, and $(W/L)_{Mi|i=ta5,ta4}$ represent the transconductance, output resistance, and aspect ratio of the corresponding transistors, respectively. v_{X1} and v_{Y1} turn on the Mt8 if the load current increases otherwise M_{ta3}. As V_{out} reaches its final value M_{ta3} and M_{ta8} turned off.

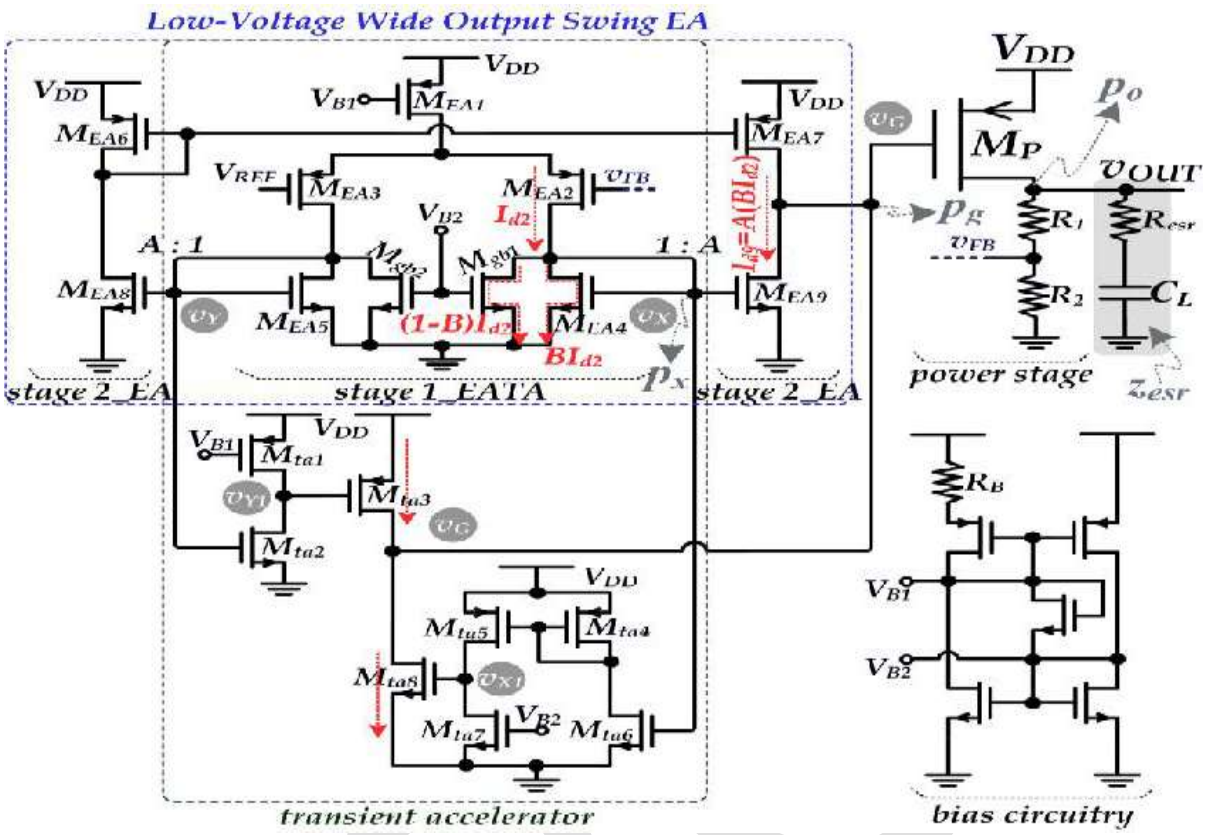


fig 1. Schematic of the proposed LDO regulator.

The proposed LDO is designed in 45 nm CMOS process. The LDO is able to operate at 1V, which covers a wide range of the battery voltage. The proposed LDO provides dropout voltage near about 200mV. It gives near about 0.8 V output voltage which is shown fig2.

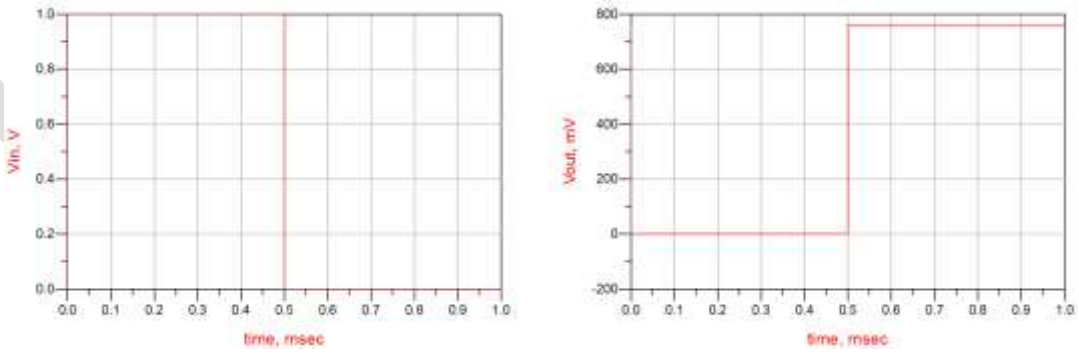
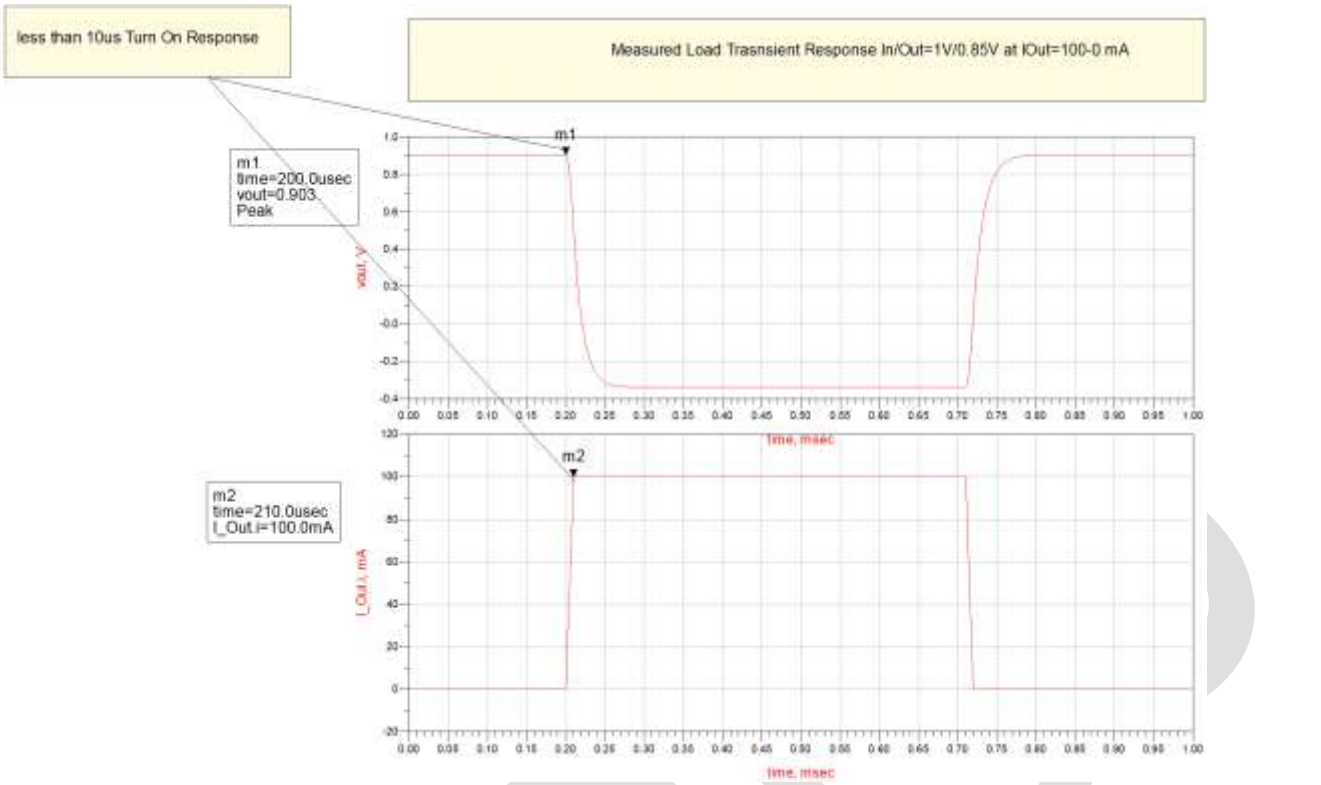
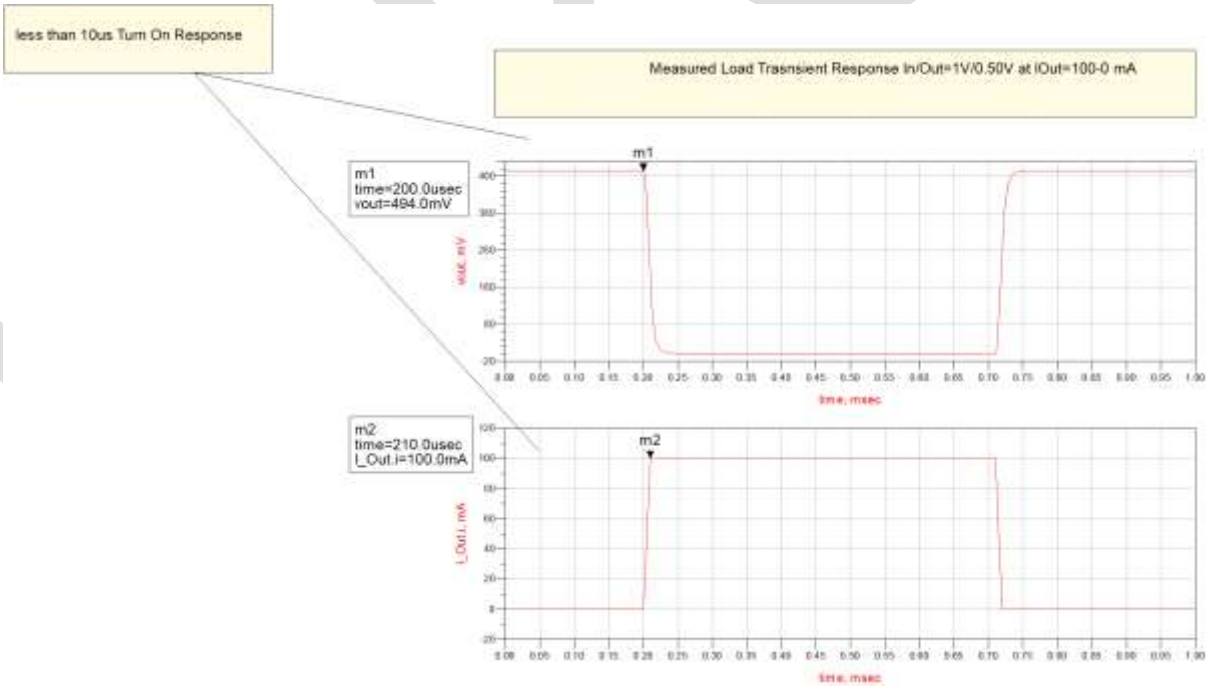


Fig2: Output Voltage waveform

The input voltage is 1 V and the values of *R*1 and *R*2 can be adjusted to generate any regulated output level between 0.85 and 0.5 V. The maximum *IQ* is 60 μA, achieving a 99.94% current efficiency. The *CL* used for measurement is 1 μF with a *R*esr of 1 Ω. Fig. 3 shows the measured waveforms of the load transient test where the load current is switched between 0 and 100 mA within 10 µs. The input/output voltage VDD and VOUT is set to {1 V, 0.85 V} and {1 V, 0.5 V}, respectively.



(a)



(b)

Fig 3. Load Transient Response (a) LDO Load Transient Response at 0.8V output

(b) LDO Load Transient Response at 0.5V output

The PSR performance is also measured when the test conditions are *V*DD = 1 V, *V*OUT = 0.85 V, and *I*OUT =100 mA and the measured result is shown in Fig. 4. The proposed LDO regulator achieves a PSR more than 60 dB at low frequencies whereas the roll off frequency is 100 kHz.

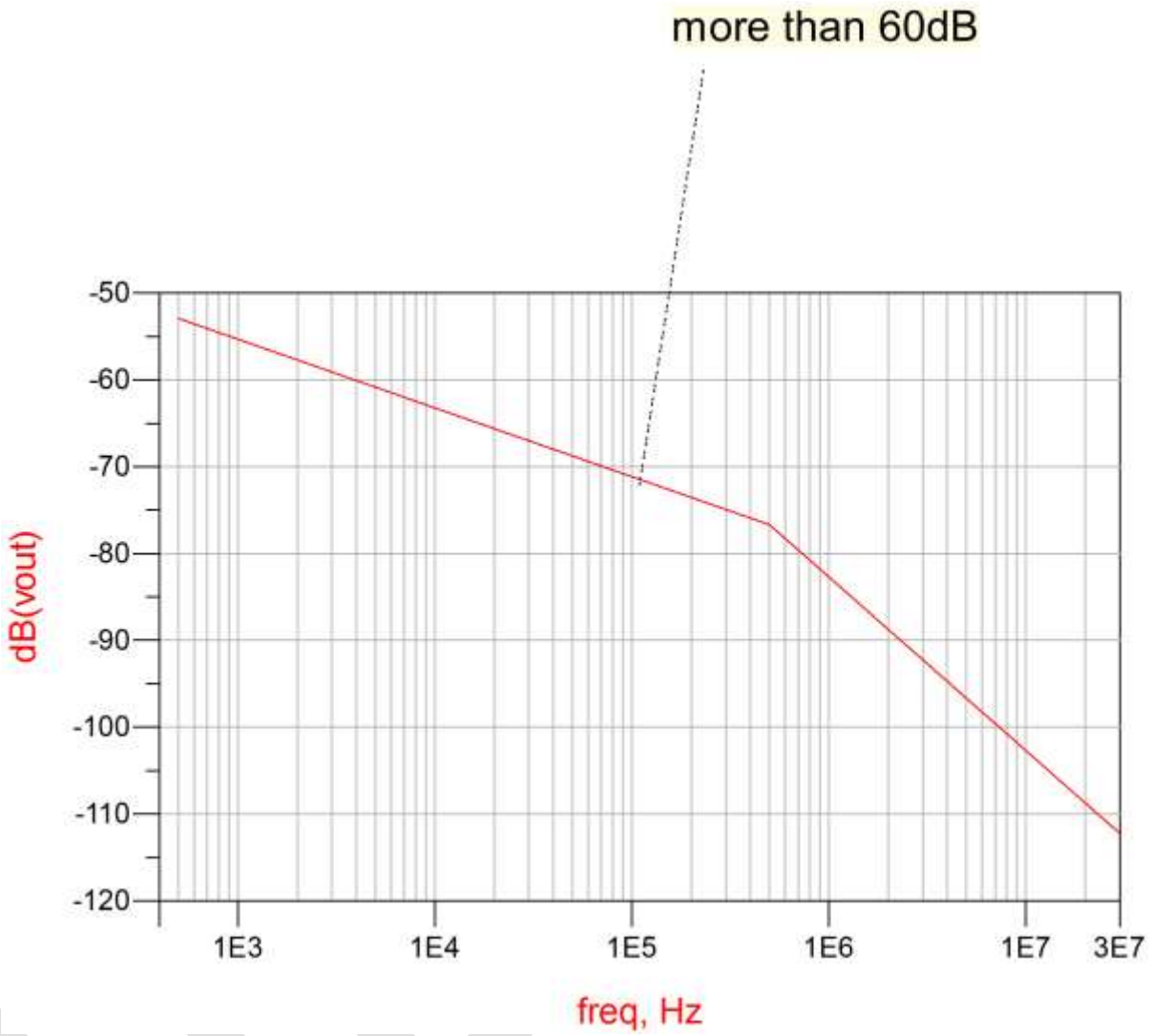


Fig 4 LDO Load PSR at Iout=100mA

CONCLUSION

In this paper presented an LDO regulator with a simple OTA-type EA plus an adaptive transient accelerator, which can achieve operation below 1 V, fast transient response, low *IQ*, and high PSR under a wide range of operating conditions. The proposed LDO regulator was designed using a 45 nm CMOS process to convert an input of 1 V to an output near about 0.8V, while achieving a PSR more than 60 dB with a 0–100-kHz frequency range. The output variation is 12mV for current of 0-100mA.The experimental results verified the feasibility of the proposed LDO regulator.

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