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Advanced High Speed Frequency to Voltage Converter for Industrial Controllers.

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Abstract— This paper presents utilization of on chip Pulse Width Modulation (PWM) for generating analog voltage. Industrial controllers or PLC requires digital to analog converters for process control. Many industrial devices like Variable Frequency Drive (VFD) work on standard analog input 0 to 10v. To communicate DAC modules and PLC special protocol are involved. It leads to time latency to get analog output. This paper represents without any protocol single digital output pin of PLC to give frequency to DAC module. This module converts those ranges of frequency signal to calibrated PWM to get analog output with low pass filter. With this module one can get analog voltage in standard range of 0 to 10v with ripple less than 0.1V. For This module can work in range of 1 kHz to 10 kHz.

Keywords— DAC, LOW PASS FILTER, PLC, PWM, PROTOCOL, VFD.

INTRODUCTION

IN Automated industry there are lots of process variable need to be controlled so as to get process under control. Simply saying there are lots of continuous signals need to monitor and control. Continuous actuators are major parts of the process. Today's continuous actuators are able to work on multiple standards like 4-20 mA,-10v to +10V DC, 0 to 10V DC. It is necessary to create interface between digital controllers and actuators. Industrial controller like PLC has capability to generate frequency signal. It's a need to create an interface can accept those frequency signals from PLC and generate 0 to 10V DC analog output. This analog output signal can then easily feed to industrial devices like VFD, PID controller etc.

In a typical PWM signal, the base frequency is fixed, but the pulse width is a variable or fixed. The pulse width is directly proportional to the amplitude of the original unmodulated signal. In other words, in a PWM signal, the frequency of the waveform is a constant while the duty cycle varies according to the amplitude of the original signal. A simple low pass filter is used to generate an output voltage directly proportional to the average time spent in the high level.

RESEARCH PROBLEM

Many industrial devices work on standard analog input 0 to 10v. To communicate DAC modules and PLC special protocol are involved. It leads to time latency to get analog output. DAC using R-2R ladder requires more power, more no of components, uses more no of bits to achieve good resolution. Potentiometric DACs have excellent linearity but they are much expensive and available with limited no of bits. All these methods involve reference power supply.

RELATED WORK

1.4V 13µW 83dB DR CT-ΣΔ modulator with Dual-Slope quantizer and PWM DAC for bipotential signal acquisition. This paper presents the implementation and measurements of a novel ultra-low power low voltage multi-bit continuous-time sigma-delta (CT-ΣΔ) modulator, whose quantizer and feedback DACs operate in the time domain [1]. A low power successive approximation A/D converter based on PWM technique, this paper introduces a new architecture for a simple, practical and high precision conversion and analysis with Fourier transform method [2]. An AC voltage standard based on a PWM based DAC. This paper describes a new AC voltage standard which uses a traceable DC voltage standard as an input and produces an AC output at an equivalent RMS voltage to 1 µV/V uncertainty [3].

PWM BASED DAC APPROACH

Industrial controller requires converting of digital to analog signal with minimum settling time, less bulky system, and accurate result without investing in much cost in new modules. Some advantages of PWM based DAC systems are

- Single pin requirement from the microcontroller GPIO pins.
- Extremely low external component requirement, without severe precision requirement.
- Output resistance that is independent of input.

$$[\text{ScaleCount}] = \left[\frac{\text{ScaleMaxValue}}{\text{Digital Input Max Count}}\right] \times \text{Digital Input}$$

As the scaling factor is a constant for a given DAC implementation, it can be precomputed and stored for use. e.g. In 8 bit PWM max count can be given is 255. In this case we need to read input frequency by means of timer, this is the digital count. For measuring of input frequency max up to 100 kHz. Timer need to select must have time base of 0.01 mS.

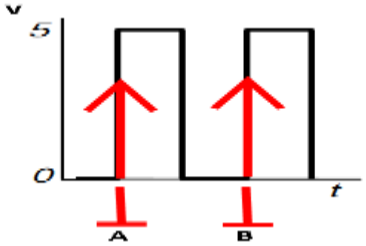


Figure 1: Input frequency signal.

Here to measure frequency of input signal; it is necessary to start timer at first rising edge A and stop timer at second rising edge B. Frequency of input signal is reciprocal of timing count difference between B and A multiplied by time base for timer. This digital input is must be calibrated for full scale 100% duty cycle. For example digital count of input frequency is 46015; max count possible with 16 bit variable register is 64536. If duty cycles register is 8 bit so for 100% duty cycle count should be 255. Therefore

$$[\text{ScaleCount}] = \left[\frac{255}{65536}\right] \times \text{Digital Input}$$

[Scale Count]=0.003890 × Digital Input.
0.003890 is precomputed constant based on calibration factors.
Scale Count is same to Duty Cycle count.
Duty Cycle = [0.003890] × 46015.
Duty Cycle= 179; it is 70% of total 100% duty ratio.

The PWM/DAC approach is not new, but performance limitations have historically confined its use to low-resolution, low-bandwidth applications. The performance of the method relates directly to the ability of the low pass filter to remove the high frequency components of the PWM signal. Use of filter with too low a cut-off frequency, and DAC bandwidth suffers. Use a filter with too high a cut-off frequency DAC resolution suffers but one way to improve both of these problems is to increase the frequency of the PWM.

dac resolution:

$$Ao = \left[\frac{Di}{2^N}\right] \times Ref$$

Where:
Ao = Analog output.
Di = Digital input as a duty cycle count.
N = Number of digital input bits (resolution)
Ref = Reference Value (full scale).

Band width of the desired signal should be $F_{BW} \leq [F_{PWM}]$. If F_{BW} is selected such that, $F_{BW} = F_{PWM}$ then the external low pass filter should be a brick wall type filter. Brick-wall type analog filter are very difficult and expensive to build. So, for practical purpose, the external low pass filter, that has much smaller cut-off bandwidth than PWM bandwidth, should be used as shown in figure below[6].

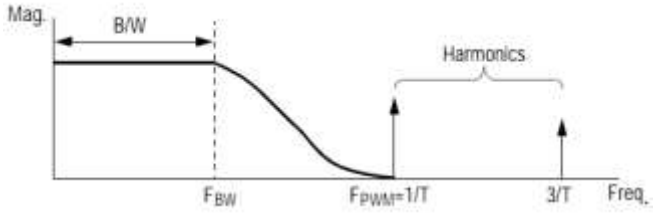


Figure 2: Bandwidth of Low Pass filter.

The 2nd order low-pass filter offers 40 dB/decade of stop band roll off, which is a two-fold improvement over the 1st order filter. The transfer function is given by the equation.

$$\frac{V_{out}(s)}{V_{In}(s)} = \frac{\omega_n^2}{s^2 + 2\varsigma\omega_n + \omega^2}$$

Where ωn is the undammed natural frequency in units of (rad/s) 2 and ζ is the non-dimensional damping ratio. It is straightforward to show that the filter bandwidth is BW [7].

$$BW = \omega_n\left[(1-2\varsigma^2) + \sqrt{4\varsigma^4 - 4\varsigma^2 + 2}\right]^{1/2}$$

MODELING AND SIMULATION

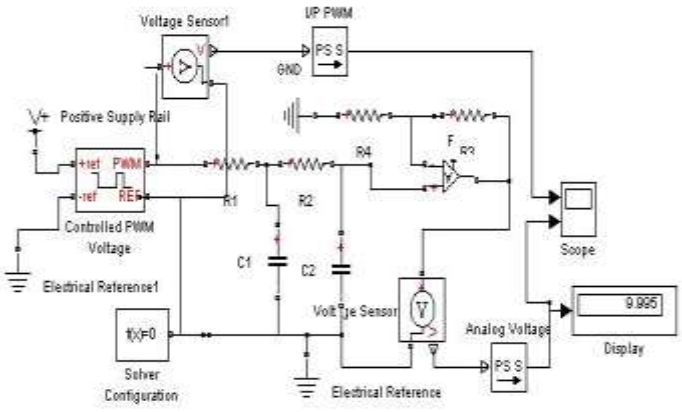
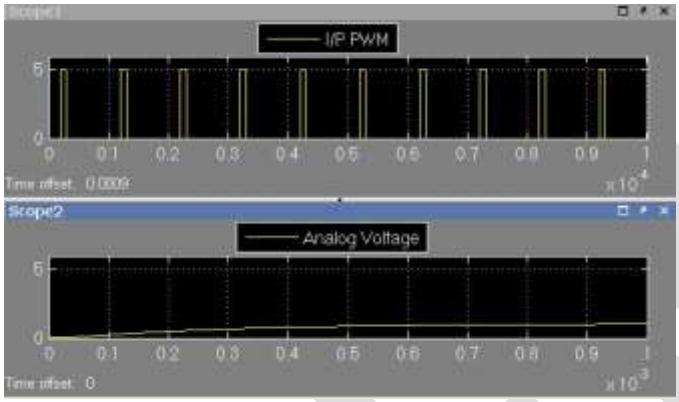


Figure 3: Simulation of DAC.

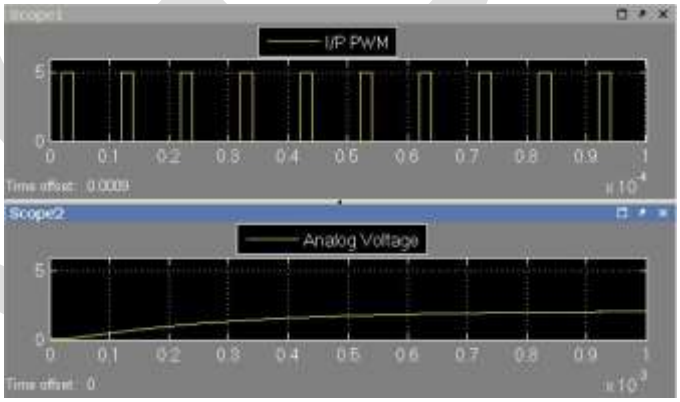
RESULTS:-

Sr. no	% Duty Cycle	Analog Voltage V
1	10	1.023
2	20	2.046
3	30	3.068
4	40	4.091
5	50	5.113
6	60	6.135
7	70	7.157
8	80	8.178
9	90	9.919
10	100	9.995

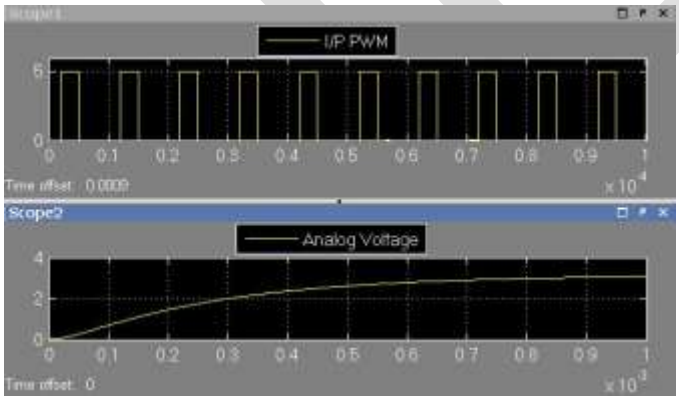
Wave forms for each % Duty Cycle



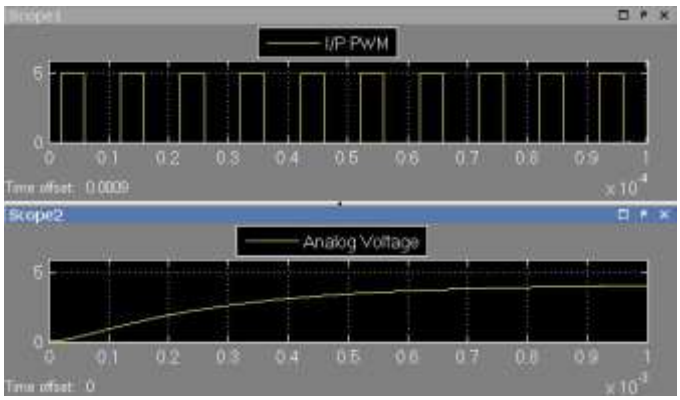
Duty Cycle =10 %, analog voltage 1.023 V.



Duty Cycle =20 %, analog voltage 2.046 V.



Duty Cycle =30 %, analog voltage 3.068 V.



Duty Cycle =40 %, analog voltage 4.091 V

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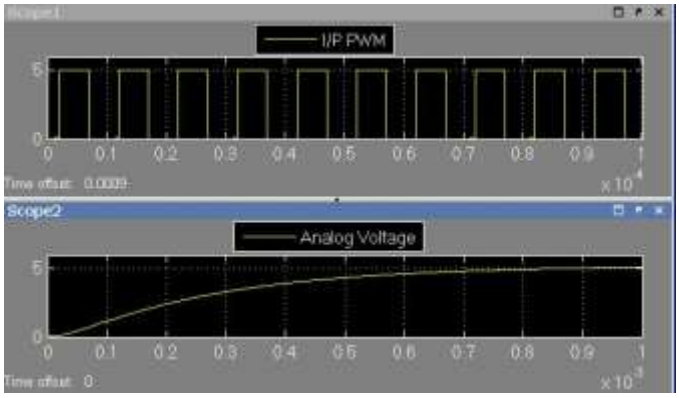
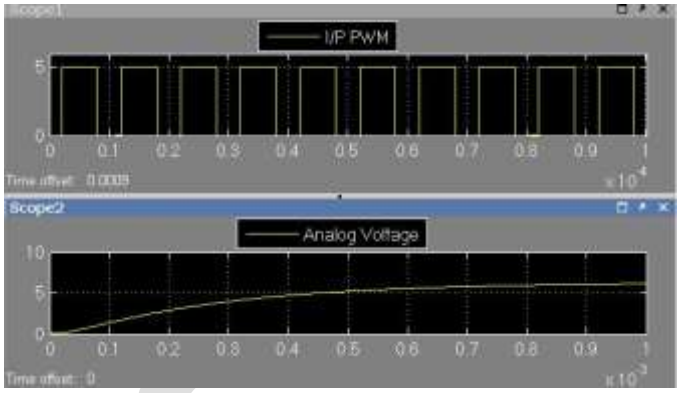
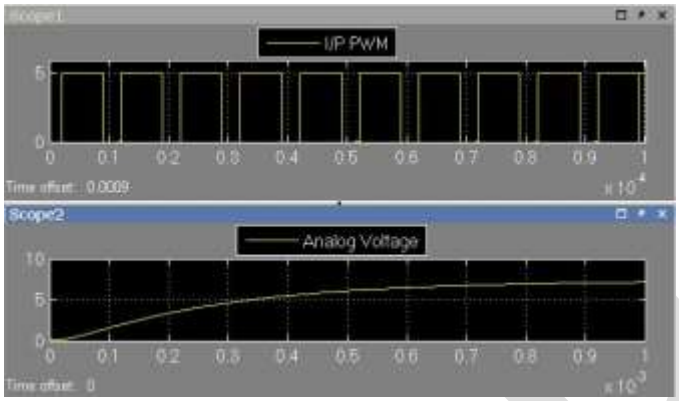


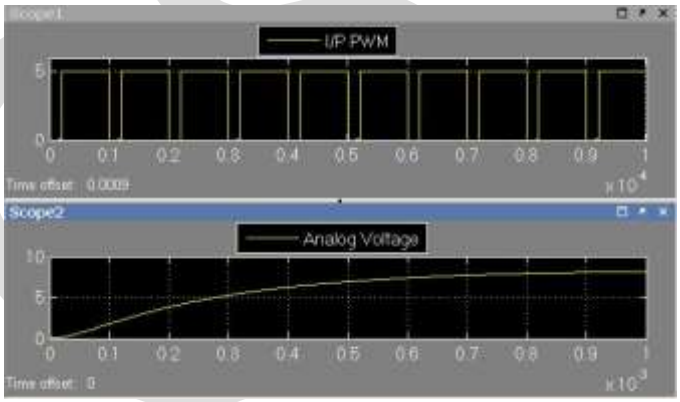
Duty Cycle =50 %, analog voltage 5.113 V.



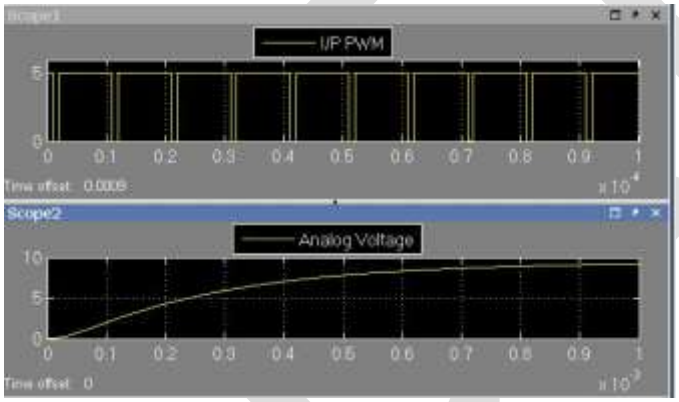
Duty Cycle =60 %, analog voltage 6.135 V.



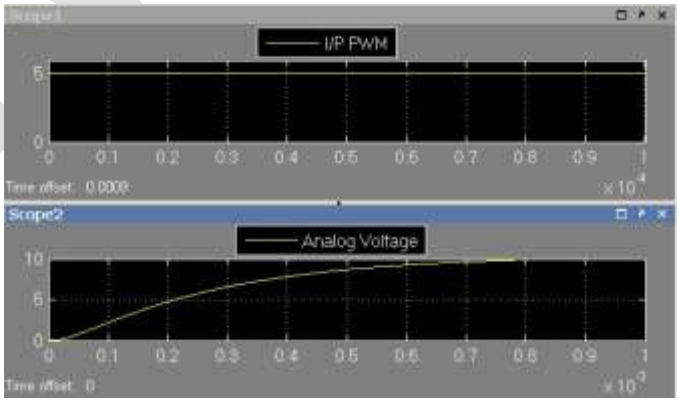
Duty Cycle =70 %, analog voltage 7.157 V.



Duty Cycle =80 %, analog voltage 8.178 V.



Duty Cycle =90 %, analog voltage 9.119 V.



Duty Cycle =100 %, analog voltage 9.995 V.

MATERIALS

The simulation model is developed under Matlab 7.0 With Dell XPS m1210 machine core 2 duo processor and 1 GB Ram on windows 7 platforms. Actual circuit is built with PIC18f4550 microcontroller having high speed PWM facility. Optoisolator PC817 is used for PLC and Module isolation. Ladder program written for Mitsubishi FX-2N PLC used with Gx Developer.

Figure 4: Ladder to generate frequency signal.

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