International Journal of Engineering Research and General Science Volume 3, Issue 4, July-August, 2015
ISSN 2091-2730

A High-Performance Single-Phase Bridgeless Interleaved PFC Converter with Over - Current Protection

Edwin Basil Lal[1], Bos Mathew Jos[2],Leena Thomas[3]
P.G Student[1], edwinbasil@gmail.com , 9746710546

Abstract- In AC to DC conversion boost converter is a key element. Conventional power factor corrected boost converter used for the purpose of AC to DC conversion have disadvantages like low power factor and high value of total harmonic distortion. These disadvantages can be eliminated in Bridgeless Interleaved power factor corrected boost converter. Self-commutating devices are used in these converters for the purpose of switching according to load rating. A protection circuit is provided which will isolate the converter from supply when current in load goes above the rated value of load current. When the load varies, the output voltage is maintained constant by providing the closed loop control. The Comparison Study between different topology can be find out to ensure BLIL topology's merits. The simulation of BLIL converter is done using MATLAB. The protection circuit of BLIL converter is simulated using MATLAB and The closed loop implementation of BLIL inoder to stabilize the output voltage with low ripples in the output.

Keywords-Uninterrupted Power Supplies(UPS),Battery energy storage systems(BESS), Bridgeless interleaved (BLIL),Adjustable Speed Drives(ASD), Power Factor Correction(PFC) ,Bridgeless Converters , Boost conveters

INTRODUCTION

AC-DC conversion of electric power is widely used in adjustable-speed drives (ASDs),switch-mode power supplies (SMPSs), uninterrupted power supplies (UPSs), and utility interface with nonconventional energy sources such as solar PV, battery energy storage systems (BESSs), in process technology such as electroplating, welding units, battery charging for electric vehicles, and power supplies for telecommunication systems, measurement and test equipment. There are different types of AC-DC converters such as conventional boost converter, bridgeless boost converter and interleaved boost converter are common AC-DC PFC topologies. These AC-DC converters involve a number of non-linear devices which reduce the system power factor and introduce harmonics in the power system leading to adverse effects. Hence it is essential to use a suitable power factor correction technique to condition the supply current. One such Active Power Factor corrected AC-DC Converter topology is Bridgeless Interleaved Boost Topology, which results in an improved supply power factor and reduced line current harmonics. Bridgeless Interleaved Boost Topology can also improve efficiency due to the elimination of the boost diode rectifier bridge. The conventional boost converter, bridgeless boost converter and interleaved boost converter are common AC- DC converters.

The conventional boost topology is the most popular topology for PFC applications. With this topology, the output capacitor ripple current is very high and as the power level increases, the diode bridge losses significantly degrade the efficiency. The bridgeless boost converter is good for a low to medium power range, up to approximately 1 kW [2]. It is an attractive solution for applications at power levels greater than 1 kW. This topology solves the problem of heat management in the input rectifier diode bridge, but it introduces increased EMI [7]. Another disadvantage of this topology is the floating input line with respect to the PFC stage ground, which makes it impossible to sense the input voltage without a low frequency transformer or an optical coupler. Also, in order to sense the input current, complex circuitry is needed to sense the current in the MOSFET and diode paths separately, since the current path does not share the same ground during each half-line cycle. The interleaved boost converter, consists of two boost converters in parallel so the input current is the sum of the two inductor currents in LB1 and LB2. Interleaving yields several advantages. The ripple currents in these inductors are out of phase, so they tend to cancel each other therefore reduce the high frequency input ripple current caused by the switching action, so the input EMI filter can be smaller. Additionally, the topology also inherently has the advantage of paralleling semiconductors to reduce conduction losses [7]. Finally, interleaving also reduces output capacitor high frequency ripple. One significant drawback of the interleaved boost PFC converter is that similar to the boost PFC converter, it retains the problem of heat management in the input diode bridge. In order to achieves high efficiency and low EMI bridgeless interleaved (BLIL) topology is used[1]. BLIL topology can achieve high efficiency at power levels above 3 kW due to the elimination of the boost diode Rectifier Bridge and low EMI due to interleaving [3].

In this paper, BLIL topology is simulated for different duty ratio to understand the comparison between PFC correction levels that happens in a circuit. This converter retains the same semiconductor device count as the interleaved boost PFC converter but the merits are on higher side than the conventional converters. BLIL topology is protected by using a control switch for permanent isolation and non-permanent isolation. This model significantly improves the reliability of the circuit even the extra switching causes losses but making it closed loop control the output voltage and reduction in ripple in the output voltage.

MODELING OF BLIL CONVERTER

Introduction

This converter retains the same semiconductor device count as the interleaved boost PFC converter. In comparison, it requires two additional MOSFETs and two fast diodes in place of four slow diodes used in the input bridge of the interleaved boost PFC converter. Circuit operation has been separated into the positive and negative half cycles.

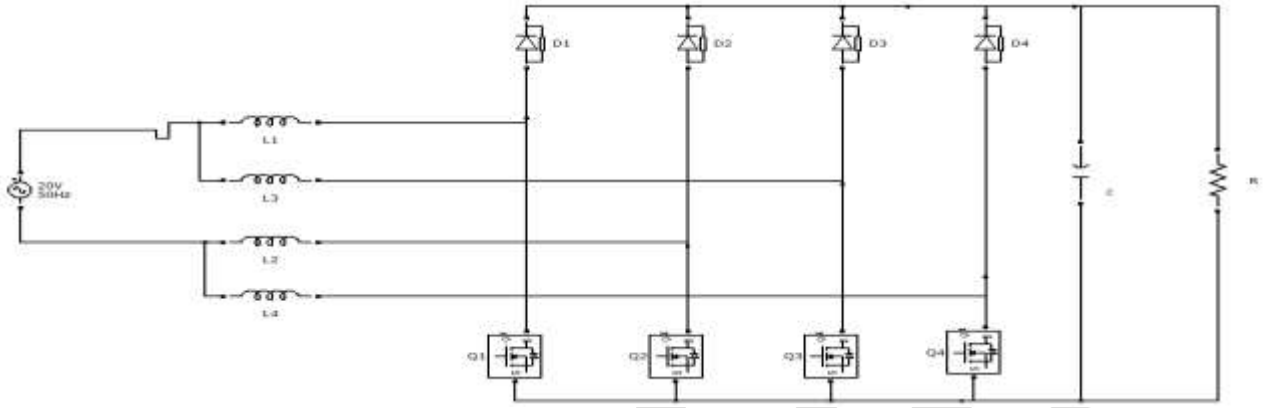

Figure 2.1: The BLIL Converter

During the positive half cycle, when the ac input voltage is positive, Q1/Q2 turn on and current flows through L1 and Q1 and continues through Q2 (and partially its body diode) and then L2, returning to the line while storing energy in L1 and L2. When Q1/Q2 turn off, energy stored in L1 and L2 is released as current flows through D1, through the load and returns through the body diode of Q2 back to the input mains. With interleaving, the same mode happens for Q3/Q4, but with a 180◦ phase delay. The operation for this mode is Q3/Q4 on, storing energy in L3/L4 through the path L3-Q3-Q4-L4 back to the input. When Q3/Q4 turn off, energy is released through D3 to the load and returning through the body diode of Q4 back to the input mains.

During the negative half cycle, when the ac input voltage is negative, Q1/Q2 turn on and current flows through L2 and Q2 and continues through Q1 (and partially its body diode) and then L1, returning to the line while storing energy in L2 and L1. When Q1/Q2 turn off, energy stored in L2 and L1 is released as current flows through D2, through the load and returns through the body diode of Q1 back to the input mains. With interleaving, the same mode happens for Q3/Q4, but with a 180◦ phase delay. The operation for this mode has Q3/Q4 on, storing energy in L3/L4 through the path L4-Q4-Q3-L3 back to the input.

The operation of converter during the negative input voltage half cycle is similar to the operation of converter during the positive input voltage half cycle. In addition, the detailed circuit operation depends on the duty cycle, therefore positive half cycle operation analysis for D >0.5 and D <0.5 is provided. When the BLIL is made protective also the operation of the converter remains the same and the closed loop modelling of BLIL shows the reduction in output ripple voltage.

B. Operational modes:

Interval 1[to-t1]: At t0, Q1/ Q2 are ON, and Q3/Q4 are off, as shown in Fig.2.2 During this interval, the current in series inductances L1 and L2 increases linearly and stores the energy in these inductors. The ripple currents in Q1 and Q2 are the same as the current in series inductances L1 and L2. The current in series inductances L3 and L4 decreases linearly and transfers the energy to the load through D3, Co and body diode of Q4. Assuming matched inductors, L1- L4, the input ripple current is the sum of currents in L1/L2 and L3/L4.

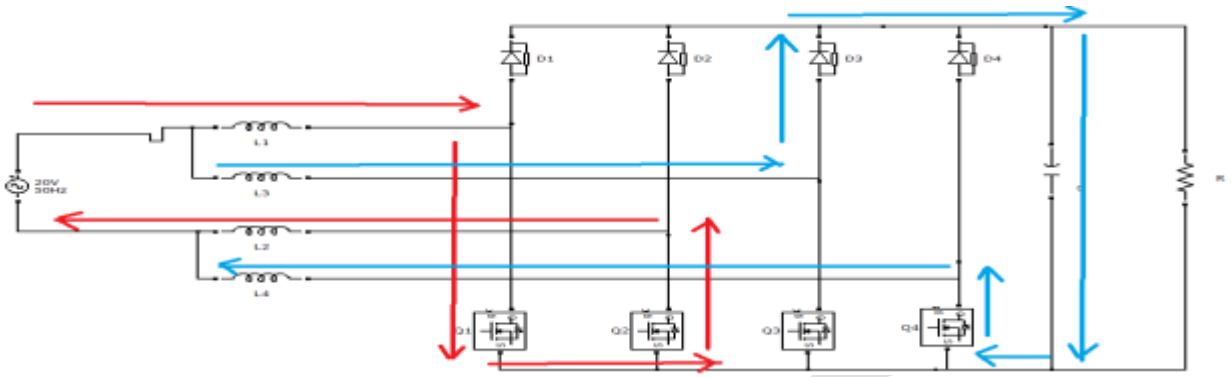

Figure 2.2: Mode 1 of BLIL

Interval 2[t1-t2]: At t1, Q3/Q4 are turned on, while Q1/Q2 remain on, as shown in Fig.2.3. During this interval the current in the four inductors each increase linearly, storing energy in these inductors. The ripple currents in Q1 and Q2 are the same as the ripple current in series inductances L1 and L2. Similarly, the ripple currents in Q3 and Q4 are the same as the ripple current in series inductances L3 and L4.

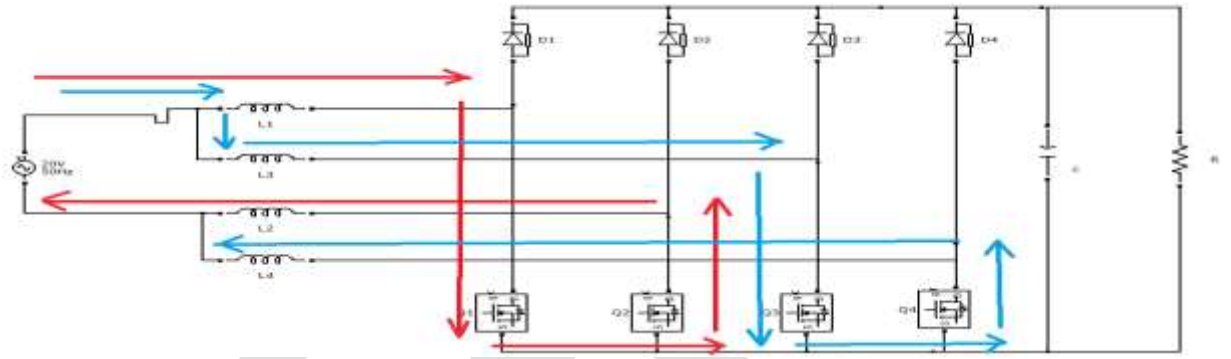

Figure 2.3: Mode 2 of BLIL

Interval 3[t2-t3]: At t2, Q1/Q2 are turned off, while Q3/Q4 remain on, as shown in Fig.2.4. During this interval, the current in series increases linearly and inductances L3 and L4 stores the energy in these inductors. The ripple currents in Q3 and Q4 are the same as the ripple current in series inductances L3 and L4. The current in L1 and L2 decreases linearly and transfers the energy to the load through D1, Co, and body diode of Q2.

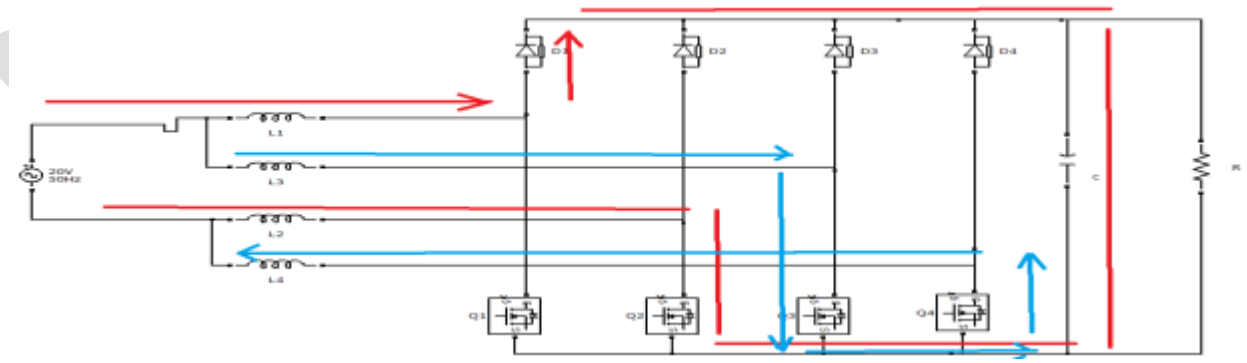

Figure 2.4: Mode 3 of BLIL

Interval 4[t3-t4]: At t3, Q3/Q4 remains on, while Q1/Q2 are turned on, as shown in Fig.2.5. During this interval, the currents in the four inductors each increase linearly, storing energy in these inductors. The ripple currents in Q1 and Q2 are the same as the ripple currents in L1 and L2. The current in series inductances L1 and L2 decreases linearly and transfers the energy to the load through D2, Co, and body diode of Q4.

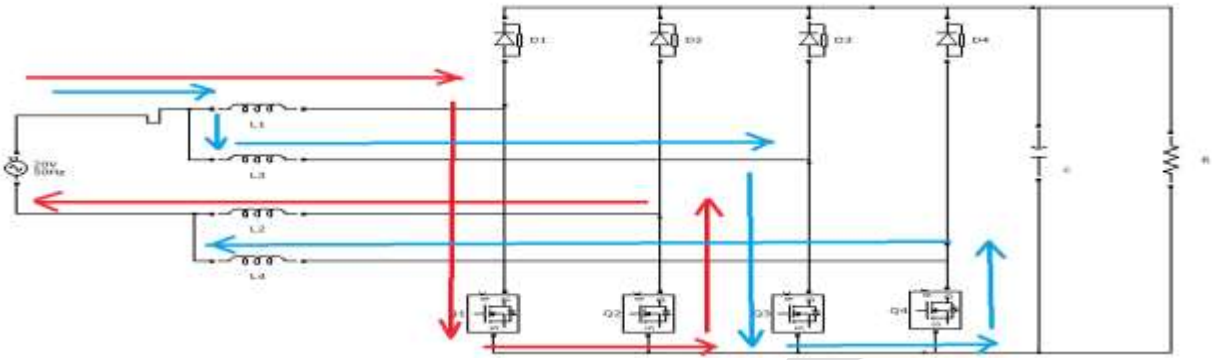

Figure 2.5: Mode 4 of BLIL

MODELING OF PROTECTIVE CIRCUIT BLIL CONVERTER

A. Introduction

An overcurrent is said to have occurred when a current flowing through the load is greater than the rated load current. This may damage to the diode, MOSFET and also the inductor. So a protection circuit is provided which will isolate the converter from the supply when current in the load goes above the rated value of load current. The power circuit block in the above mentioned block diagram is BLIL PFC boost converter. A current sensing element will sense the output current of the converter which will be compared with a constant current set in the comparator. Current set in the comparator will be equal to the rated load current of the converter. When the output from the current sensing element exceeds the current set in the comparator, pulses will be generated from the comparator which will be given to the trip circuit. Converter can be isolated from the supply in two ways depends upon the load
If the load current exceeds the rated load current converter is permanently isolated from the supply. This method of isolation is used for the load which requires desired voltage and current. When the load current exceeds the rated load current converter is isolated from the supply and converter is reconnected to the supply whenever the load current is below the rated load current. In this method output voltage and current is not at the desired voltage and current levels.The mode of operation is same as that of BLIL converter.

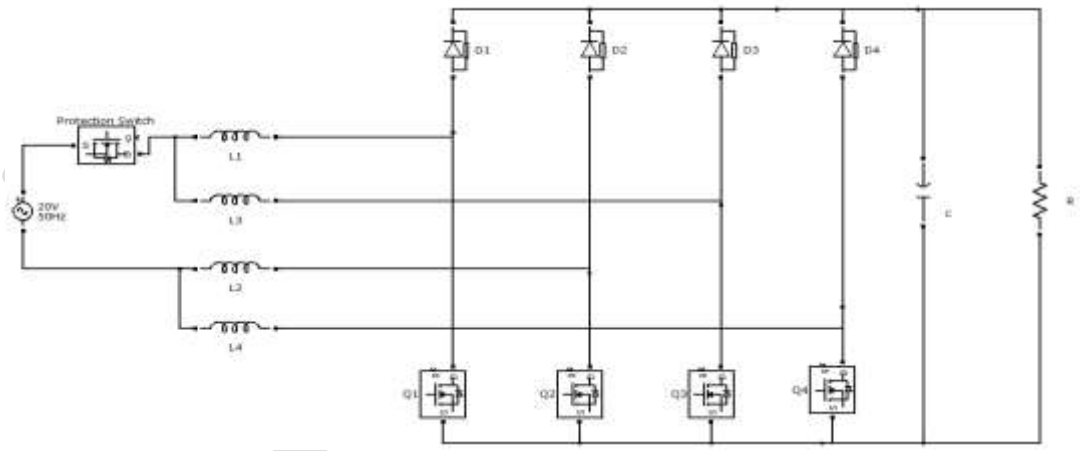

Figure 3.1: BLIL with Over Current Protection

B. Design

Design procedure of this converter is explained with the following specifications.

Input Voltage = 20V
Load Current = 1.5A
Duty Ratio = 0.6

D = $\frac{V_0 - V_i}{V_0}$ so the output Voltage = 50V.

Resistance across the load = $\frac{V_0}{V_i}$ = 33Ω

Ripple Current(ΔI) = 0.45A.

$\Delta I = \frac{1}{L_3 + L_4}(V_0 - V_i)(1 - D)T_s$, Assuming $L_3 = L_4$.

L_3 = 1.6mH. Assuming Ripple Current = 0.08%.

ΔV = 0.4 V

C = $\frac{V_0 * D}{f * \Delta V * R}$ = 9000µF.

SIMULATION MODEL AND RESULTS

BLIL Converter is simulated with Duty Ratio = 0.6 with a protection switch .The input ac Voltage = 20V and we get a output Voltage = 50V at switching frequency = 25KHz . The designed value for different duty ratio is used to get the best possible PFC in the circuit as shown in the table 4.1. Due to the interleaving operation in BLIL PFC boost converter the inductive effect will get cancelled. The interleaving operation in positive half cycle will cancel the ripples in inductor currents IL1 and IL3. The ripple cancellation in inductor currents IL1 and IL3 during the positive half cycle operation is shown in Fig.4.1. Similarly during the negative half cycle ripples in inductor currents IL2 and IL4 will cancel each other.

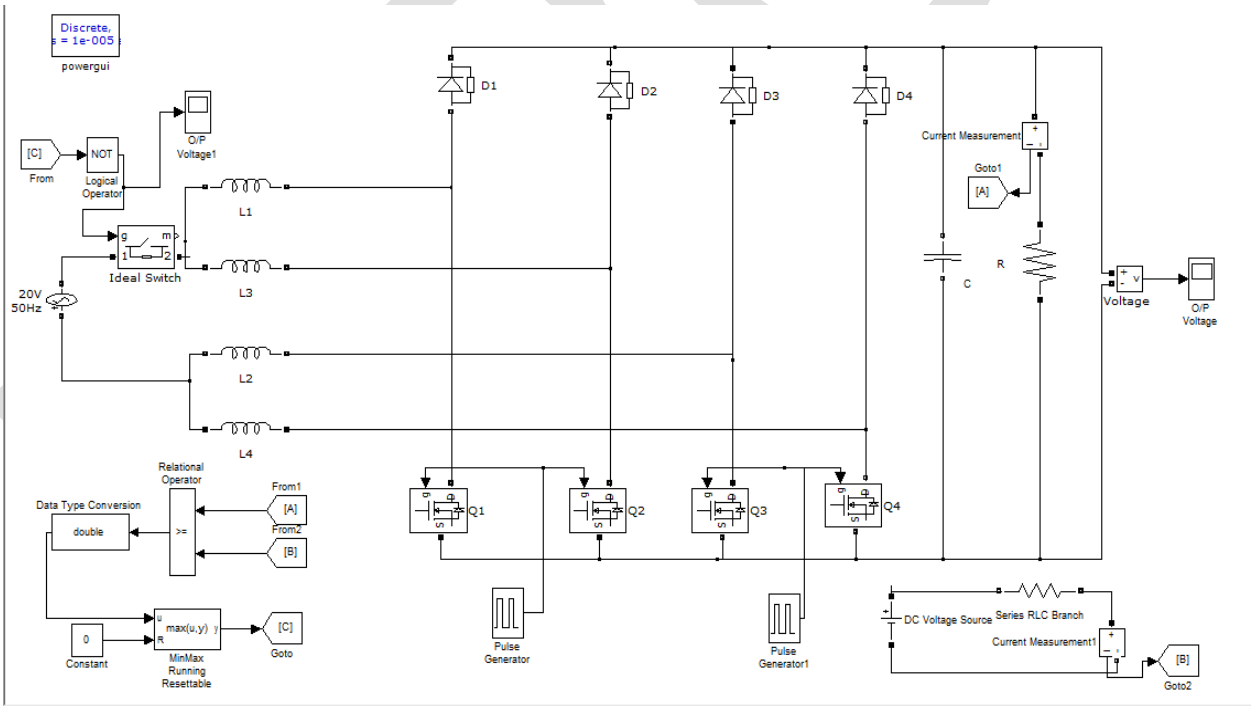

Figure 4.1: Simulink Model of BLIL Converter with Over Current Protection

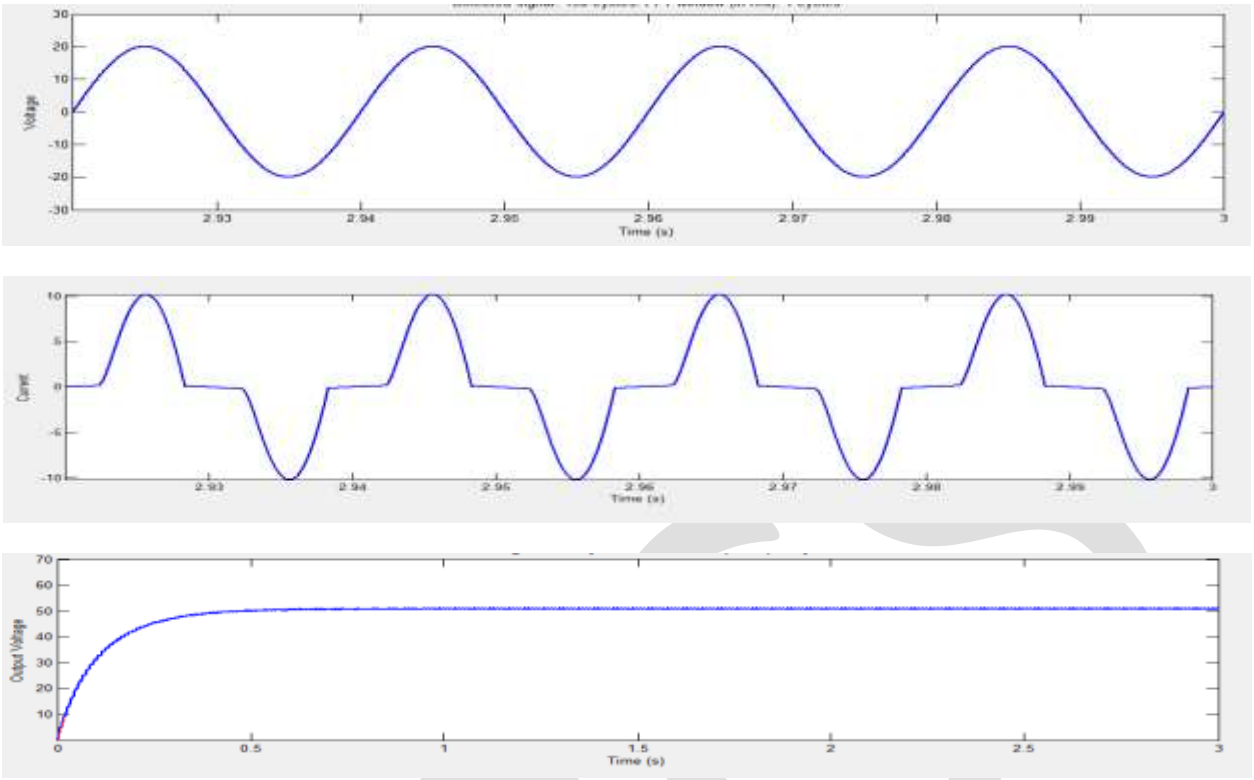

Figure 4.2: Simulink Result of BLIL a) Input Voltage b) Input Current c)Output Voltage

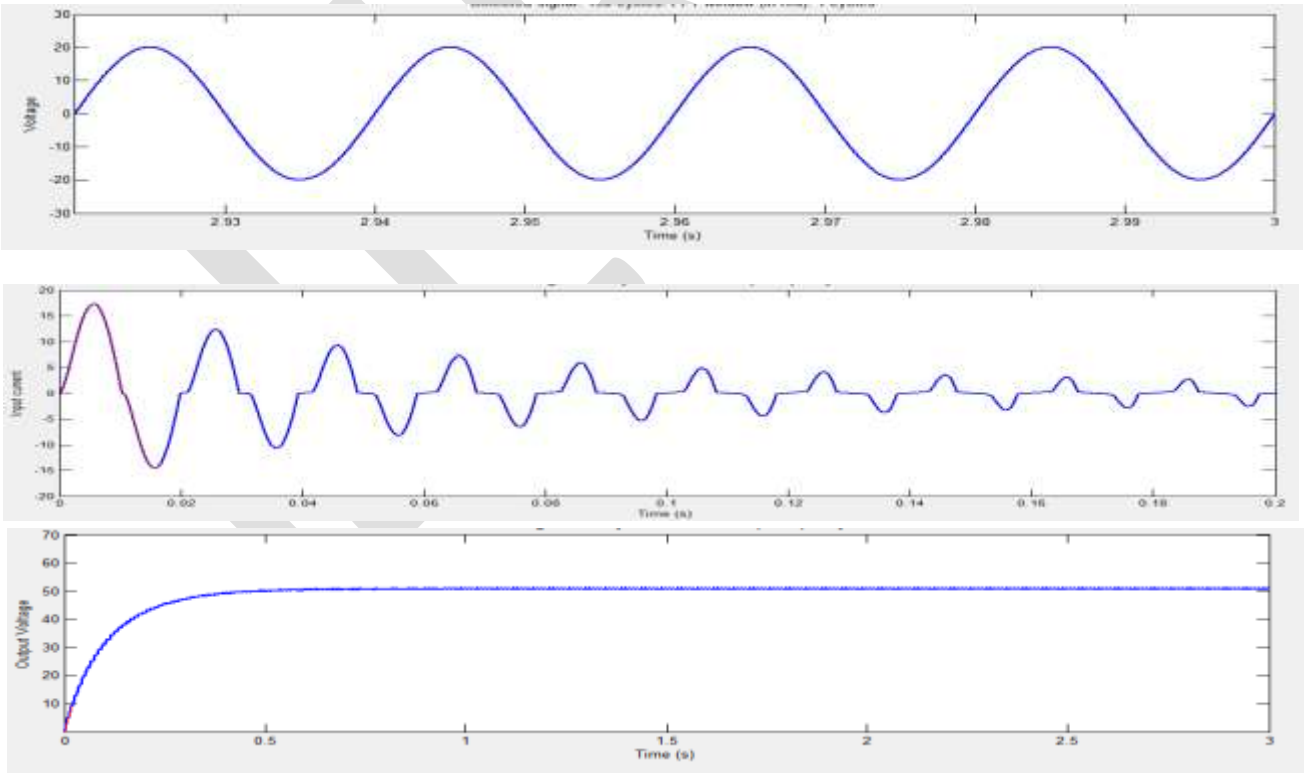

Figure 4.3: Simulink Result of BLIL with permanent isolation a) Input Voltage b) Input Current c)Output Voltage

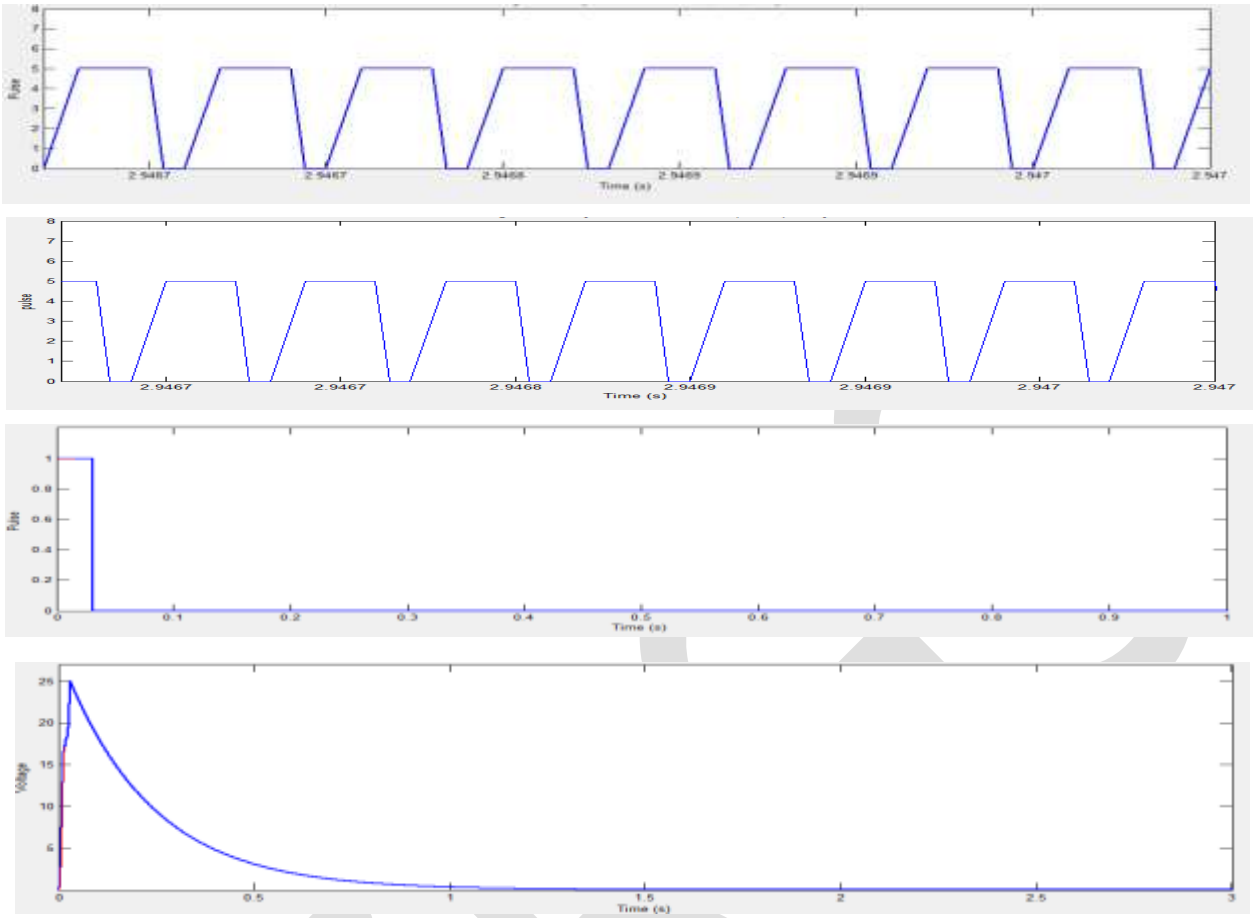

Figure 4.4: Simulink Result of BLIL Permanent Isolation a) Converter switching pulses b) Protection Pulse c)Input Voltage

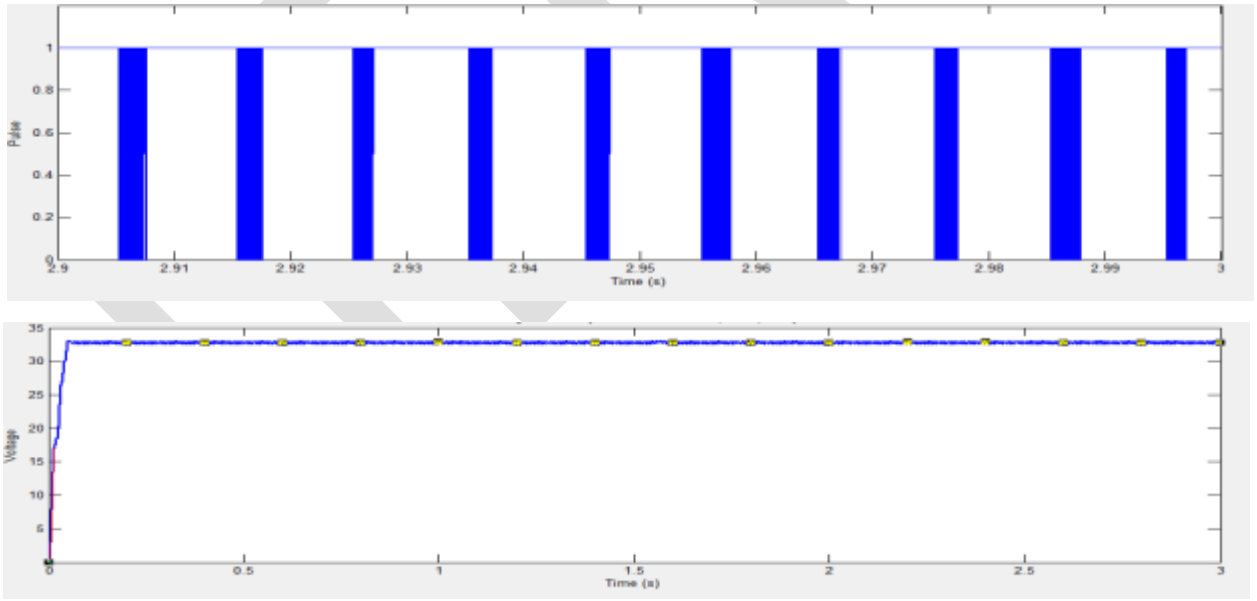

Figure 4.5: Simulink Result of BLIL Non - Permanent Isolation a) Protection Pulse c)Output Voltage

The output voltage waveform of the converter with permanent isolation is shown in Fig.4.4. In simulation comparator set current is 1A that is when output current exceeds 1A tripping occur. The output voltage of the converter is reduced to zero when tripping occurs. The tripping is done through a switch. The gating signal to the switch is shown in Fig.4.5. Whenever load current exceeds rated load current gate signal to the switch is reduced to low level and maintained at the low level. In Fig 4.5 shows the non – permanent

isolation of the BLIL converter where the isolation will be used for detecting minor over currents that occur in the circuit for a short time period then the circuit will be braked from the input for a short period and then reconnected the only problem with this circuit is that the converter boost efficiency reduces. Looking on the advantage side of reliable protection circuit BLIL topology with a protection circuit is more useful.

Converter	THD	Power factor
Boost Converter	0.4287	0.800
BLIL with D<0.5	0.0708	0.997
BLIL with D>0.5	0.1063	0.994

CONCLUSIONS

Conventional PFC boost converter and BLIL PFC boost converter were simulated using MATLAB/SIMULINK. It was found that the total harmonic distortion got reduced and the input side power factor got improved with BLIL PFC boost converter. Interleaving operation i.e. cancellation of the ripples at the input is obtained using simulations. Form the above two observations it is clear that the BLIL PFC boost converter is a better topology compared to the conventional PFC boost converter. Isolation was provided for the converter to isolate converter from supply in case of occurrence of overcurrent. When the load varies, the output voltage is maintained constant by providing the closed loop control when the input voltage is 20V we get an output voltage of 50V with a power factor of .997. BLIL model is made over - current protective to provide safe operating range to the converter. BLIL with over current protection and closed loop can be employed in a PFC application to get a protective as well as power factor close to unity.

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