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Design of Low Power High Speed 16 bit Adders with McCMOS in 45nm Technology

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Abstract-Adder are the core component of processors and digital design architecture. Also, not only addition, but performs many other arithmetic operations such as subtraction, division and multiplication. The focus of VLSI technology is to reduce power consumption, enhancing the performance and speed of a digital circuit. Less power consumption is the ultimate attention for any computation. In this paper, 16 bit adders are designed using one such technique i.e. McCMOS and compared for power dissipation, delay, leakage power and power delay product. Different types of adders have been designed using Multiple channel CMOS (McCMOS) technology and compared with conventional with 45nm technology. The simulation result shows that the average power reduces to 30 – 35% less and PDP is reduced to 15- 17% than the power and PDP of the conventional CMOS. Hence the technique can be used for low leakage high speed application. The simulation has been carried out in tanner tool EDA 14.1 with 1V power supply.

Keywords: Carry Skip Adder, Carry Select Adder, Modified Carry Skip Adder, Modified Carry Select Adder McCMOS, ALU (Aritematic logic Unit).

I.INTRODUCTION

Adders are the key components in any arithmetic operation calculation. There are some more operations such as subtraction, division and multiplication which are addition based arithmetic circuits. Adders and multipliers are the most significant part of all data path circuits in digital signal processors and microprocessors. Multiplication process need adders, for the addition in the final step [1]. So it is very clear that the performance of multiplier is totally depends on the performance of the addition i.e. adders. Hence the optimization of the adders will affect the constraints (power, delay, pdp) of the multiplier.

The reduction of propagation delay and power dissipation are the primary concern in modern VLSI designs. This reduction can be done by an effective technique which reduces leakage power as well as average power and delay for the addition of binary numbers. This presented technique increase the speed of the adders. The scheme for controlling the leakage, McCMOS (multiple channel CMOS) [2] has been used to achieve optimized power and performance of the adders. Furthermore, an optimization in elementary unit which will further reduce the parameters of higher order units, for example multiplier. This paper proposed a modified binary adders such as carry bypass adders and carry select adder. The results shows a considerable improved performance is achieved by using McCMOS compare to conventional adder which uses CMOS style and contributes a better performance in applications. The structure of paper is as follows: section II presents basic leakage control using McCMOS; Section III deals with the conventional CMOS adder; Section IV describes the modified adders using McCMOS; Section V encompasses simulation results; and section VI shows conclusion.

II. MCCMOS (MULTIPLE CHANNEL CMOS)

Keeping in mind, the acceptable level down of heat dissipation and power, so to achieve high performance, around 1V low supply voltage and very short channel length is required for the maximum performance of any CMOS design. But this scaling, leads to low threshold voltage and cause increase in leakage current. Also this leakage current will increase the leakage power which is the major issue to be concern in deep sub-micron CMOS technology design. The MOS scaling technology depends on following parameters [3]

$$L_{min} = A[X_j\, t_{ox}(w_s + w_d)^2]^{1/3} \qquad \ldots (1)$$

Here L_{min} is the minimum channel length, long channel subthreshold behaviour will be observed. Here 'A' is the proportionality factor, 't_{ox}' is oxide thickness, 'X_j' is junction depth, 'w_d' is source depletion depth and 'w_d' is drain depletion depth in a one dimension abrupt junction formulation [4-5].

The parameters of MOSFET scaling is described as

$$w_d = \sqrt{2}L_B\,[B(V_{DS} + V_{bi} + V_{BS})]^{1/2} \quad \ldots (2)$$

Where $L_B = {}^{\in_s}/_{BqN_a}$ = Bulk Debye length And $= ({}^{kT}/_{q})^{-1}$,

V_{DS} = Drain to source voltage,

V_{BS} = Body to source reverse bias, and

V_{bi} = Built in voltage of the junctions.

The threshold voltage, short channel effect, current carrying ability, gate oxide, leakage current edge, and power supply are the important parameters which need to be concern in deep sub-micron designs. The possibility of achieving the tremendous leakage control is non minimum transistor length without the other accepted leakage current controlling technique disadvantage.

While lowing the supply voltage, threshold voltage will scale down in order to maintain the actual performance requirement. However such scaling increase the leakage current. A technique in this paper name as McCMOS, to achieve an improved leakage control together with optimized power and performance. The leakage power is controlled by using a nonminimum transistor length of at least one transistor of the circuit in noncritical path which results in increase in channel resistance, due to which leakage current reduces [6]. However, same technique is applied in critical path but here channel width increases for performance requirement.

In this paper, we use 45nm model file. To reduce the leakage current in non-critical path, non minimum length of nmos is used and for critical path, channel length is minimum but increasing the channel width of the pmos to satisfy performance. The figure 1 shows the inverter with McCMOS technique.

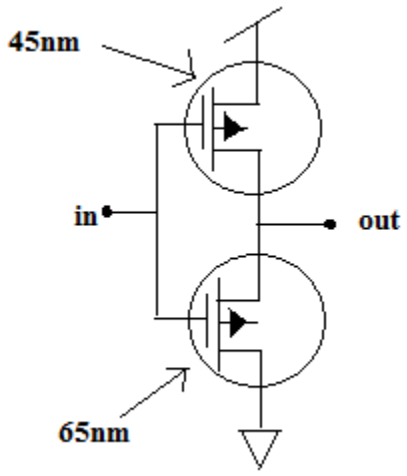

Figure 1: McCMOS Inverter

III. CONVENTIONAL ADDER ARCHITECTURE

The simple binary addition usually carried out using full adder. However, if we add multiple bits then the easier method is to connect full adder in series. The technique use for adding multiple bit is defined as adders. RCA (ripple carry adder) is most common among the adders, although implementation of this adder for small length is effective. But, most desktop computers now a days using word length of 32 bit, while server require 64 bit; and the fast computer, such as super computers, mainframes etc., require word length of up to 128 bits. The overall performance limit by the adder's computational time. And the dependence of this computational time is on number of bits of the adder. Many such architecture are proposed to eliminate or reduce the proportional dependency. This section describes the conventional adders.

A. Carry Skip Adder

Carry skip adder is much more like a ripple carry adder but in this adder implementation there is a carry skip (bypass) path. As in ripple carry adder, full adder needs to wait for the incoming carry to generate outgoing carry [7]. Hence the dependency is eliminated by introducing a bypass to speed up the computation. It divide the no. of bits of adder in even stages. The figure 2 shows carry propagation and figure 3 show 4 bit carry bypass adder. Hence this adder reduce the carry computation delay by bypassing carry of successive adder stage.

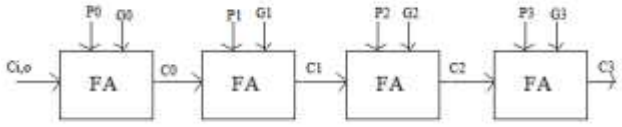

Figure 2 Carry Propagate

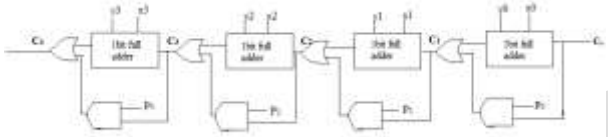

Figure 3: 4 bit Carry Skip Adder

B. Carry Select Adder

Carry select adder is fastest and conditional sum adder used for many processors for fast arithmetic computation. In carry select adder several group of addition are performed, two addition are performed parallel using double RCA. One evaluate the result with carry '1' and other evaluate with carry '0' [7]. Once the input carry is computed, the output sum and output carry C_{out} is selected by the multiplexer. From the circuit point of view, two carry result is generated. Although this adder increase the number of units. But its computation is much faster than usual computation. Figure 4 shows 4 bit carry select adder. The 16 bit Carry select adder is constructed by cascading a number of equal length adder stage.

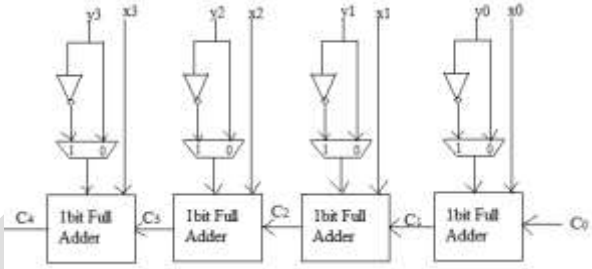

Figure 4: 4 bit Carry Select Adder

IV. MODIFIED ADDER ARCHITECTURE

A. Modified Carry Skip adder

To eliminate the dependency of input carry on output carry, we need to bypass carry in such a way that the speed of computation increase. It is known that the incoming carry $C_{i,o}$ = 1 propagates through the complete unit of adders and provoke the output carry to 1, , while all propagating signal to be 1. Then this information can be used to speed up the adder operation. For 8 bit carry select adder, bypass BP=P0P1P2P3P4P5P6P7P8 = 1, then the incoming carry is forward to next module or bypass immediately and if in case BP = 0 then the normal operation occur. An approximate propagation delay for the worst case is given by

$$t_p = t_{setup} + Mt_{carry} + \left(\frac{N}{M} - 1\right) t_{bypass} + (M-1)t_{carry} + t_{sum} \ldots (3)$$

Where N is number of bits and M is number of bit per stage. t_{setup}, t_{sum} are fix delay. t_{carry} is delay through a full adder and t_{bypass} is propagation delay due to additional bypass used, MUX.

If $P_0P_1P_2P_3P_4P_5P_6P_7P_8$ =1, then

$C_{o,7} = C_{i,o}$

Else DELETE OR GENERATE occur.

B. Modified Carry Select Adder

Because of the dual ripple carry adder more area is required and carry out stage ripple at each stage. Considering the block of an adder, adding bits K to K+3. Instead of waiting for previous carry to come and then compute the computation further, there are two possibilities generated. First, if input carry is '0' and other if input carry is '1', which means two path of carry need to implement. When either the result are decided then the path is selected using multiplexer. The figure 5 shows the 16bit modified carry select adder with dual carry look ahead adder. Propagation delay for the worst case of the unit is

$$t_{add} = t_{setup} + Mt_{carry} + \left(N/M\right)t_{mux} + t_{sum} \ldots .(4)$$

Where N is number of bits and M is number of bit per stage. t_{setup}, t_{mux} and t_{sum} are fix delay. t_{carry} is delay through a full adder.

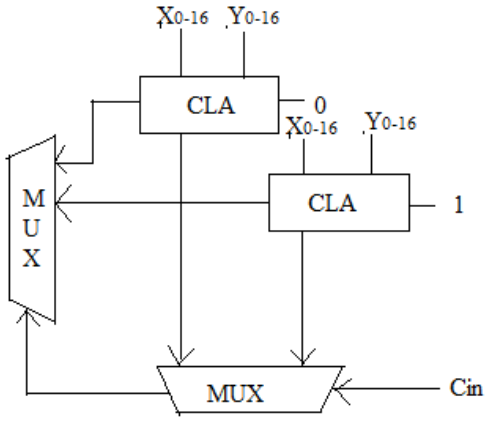

Figure 5: Modified Carry Select Adder

V. SIMULATION RESULTS

The simulation results are carried out on 45 nm node technology at 1V using tanner tool. Adder using McCMOS have very low power consumption compare to conventional [8]. The overall decrease in PDP is 30 -33% of the adder. Table 1, Table 2 and Table 3 shows the comparative study of the 4 bit, 8 bit and 16 bit conventional McCMOS and Modified McCMOS, respectively. Comparing the average power and PDP of 4 bit CSKIP and CSELECT from figure 6 that CSKIP have very less power and PDP than CSELECT.

The simulation results of power and PDP is compared graphically for different bits 4, 8, 16 in figure 6, 7, 8 respectively.

Table 1: Comparison of 4 bit Adders

Adder	**Conventional CMOS**				**Modified McCMOS**			
	Power	Delay	PDP	Transistor count	Power	Delay	PDP	Transistor count
CSKIP	6.85E-06	2.04E-08	1.39E-13	252	5.02E-06	2.04E-08	1.03E-13	252
CSELECT	8.55E-06	2.04E-08	1.74E-13	288	5.25E-06	2.05E-08	1.08E-13	288

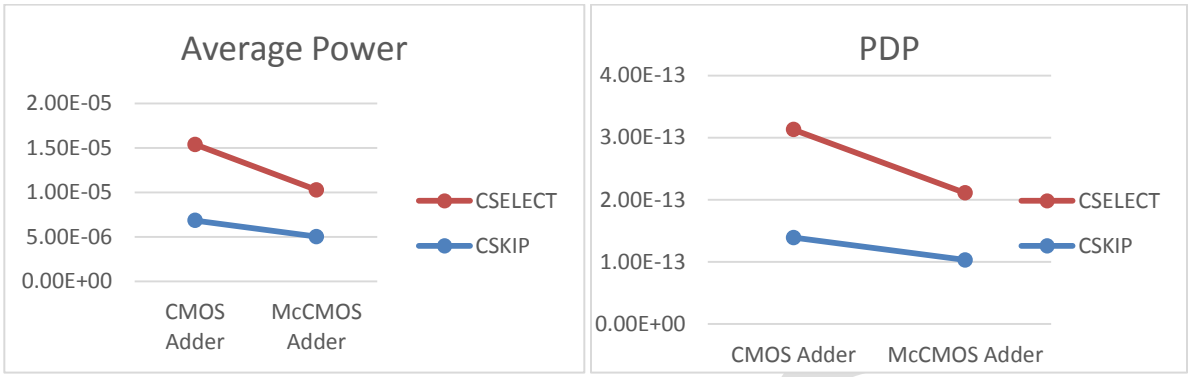

Figure 6: Comparison of 4 bit average power and PDP

Table 2: Comparison of 8 bit Adders

Adder	**Conventional CMOS**				**Modified McCMOS**			
	Power (10^{-6} W)	Delay (10^{-8} sec)	PDP (10^{-13} J)	Transistor count	Power (10^{-6} W)	Delay (10^{-8} sec)	PDP (10^{-13} J)	Transistor count
CSKIP	1.43E-05	2.03E-08	2.91E-13	492	9.74E-06	2.04E-08	1.99E-13	492
CSELECT	1.69E-05	2.03E-08	3.44E-13	564	1.10E-05	2.05E-08	2.25E-13	564

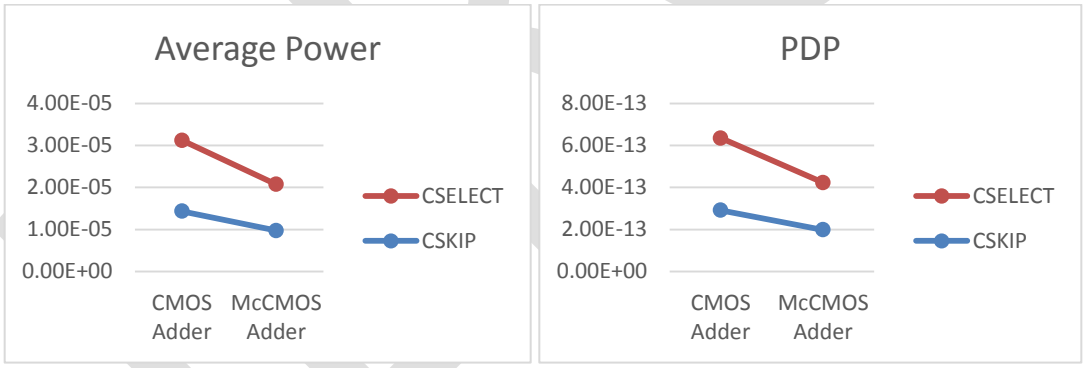

Figure 7: Comparison of 8 bit average power and PDP

Table 3: Comparison of 16 bit Adders

Adder	**Conventional CMOS**				**Modified McCMOS**			
	Power (10^{-6} W)	Delay (10^{-8} sec)	PDP (10^{-13} J)	Transistor count	Power (10^{-6} W)	Delay (10^{-8} sec)	PDP (10^{-13} J)	Transistor count
CSKIP	2.28E-05	2.03E-08	4.64E-13	984	1.97E-05	2.04E-08	4.02E-13	984
CSELECT	3.51E-05	2.03E-08	7.13E-13	1128	2.23E-05	2.05E-08	4.56E-13	1128

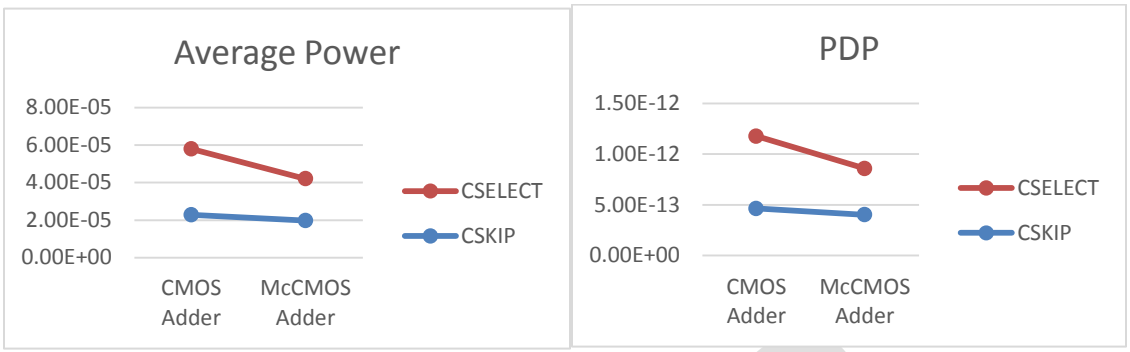

Figure 8: Comparison of 16 bit average power and PDP

VI. CONCLUSION

In this paper, design and implementation of carry skip adder and carry select adder. Different bits of adder has been designed and compare for the conventional CMOS and Modified McCMOS. Comparison shows that the average power reduces to 30 – 35% less and PDP is reduced to 15- 17% than the power and PDP of the conventional CMOS. From table 1, table 2, and table 3 it is also clear that the number of transistor of CSKIP is much more less than CSELECT. Hence, the overall performance of the carry skip adder is efficient with less power consumption and high speed.

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