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Design of Modified Carry Select Adder for Addition of More Than Two Numbers

Jasbir Kaur[1] and Lalit Sood[2]

Assistant Professor, ECE Department, PEC University of Technology, Chandigarh, India [1]

PG Scholar, Electronics (VLSI Design), PEC University of Technology, Chandigarh, India [2]

jasbirkaur@pec.ac.in[1] and lalitsood3@gmail.com[2]

Abstract— Due to rapidly growing system-on-chip industry, not only the faster units but also smaller area and less power has become a major design constraint for VLSI community. Further, demand for high speed is continuously increasing. In processors, most commonly used arithmetic operation is the addition operation. It is the adder delay that determines the maximum frequency of operation of the chip. Different topologies have been put forward, each providing trade-off between different performance parameters and as such no design is considered as superior. Carry select adder is considered to be best in terms of speed and provide compromise between ripple carry adder and carry look-ahead adder, but to a lesser extent at the cost of its area. In this paper, a modified carry select adder is designed that can add up to five 16-bit numbers with the help of compressors by following basic carry select addition procedure which is efficient to increase its speed of operation. This design is simulated using Cadence Tool.

Keywords— VLSI, High Speed, Ripple Carry Adder, Carry Look ahead Adder, Carry Select Adder, Modified Carry Select Adder, Cadence Tool.

I. INTRODUCTION

Due to the rapid growth of portable electronic component the low power arithmetic circuits become very important in VLSI industry. Multiplier-Accumulator (MAC) unit is the main building block in DSP processor. Full Adder is a part of the MAC unit can significantly affect the efficiency of whole system. Hence the reduction of power consumption of Full Adder circuit is necessary for low power application. Carry Select Adder are used for high speed application by reducing propagation delay. The basic operation Carry Select Adder (CSLA) is parallel computation. CSLA generates many carriers and partial sum [3]. The final sum and carry are selected by multiplexers (mux). Multiple pairs of Ripple Cary Adders (RCA) are used in CSLA structure. Hence, the CSLA is not area efficient.

This paper proposes the design of modified carry select adder which has two main features. One is this adder follows the basic procedure of carry select addition that increases speed of operation. Second is the compressors used for addition operate simultaneously and are independent of previous stage outputs that also contribute in increased speed of multiplication.

This paper is partitioned into six sections. Section II describes the conventional method for addition. Section III gives introduction to modified carry select adder. Section IV deals with design of modified carry select adder. Section V compares the results of proposed adder with conventional one. Conclusions and references follow.

II. CONVENTIONAL ADDER

The basic algorithm for addition of five numbers, *P*, *Q*, *R*, *S* and *T* makes use of the associative property of addition. That is, if 'Sum' can be written as sum of *P*, *Q*, *R*, *S* and *T*, then $Sum = P + Q + R + S + T$ can be written in a number of ways. Few examples are given below:

$Sum = (P + Q) + (R + S) + T;$

or

Sum = P + (Q + R) + (S +T);

or

Sum = (P + Q + R) + (S +T);

Or

… (a number of such combinations)

The terms on the right hand side can be readjusted and grouped together as per requirement. An addition algorithm finds a simple way to allow a simple calculation of the addends.

A bit-wise addition of five different 16-bit binary numbers using conventional method can be described with the help of Table 1. The schematic diagram for conventional adder is shown in Figure 1.

Table 1: Bit-wise addition of five 16-bit numbers using conventional method

Bits to be added	Sum	Carry[0]	Carry[1]
P[0],Q[0],R[0],S[0], T[0]	Sum[0]	$C_0[0]$	$C_0[1]$
P[1],Q[1],R[1],S[1], T[1],$C_0[0]$	Sum[1]	$C_1[0]$	$C_1[1]$
P[2],Q[2],R[2],S[2], T[2],$C_1[0]$,$C_0[1]$	Sum[2]	$C_2[0]$	$C_2[1]$
P[3],Q[3],R[3],S[3], T[3],$C_2[0]$,$C_1[1]$	Sum[3]	$C_3[0]$	$C_3[1]$
P[4],Q[4],R[4],S[4], T[4],$C_3[0]$,$C_2[1]$	Sum[4]	$C_4[0]$	$C_4[1]$
P[5],Q[5],R[5],S[5], T[5],$C_4[0]$,$C_3[1]$	Sum[5]	$C_5[0]$	$C_5[1]$
P[6],Q[6],R[6],S[6], T[6],$C_5[0]$,$C_4[1]$	Sum[6]	$C_6[0]$	$C_6[1]$
P[7],Q[7],R[7],S[7], T[7],$C_6[0]$,$C_5[1]$	Sum[7]	$C_7[0]$	$C_7[1]$
P[8],Q[8],R[8],S[8], T[8],$C_7[0]$,$C_6[1]$	Sum[8]	$C_8[0]$	$C_8[1]$
P[9],Q[9],R[9],S[9], T[9],$C_8[0]$,$C_7[1]$	Sum[9]	$C_9[0]$	$C_9[1]$
P[10],Q[10],R[10], S[10],T[10],$C_9[0]$, $C_8[1]$	Sum[10]	$C_{10}[0]$	$C_{10}[1]$
P[11],Q[11],R[11], S[11],T[11],$C_{10}[0]$, $C_9[1]$	Sum[11]	$C_{11}[0]$	$C_{11}[1]$
P[12],Q[12],R[12], S[12],T[12],$C_{11}[0]$, $C_{10}[1]$	Sum[12]	$C_{12}[0]$	$C_{12}[1]$

P[13],Q[13],R[13], S[13],T[13],C_{12}[0], C_{11}[1]	Sum[13]	C_{13}[0]	C_{13}[1]
P[14],Q[14],R[14], S[14],T[14],C_{13}[0], C_{12}[1]	Sum[14]	C_{14}[0]	C_{14}[1]
P[15],Q[15],R[15], S[15],T[15],C_{14}[0], C_{13}[1]	Sum[15]	C_{15}[0]	C_{15}[1]
C_{15}[0], C_{14}[1]	Sum[16]	C_{16}[0]	0
C_{16}[0], C_{15}[1]	Sum[17]	C_{17}[0]	0
Carry out	C_{17}[0]	0	0

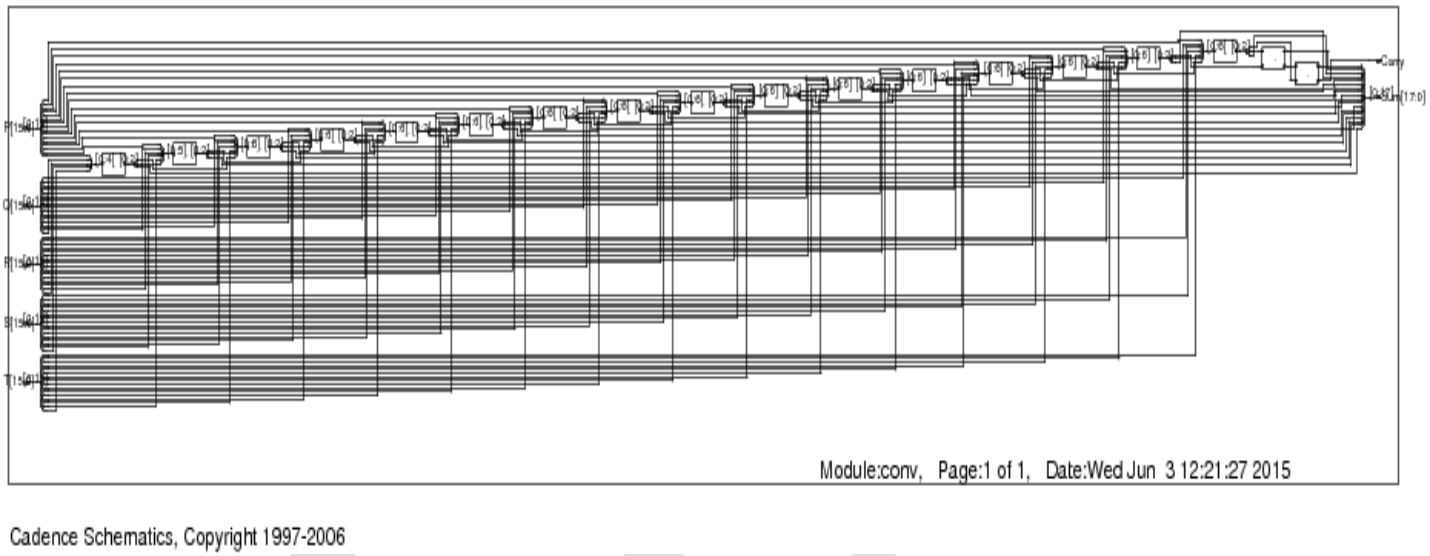

Figure 1: Schematic diagram of Conventional Adder

III. Introduction to Modified Carry Select Adder (MCS*l*A)

Modified Carry Select Adder is designed to add up to five 16-bit numbers. This MCS*l*A is made up of two components. First component is compressor that compresses five bits into two bits. Second component is carry select adder that generates the result by using ripple carry adders and multiplexers.

A. Compressor

For compressing five bits into two bits, two compressors are used. One is 3:2 compressor and another one is 5:3 compressor.

(i) 3:2 Compressor

3:2 Compressor is simply a full adder that adds three bits and generates two bit output as sum and carry [10]. The block diagram of 3:2 compressor is shown in Figure 2(a).

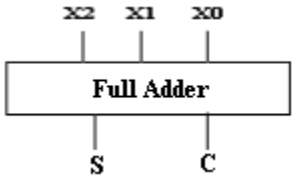

Figure 2(a): Block Diagram of 3:2 Compressor

(ii) 5:3 Compressor

5:3 Compressor is made up of two full adders and one half adder. It is designed to add five bits and generates final sum of three bits [8]. The block diagram of 5:3 compressor is shown in Figure 2(b).

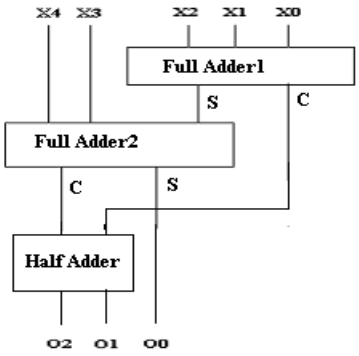

Figure 2(b): Block Diagram of 5:3 Compressor

B. Carry Select Adder

Carry Select Adder (CS*l*A) architecture consists of independent generation of sum and carry i.e., Cin=1 and Cin=0 are executed in parallel [6]. Depending upon Cin, the external multiplexers select the carry to be propagated to next stage. Further, based on the carry input, the sum will be selected. Hence, the delay is reduced. However, the structure is increased due to the complexity of multiplexers [4].The architecture of CS*l*A is shown in Figure 3.

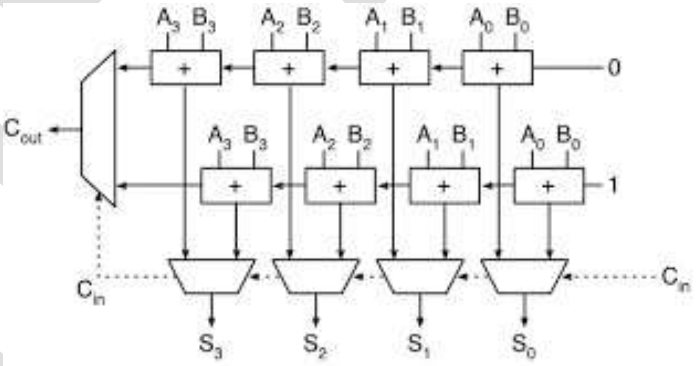

Figure 3: Block Diagram of CS*l*A

IV. Design of Modified Carry Select Adder

This MCS*l*A takes five 16-bit numbers P, Q, R, S and T as input and generates 18-bit sum and a carry. The architecture of MCS*l*A is shown step by step with the help of Figure 4(a), Figure 4(b), Figure 4(c), Figure 4(d) and Figure 4(e).

The schematic diagram for MCS*l*A is shown in Figure 5.

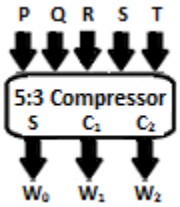

Figure 4(a): 16-bit 5:3 Compressor

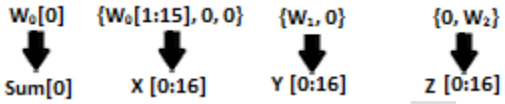

Figure 4(b): Rearrangement of bits

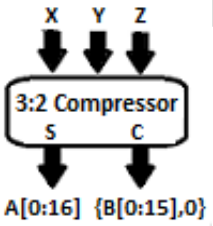

Figure 4(c): 17-bit 3:2 Compressor

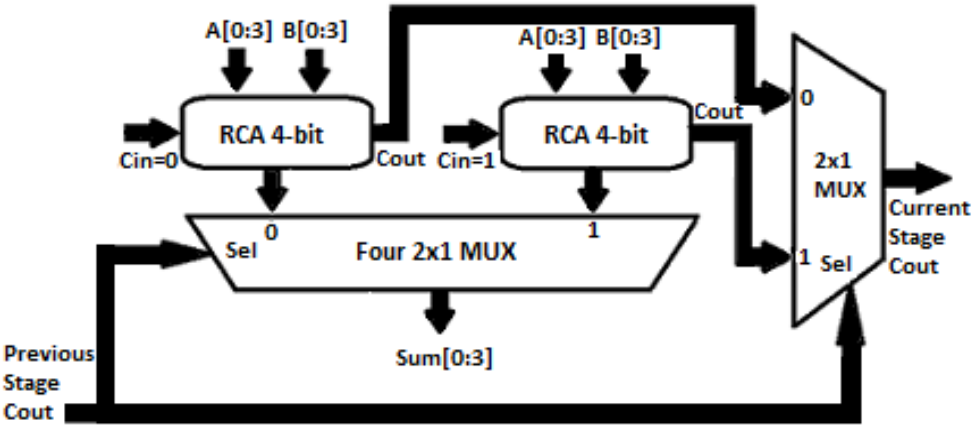

Figure 4(d): Basic Block of CS*l*A

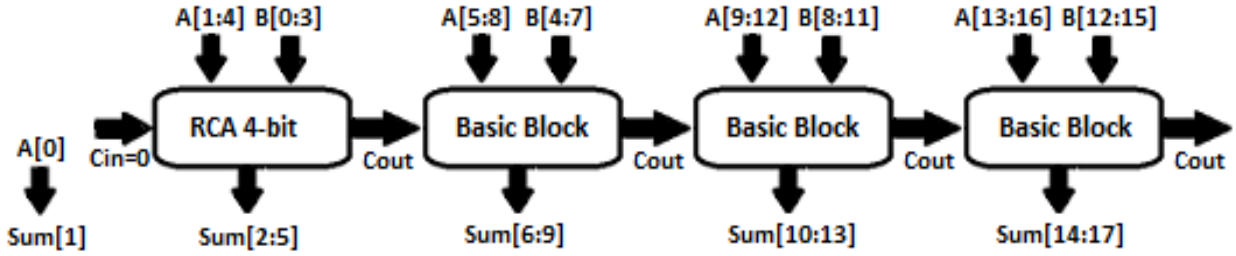

Figure 4(e): Block Diagram of CS*l*A

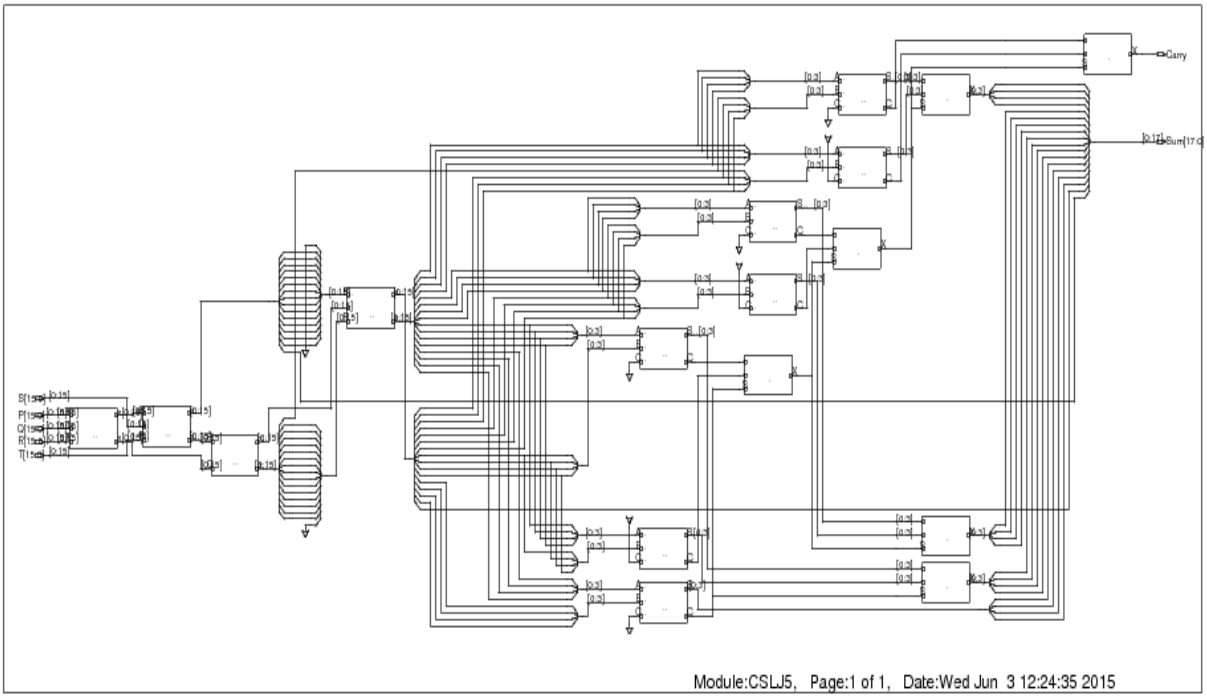

Figure 5: Schematic Diagram of MCS*l*A

V. Comparison

In this paper, the proposed modified carry select adder and conventional adder have been simulated using Cadence Tool. The comparison is done on the basis of basic parameters such as power consumption, speed of operation and area used. The comparative results of these two adders are shown in Table 2.

Table 2: Comparison between designed adder and conventional adder

Parameter	% increase/decrease for proposed adder as compared to conventional adder
Power	60.48% increased
Delay	82..66% decreased
Area	43.90% increased

VI. Conclusions

Different types of adder topologies are used for addition of binary numbers [1]. On comparing different adder topologies, it is found that carry select adder is the fastest one among other mostly used adders [2]. The carry select adder is modified to add up to five 16-bit numbers. This proposed adder is 82.66% faster than conventional adder. It can be used for high speed applications where area and power are not major issues.

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