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Efficient Implementation of Parallel Linear Phase FIR Digital Filters for Symmetric Convolution using Polyphase Decomposition

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Abstract- This paper presents very efficient method that greatly reduces the consumption of hardware during design of FIR filters. Parallel processing together with linear phasing is a powerful technique which can be used to increase the throughput of the FIR filter or reduce the power consumption of the FIR filter. FIR filters are designed by exploiting the nature of symmetric coefficients. With the efficient usage of symmetric coefficients reduces the number of multipliers with increasing the number of adders, which does not affect the hardware cost to a great extent. Reduction in multiplier is advantageous with increase in certain number of because adders weight less in cost in terms of its silicon area and also the number of sub filter blocks remains fixed and does not increase along with the length of the FIR filter. With combination of fast FIR filtering and area reduction technique, a major reduction of multipliers is done. Overall, the proposed parallel FIR structures can lead to significant hardware savings for symmetric convolutions from the existing FFA parallel FIR filter, especially when the length of the filter is large

Keywords- Digital signal processing (DSP), fast finite-impulse response (FIR) algorithms (FFAs), parallel FIR, symmetric convolution, very large scale integration (VLSI)

I. INTRODUCTION

Digital audio, speech recognition, cable modems, radar, and high - definition television-these are but a few of the modern computer and communications applications rely on digital signal processing (DSP) and application-specific integrated circuits (ASICs). As industries constantly reinvent ASIC chips for lower power consumption and higher efficiency, there is a growing need in VLSI design methodologies for DSP. VLSI architecture theory and algorithms, addresses various architectures at the implementation level, and presents several approaches to analysis, estimation, and reduction of power consumption. to design high-speed, low-area, and low-power VLSI systems for a broad range of DSP applications. In some applications, FIR filters must be low-power or high speed supporting structures. For certain applications like video television broadcasts, higher order FIR filters are required. Design of these filters leads to hardware complexity and consumption of area and power. There are some techniques to reduce the complexity of the larger size filter blocks. In order to design these filters, polyphase decomposition is to be carried out where small-sized sub filter blocks are derived first and those sub-structures are cascaded or iterated to construct larger size filter blocks. This decomposition for FIR filter is used as a processing core to implement sub filters of proposed parallel FIR filters. Furthermore there have been papers proposing the FIR implementation using pipelining and parallel processing. Pipelining leads to increase in number of latches and system latency. Parallel processing increases the sampling rate by replicating the hardware. But parallel processing loses its advantage in practical implementation. Both the techniques reduce the power consumption to some extent. Considering the inefficiency of the above techniques, the basic nature of symmetric coefficients together with the polyphase decomposition is used in this paper to further reduce the amount of multipliers. This paper is organized as follows. A brief introduction is given in Section I , In Section II, the Introduction in Pipelining and Parallel Processing, In Section III Traditional FIR Algorithm and FFA, in section IV Proposed structure for symmetric convolution, Section V gives Proposed cascading scheme for FFA , Section VI conclusion And Section VII gives Acknowledgment.

II.PIPELINING AND PARALLEL PROCESSING

Pipelining transformation leads to a reduction in the critical path, which can be exploited to either increase the clock speed or sample speed or to reduce power consumption at same speed. In parallel processing, multiple outputs are computed in parallel in a clock period. Therefore, the effective sampling speed is increased by the level of parallelism. Similar to the pipelining, parallel processing

can also be used for reduction of power consumption. It is of interest to note that parallel processing and pipelining techniques are duals of each other, and if a computation can be pipelined, it can also be processed in parallel. Both techniques exploit concurrency available in the computation in different ways. While independent sets of computations are computed in an interleaved manner in a pipelined system, they are computed using duplicate hardware in parallel processing mode.

Designing a Parallel FIR System: Consider the 3-tap FIR filter described by, this system is a single-input single-output (SISO) system and is described by

$$y(n) = ax(n) + bx(n-1) + cx(n-2)$$

To obtain a parallel processing structure, the SISO system must be converted into a MIMO (multiple-input multiple-output) system. For example, the following set of equations describe a parallel system with 3 inputs per clock cycle (i.e., level of parallel processing $L = 3$).

$$y(3k) = ax(3k) + bx(3k-1) + cx(3k-2)$$

$$y(3k+1) = ax(3k+1) + bx(3k) + cxz(3k-1)$$

$$y(3k+2) = ax(3k+2) + bx(3k+1) + cx(3k)$$

Here k denotes the clock cycle. As can be seen, at the k-th clock cycle the 3 inputs $x(3k)$, $x(3k + 1)$ and $x(3k + 2)$ are processed and 3 samples are generated at the output. Parallel processing systems are also referred to as *block processing* systems and the number of inputs processed in a clock cycle is referred to as the *block size*. Because of the MIMO structure, placing a latch at any line.

III. TRADITIONAL FIR ALGORITHM AND FFA

A. Traditional FIR Algorithm

Assuming {x (n)} is an infinite-length input sequence and {h (i)} are the length-N FIR filter coefficients and {h (i)} are output sequence y(i) N-tap FIR filter which can be expressed in the general form as

$$y(n) = \sum_{i=0}^{N-1} h(i)x(n-i), \quad n = 0,1,2,...,\infty \qquad (1)$$

Traditional L- parallel FIR filter can be derived using polyphase decomposition as

$$\sum_{p=0}^{L-1} Y_p(z^L)z^{-p} = \sum_{q=0}^{L-1} X_q(z^L)z^{-q} \sum_{r=0}^{L-1} H_r(z^L)z^{-r} \qquad (2)$$

Where, $Xq = \sum_{k=0}^{\infty} z - kx(Lk + q)$,

$$Hr = \sum_{k-0}^{\left(\frac{N}{L}\right)-1} z - kx(Lk + r)$$

$$Yp = \sum_{k=0}^{\infty} z - kx(Lk + p)$$

For p, q, r = 0, 1, 2, 3, ……., L-1. From this FIR filtering equation, it shows that the traditional FIR will require L^2 – FIR sub filter blocks of length N/L for implementation.

$$Y_0 = H_0X_0 + z^{-2}H_1X_1$$

$$Y_1 = H_0X_1 + H_1X_0 \qquad (3)$$

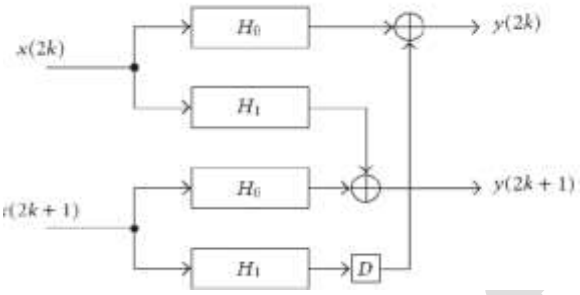

Figure1. Traditional 2-Parallel FIR Filter

B. Two parallel Fast FIR Algorithm

A two- parallel FIR filter can be expressed as

$$Y_0 = H_0X_0 + z^{-2}H_1X_1$$

$$Y_1 = (H_0 + H_1)(X_0 + X_1) - H_0X_0 - H_1X_1 \qquad (4)$$

For FFA with (4) require three FIR sub filter blocks of length N/2, one preprocessing and three post processing adders, and 3N/2 multipliers and 3(N/2-1)+ 4 adders, which reduces approximately one fourth over the traditional two- parallel filter hardware cost from (3). As implementation cost of a multiplier is greater than that of an adder, the cost to implement the parallel filtering structure can be approximated as being proportional to the number of multipliers required for the implementation. The hardware consumption of parallel fast FIR filter is 25% less when compared to traditional parallel FIR filters.

C. Three parallel Fast FIR Algorithm

A three-parallel FIR filter using FFA can be expressed as

$$Y_0 = H_0X_0 - z^{-3}H_2X_2 + z^{-3}\left(H_1 + H_2\right)\left(X_1 + X_2\right) - H_1X_1$$

$$Y_1 = \left(H_0 + H_1\right)\left(X_0 + X_1\right) - H_1X_1 + \left(H_0X_0 - z^{-3}H_2X_2\right)$$

$$Y_2 = \left(H_0 + H_1 + H_2\right)\left(X_0 + X_1 + X_2\right)$$

$$- \left(H_0 + H_1\right)\left(X_0 + X_1\right) - H_1X_1$$

$$- \left(H_1 + H_2\right)\left(X_1 + X_2\right) - H_1X_1 \qquad (5)$$

Above implementation requires six length N/3 FIR sub-filter blocks, three preprocessing and seven post processing adders, and three N multipliers and 2N+4 adders, which has reduced approximately one third over the traditional three-parallel filter hardware cost.

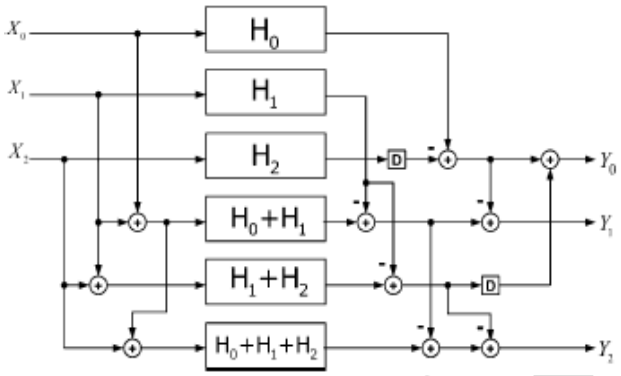

Figure2. Three-parallel FIR Filter implementation using FFA

IV. PROPOSED STRUCTURES FOR SYMMETRIC CONVOLUTIONS

The main idea is to create be low-power or high speed FIR filter. So it is necessary to manipulate the polyphase decomposition to earn as many sub filter blocks as possible exploiting the symmetry of coefficients.

A. Proposed Structure 3A, ((N mod) = 0)

For a set of symmetric coefficients in odd length N, when (N mod 3) equals zero,(8) can earn two more sub filter blocks containing symmetric coefficients than(7) This can be described with an example..

Example: - Consider a 27-tap FIR filter with a set of symmetric coefficients applying to the proposed two-parallel FIR filter.

{h(0),h(1),h(2),h(3),h(4),h(5),

h(6),h(7),h(8),h(9),…,h(26)}

where h(0)=h(26), h(1)=h(25), h(2)=h(24), h(3)=h(23), h(4)=h(22), h(5)=h(21),… ,h(12)=h(14), applying to the proposed two-parallel FIT filter structure , and the top two subfilter blocks will be as

$$H_0 \pm H2 = \{h(0) \pm h(2), h(3) \pm h(5),$$

$$h(6) \pm h(8), h(9) \pm h(7), \ldots h(18) \pm h(19)$$

$$h(20) \pm h(21), h(22) \pm h(23)\}$$

Where

$$h(0) \pm h(2) = \pm(h(24) \pm h(26))$$

$$h(3) \pm h(5) = \pm(h(21) \pm h(23))$$

$$h(6) \pm h(8) = \pm(h(18) \pm h(20))$$

$$h(9) \pm h(11) = \pm(h(15) \pm h(17)) \ldots \quad (6)$$

$$\begin{aligned}
Y_0 &= H_0X_0 + z^{-3} \times \{(H_1 + H_2)(X_1 + X_2) - H_1X_1 \\
&\quad - \Big((H_0 + H_2)(X_0 + X_2) - H_0X_0 \\
&\quad - \frac{1}{2}[(H_0 + H_2)(X_0 + X_2) \\
&\quad - (H_0 - H_2)(X_0 - X_2)]\Big)\} \\
Y_1 &= (H_0 + H_1 + H_2)(X_0 + X_1 + X_2) - (H_1 + H_2)(X_1 + X_2) \\
&\quad - (H_0 + H_2)(X_0 + X_2) \\
&\quad + \Big\{(H_0 + H_2)(X_0 + X_2) - \frac{1}{2} \\
&\quad \times [(H_0 + H_2)(X_0 + X_2) \\
&\quad - (H_0 - H_2)(X_0 - X_2)] - H_0X_0\Big\} \\
&\quad + z^{-3}\{(H_0 + H_2)(X_0 + X_2) \\
&\quad - (H_0 - H_2)(X_0 - X_2)] - H_0X_0\} \\
Y_2 &= H_1X_1 + \frac{1}{2} \times [(H_0 + H_2)(X_0 + X_2) \\
&\quad - (H_0 - H_2)(X_0 - X_2)]
\end{aligned}$$

(7)

Comparing with the existing FFA three-parallel FIR filter structure, the proposed structure leads to two more sub filter blocks, which contain symmetric coefficients. Hence for an N-tap three-parallel FIR filter , the proposed structure can save N/3 multipliers from the existing FFA structure.

B. **Proposed Structure 3B, ((N mod 3)=1)**

For a set of symmetric coefficients in odd length N, when(N mod 3) equals 1,such as N=25, the proposed structure 3B can earn one more sub filter block with symmetric coefficients over the existing FFA as shown in equ.(8) i.e., presented in

$$Y_0 = H_0X_0 + z^{-3} \times \{\frac{1}{2}[(H_1 + H_2)(X_1 + X_2) - (H_1 - H_2)(X_1 - X_2)]\}$$

$$Y_1 = (H_0 + H_1 + H_2)(X_0 + X_1 + X_2) - (H_1 + H_2)(X_1 + X_2) - (H_0 + H_1)(X_0 + X_1) + \left\{(H_1 + H_2)(X_1 + X_2) - \frac{1}{2} \times [(H_1 + H_2)(X_1 + X_2) - (H_1 - H_2)(X_1 - X_2)] - H_2X_2\right\} + Z^{-3}H_2X_2$$

$$Y_2 = (H_0 + H_1 + H_2)(X_0 + X_1 + X_2) - (H_1 + H_2)(X_1 + X_2) - (H_0 + H_1)(X_0 + X_1) + 2\left\{(H_1 + H_2)(X_1 + X_2) - \frac{1}{2} \times [(H_1 + H_2)(X_1 + X_2)] - H_2X_2\right\}$$

(8)

C. Proposed structure 3C, ((N mod 3) =2)

For a set of symmetric coefficients in odd length N, when (N mod 3) equals 2, such as N=23,the proposed structure 3C represented in (9),can earn one more sub filter block containing symmetric coefficients over the existing FF

$$Y_0 = \left\{\frac{1}{2}[(H_0 + H_1)(X_0 + X_1) + (H_0 - H_1)(X_0 - X_1)] - H_1X_1\right\} + z^{-2}H_1X_1$$

$$Y_1 = \frac{1}{2}[(H_0 + H_1)(X_0 + X_1) - (H_0 - H_1)(X_0 - X_1)] + z^{-3}H_2X_2$$

$$Y_2 = H_1X_1 + \{(H_0 + H_2)(X_0 + X_2) - \{(H_0 + H_1)(X_0 + X_1) - \frac{1}{2} \times [(H_0 + H_1)(X_0 + X_1) - (H_0 - H_1)(X_0 - X_1)] - H_1X_1\} - H_2X_2\}$$

(9)

Comparing with the existing FFA three-parallel FIR filter structure, the proposed structure leads to two more sub filter blocks, which contain symmetric coefficients. Hence for an N-tap three-parallel FIR filter , the proposed structure can save N/3 multipliers from the existing FFA structure.

V. PROPOSED CASCADING SCHME FOR FFA

In proposed cascading process, instead of applying the existing small-sized structured FFA's to every stage, interleaving of multiple various small-sized structures can be done to fully exploit the symmetry of coefficients. The cascading of FFA's is a straight-forward application. For example, a (m x m) FFA can be cascaded with a (n x n) FFA to produce (m x n) parallel filtering structure. The resulting filters will be of length $N/(m\,x\,n)$. During the cascading of the FFA's, it is important to keep track of both the number of multipliers and the number of adders required for the filtering structure.

MATHEMATICAL FORMULAE

The required number of multipliers for a L-parallel filter with symmetric coefficients of odd length N can be estimated by (11) and (12) as,

Case 1:

When $\frac{N}{\prod_{i=1}^{r} L_i}$ is even.

$$M = \frac{N}{\prod_{i=1}^{r} L_i}\left(\prod_{i=1}^{r} M_i - \frac{S}{2}\right). \quad (10)$$

Case 2:

When $\frac{N}{\prod_{i=1}^{r} L_i}$ is odd.

$$M = \frac{N}{\prod_{i=1}^{r} L_i}\prod_{i=1}^{r} M_i - \frac{S}{2}\left(\frac{N}{\prod_{i=1}^{r} L_i} - 1\right). \quad (11)$$

Li , is the small parallel block size such as (2 x 2) or (3 x 3) FFA.

r, is the number of FFAs used. Mr, is the number of sub filter blocks resulted from i-th FFA. S is the number of sub filter blocks containing symmetric coefficients. The number of the required adders in sub filter section can be given by

$$A_{sub} = \prod_{i=1}^{r} M_i \left(\frac{N}{\prod_{i=1}^{r} L_i} - 1\right). \quad (12)$$

A comparison between the proposed and the existing FFA structures for even symmetric coefficients with different length under different level of parallelism

VI. CONCLUSION

This paper has presented the new parallel linear-phase FIR structures which are highly beneficial to the symmetric convolutions of length. Multipliers play a major role in terms of area and power consumption in FIR implementation. Since multipliers out weight adders in hardware cost, it is economical to replace multipliers with adders. The proposed new parallel filter blocks exploit the nature of symmetric coefficients and further reduce the amount of multipliers with adders. However, the numbers of reduced multipliers increases along with the length of FIR filter whereas the number adders remain still. The Pipelining and parallel processing is including in this Paper.

VII. ACKNOWLEDGMENTS

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