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Low Power and Area Single Edge Trigger D Flip Flop for Battery Operated Devices

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Abstract - The devices such as laptop, mobile phones and personal digital assistants (PDA) require low power VLSI devices because these devices are operated on battery. The mobile devices require high speed and low power consumption for their long battery life. So power delay product plays vital role in designing of VLSI circuits. Flip flops are one of the most complex and power consuming component among the various building blocks in digital designs. Clocking network and flip flops consume about 30 to 70 % of total power in the system out of which 90 % is consumed by flip flop. So in this paper the designing of low power and area single edge triggered D flip flop is shown . This flip flop has reduce area and we are designing it by using various nanometer technologies.

Keywords - SET D flip flop, VLSI, lamada rule, single edge trigger, nanometer technology, clocking network, power dissipation and power budget.

INTRODUCTION

Flip-flops are the basic building block of the sequential circuits. They are used to store data, processed by combinational circuit and synchronization of operation at a given clock frequency. The flip flops are basic building block of the digital electronics systems used in computers and many other types of systems. Level trigger flip flop is also known as latch and this latch is mainly used as storage element. Other type of flip-flop is edge trigger. Flip-flop is edge trigger means their output changes at the rising or falling edge of clock (at positive or negative edge). Flip-Flop is an electronic circuit that stores the logical state of one or more data input signal with respect to edge of clock. They are also used in computational circuits to operate in selected sequences during recurring clock intervals to receive and maintain data for a short time period so that other circuits within a system can further process data. Data is stored in flip-flop at each rising and falling edge of clock signal so that it can be applied as inputs to other combinational or sequential circuits, the flip-flops that store data on rising or falling edge of clock are known as single edge triggered flip flops and the flip-flops that store data on both the rising and falling edge of a clock are called as double edge triggered flip-flops.

In many digital very large scale integration (VLSI) designs, the clock system there is clock distribution network and flip-flop, the flip flop is one of the most power consuming component. It approximately consume 30 to 70 % of the total system power, where 90 % of which is consumed by the flip-flops and the last branches of the clock distribution network that is driving the flip-flop . With the recent trend in frequency scaling and deep pipelining, this clocking system power is the major component in total power dissipation. For portable digital circuit the power budget is strictly limited, it is important to minimize the power consumption in both clock distribution networks and flip-flops. At high frequency operation in the timing budget, the latency of the flip-flops should be minimum. In modern VLSI technology it is necessary to reduce both power consumption and latency . The dual-edge triggering also reduce the power consumption in the clock distribution network but it increases complexity of the design and complexity of clock distribution network.

SET D FLIP FLOP DESIGN

Conventional 16-transistor SET D flip-flop operates either at positive edge or negative edge of the clock. For the proper operation of the flip-flop, the input value should be constant just before setup time (t_{setup}) and just after hold time (t_{hold}) of the triggering edge of the clock. The circuit in the fig.1. shows the conventional 16-transistor SET D flip-flop. This conventional SET D flip flop consist of master and slave section. The dashed vertical line separate master and slave sections . A PMOS transistor which is present in the feedback path as it leads to a more compact layout than using a NMOS transistor. The pass transistors can be replaced with transmission gates in high noise environment.

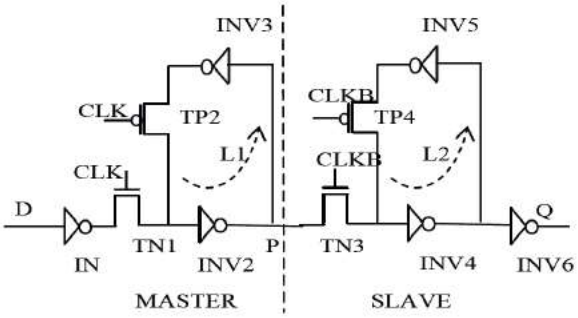

Figure 1) Conventional 16 transistor SET D flip flop

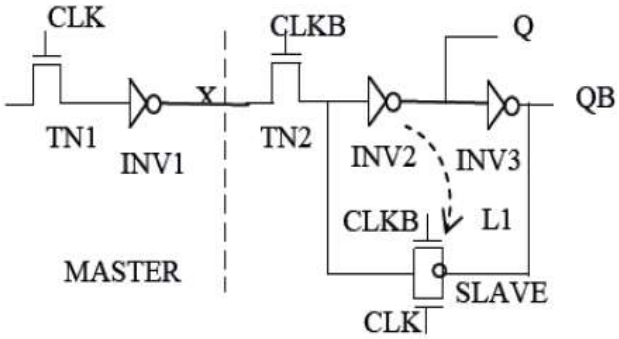

Figure 2) SET D flip flop using 10 transistor

The design of 10-transistor negative edge triggered SET D flip-flop is shown in fig.2. Here the feedback circuit of the master section is removed and in slave section feedback circuit consists of transmission gate. When clock is high , master latch is enable and the inverse of the data is stored to an intermediate node X. When the clock become LOW, the slave latch consisting of transistor TN2 and regenerative feedback circuit L1 becomes enable and produces data at the output Q and QB.

LAYOUT DESIGN OF SET D FLIP FLOP

To manufacture the physical mask layout of any circuit using a particular process it must follow some set of geometric constraints or rules, which are known as layout design rules. These layout design rules specify the minimum value of line widths for physical objects on-chip such as metal and poly-silicon interconnects or diffusion areas, minimum value of metal layer dimensions, and minimum value of separations between two such metal layer. If a metal line width is made too small then it is possible for the line to break during the fabrication process which result in an open circuit. When two lines are placed too close to each other in the layout then there may be formation of an unwanted short circuit by combining during or after the fabrication process.

The main objective of design rules is to achieve a high yield and reliability while using the smallest possible silicon area, to design any circuit with a particular technology. But there is a trade-off between higher yield which is obtained through conservative geometries and greater area efficiency, which is obtained through aggressive, high- density placement of various features on the chip.
In general the layout design rules notably increases the probability of fabricating a successful product with high yield.
The design rules are generally described in two ways
• Micron rules, in which the layout constraints such as minimum feature sizes and minimum allowable feature separations, are describe in terms of absolute dimensions in micrometers, or
• lambda rules, which specify the layout rules in terms of a single parameter (λ) and thus allow linear, proportional scaling of all geometrical constraints.

Lambda based layout design rules were originally designed to simplify the industry standard micron based design rules and to allow scaling capability for various technologies. It must be emphasized however that most of the submicron CMOS process design rules do not lend themselves to straightforward linear scaling. Therefore the use of lambda based design rules must be handled with caution in sub-micron geometries.

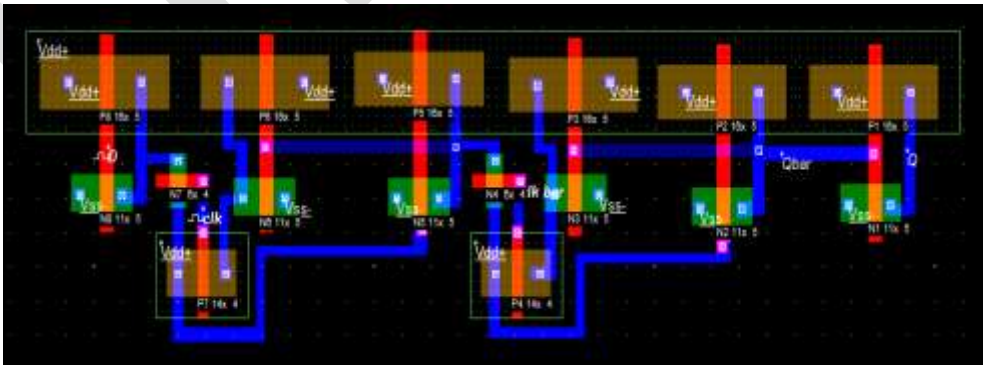

Figure 3) Layout design of conventional SET D flips flop

Device	Width	Length	Device	Width	Length
N1	11λ	5 λ	P1	16 λ	5 λ
N2	11 λ	5 λ	P2	16 λ	5 λ
N3	11 λ	5 λ	P3	16 λ	5 λ
N4	6 λ	4 λ	P4	14 λ	4 λ
N5	11 λ	5 λ	P5	16 λ	5 λ
N6	11 λ	5 λ	P6	16 λ	5 λ
N7	6 λ	4 λ	P7	14 λ	4 λ
N8	11 λ	5 λ	P8	16 λ	5 λ

Table 1) MOS size in conventional SET D flips flop

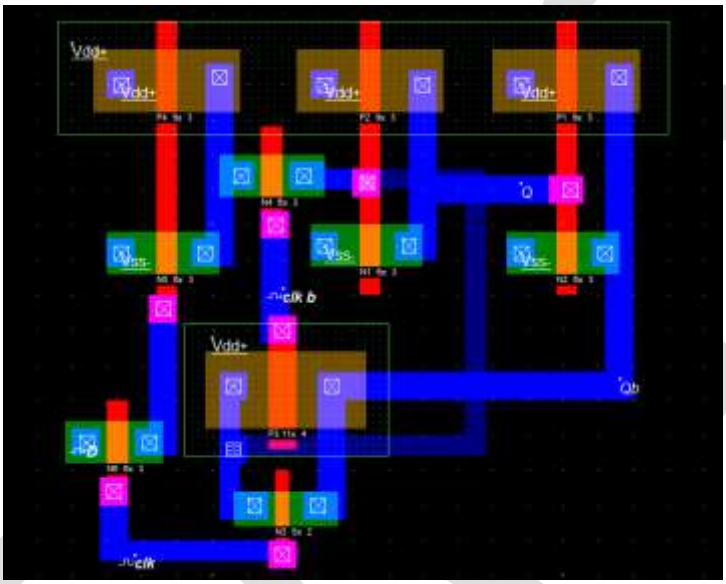

Figure 4) Layout design of ten transistors SET D flip flop

Device	Width	Length	Device	Width	Length
N1	6λ	3 λ	P1	9 λ	3 λ
N2	6 λ	3 λ	P2	9 λ	4 λ
N3	5 λ	2 λ	P3	11 λ	4 λ
N4	6 λ	3 λ	P4	9 λ	3λ
N5	6 λ	3 λ			
N6	6λ	3 λ			

Table 2) MOS size in ten transistors SET D flips flop

The value of lamada is changed with respect to nanometer technology. In 45 nm technology the value of lamada is 0.025 µm and in 32 nm its value is 0.015 µm. The fig.3. Shows the layout of conventional 16 transistors SET D flip flop with combine well. This Conventional 16- transistor SET D flip-flop operates at falling edge of the clock. For the proper operation of the flip-flop, the input value should be constant just before setup time (t_{setup}) and just after hold time (t_{hold}) of triggering edge of the clock. In this design PMOS P1,P2,P3,P5,P6 and P8 are provided with combine N well. The size of each MOS device is shown in table 1.
The fig.4. shows the layout of ten transistors SET D flip flop . In this design the feedback circuit of the master section is removed and in slave section feedback loop consists of transmission gate. In this design PMOS P1,P2 and P4 are provided . The size of each MOS device is shown in table 2.

SIMULATION

The above two layout designs are simulated using Microwind 3.5 tool in 45 nm and 32 nm process. The fig.5 shows the waveform of conventional 16 transistors SET D flip flop in 45 nm technology. The clock frequency is 1.08 GHz and for this frequency the power dissipation is 1.285 µW and maximum clock to Q rise time is 302 psec and fall time is 103 psec.

Figure 5) Waveform of conventional SET D flip flop

The fig.6 shows the waveform of ten transistors SET D flip flop in 45 nm technology. The clock frequency is 1.08 GHz and for this frequency the power dissipation is 4.644 µW and maximum clock to Q rise time is 82 psec and fall time is 83 psec.

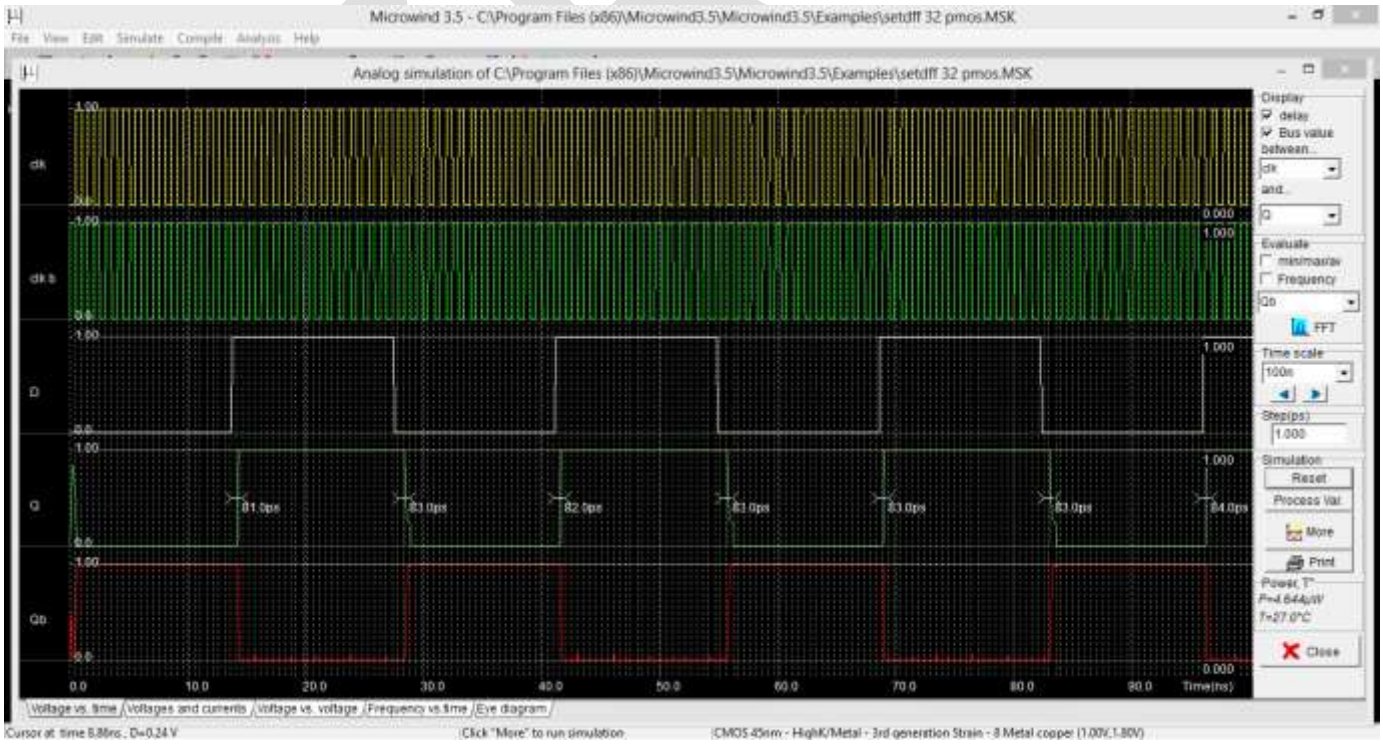

Figure 6) Waveform of ten transistors SET D flip flop

RESULT

As compared to conventional 16 transistors SET D flip flop area taken by ten transistors SET D flip flop is lowest in 32 nanometer technology than 45 nm technology but power consumed by conventional 16 transistors SET D flip flop is lowest in 32 nm technology than ten transistors SET D flip flop.

Design	45 nm	32 nm
Conventional 16 transistors SET D FF	12.1μm^2	9.8 μm^2
Ten transistors SET D FF	2.7 μm^2	2.2 μm^2

Table 3) Comparison of area

Design	45 nm	32 nm
Conventional 16 transistors SET D FF	1.282µW	1.266µW
Ten transistors SET D FF	4.644 µW	3.108 µW

Table 4) Comparison of power

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CONCLUSION

In low power applications , area and power consumption by the device are the main technological aspects to select a design over the other counterpart designs. The ten transistors SET D flip-flop shows better performance in terms of area and power dissipation over other design. This design is tested in 45nm and 32nm technology, thus it is also technology independent. The ten transistors SET D flip flop is used where the area requirement is minimum.

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