Energy Efficient and High Speed Domino Logic Circuit Design Techniques: An Overview

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Abstract: This paper discusses the various design techniques of Energy efficient and High Speed Domino Logic circuit design. Dynamic logic style is used in high speed and energy efficient circuit design because it uses the less number of transistor and fast speed in comparison to CMOS logic circuit design. Domino logic circuit design is less noise tolerant because of and they are not widely used in all types of the circuit design.

Keywords Domino Logic, Dynamic Logic, Noise Tolerance.

Introduction

This contains a dynamic logic block of NMOS. The dynamic logic block is followed by the static inverter which makes a basic domino logic circuit. This works in precharge phase and evaluation phase. During the precharge phase the output of the dynamic block is charged up to VDD and during the evaluation phase, the dynamic gate conditionally discharges.

The introduction of static inverter has the additional advantage that fan-out of gate is driven by static inverter with low impedance output which increases noise immunity. Also it reduces the capacitance of dynamic output node. Since each dynamic gate has static inverter, only non-inverting logic can be implemented. This is a major limiting while implementing the wide fan in logic gates using the dynamic logic technology, there are certain disadvantages like

Dynamic Node high capacitance, leakage current in evaluation phase. Therefore to overcome the disadvantages much logic were designed. And maximum of domino logic have some demerits. This work compares all the design of Domino logic circuit design.

Domino Logic Design Techniques

Conventional domino logic circuits such as footless and footed domino logic circuit are reviewed along with other designed schemes. These circuits includes the basic footless domino logic ,footed domino logic(FDL)[1], keeper domino logic(KDL), high speed domino logic(HSDL) . Main aim of these circuits is to improve the

circuit performance having wide fan in [2]. Using a keeper transistor helps to address the problems of leakage and charge sharing but increases power dissipation. So sizing the keeper transistor helps to overcome the problem but then tradeoff occurs between reliability and performance.

A. Footless domino logic (FLDL):

Footless domino logic circuit is a standard domino logic circuit shown in fig.1. employing a PMOS keeper transistor to reduce charge sharing problem.
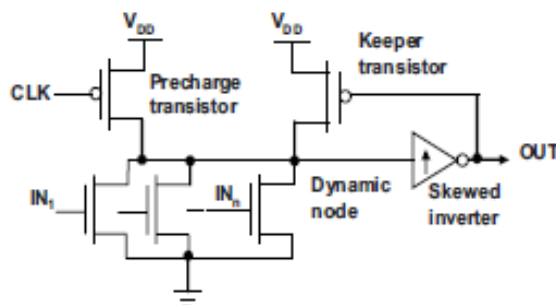

Fig 1: Footless Domino Logic [3]

B. Footed domino logic (FDL):

FDL is shown in fig.2. Here a footer NMOS transistor is employed to reduce the leakage current. During the precharge phase as clock is low, PMOS transistor PMOS_1 turns ON and output node precharges to vdd. During the evaluation phase clock is high which turns off PMOS transistor and switches on the footer transistor N_1. Now, depending upon the evaluation network, output swiches to low or high. This technique reduces power consumption but at the same time increases delay.
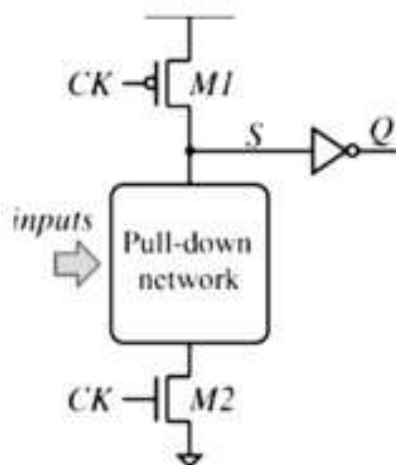

Fig 2: Footed Domino Logic [4]

C. Keeper domino logic (KDL):

Perhaps the simplest way to enhance the noise tolerance of dynamic CMOS logic gates is to employ a weak transistor, known as keeper, at the dynamic node as shown in Fig. 3.The keeper transistor provides a strong '1'

to the dynamic node so that the stored charge of the dynamic node is maintained. In the original dynamic logic network [5], the gate of the PMOS keeper is tied to the ground, as shown in Fig. 3.
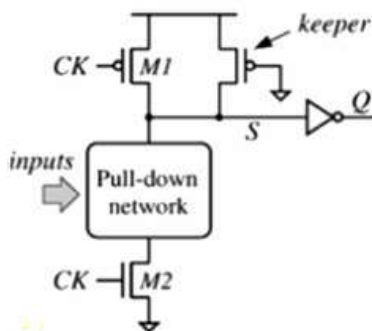

Fig 3: Keeper Domino Logic [5]

D. High Speed Domino Logic

The circuit of the HS Domino logic is shown in Fig.4 [6]. In HS domino the keeper transistor is driven by a combination of the output node and a delayed clock. The circuit works as follows: At the start of the evaluation phase, when clock is high, MP3 turns on and then the keeper transistor MP2 turns OFF. In this way, the contention between evaluation network and keeper transistor is reduced by turning off the keeper transistor at the beginning of evaluation mode. After the delay equals the delay of two inverters, transistor MP3 turns off. At this moment, if the dynamic node has been discharged to [7] ground, i.e. if any input goes high, the nMOS transistor MN1 remains OFF. Thus the voltage at the gate of the keeper goes to VDD-Vth and not VDD causing higher leakage current though the keeper transistor [7]. On the other hand, if the dynamic node remains high during the evaluation phase (all inputs at 0, standby mode); MN1 turns on and pulls the gate of the keeper transistor. Thus keeper transistor will turn on to keep the dynamic node high, fighting the effects of leakage.
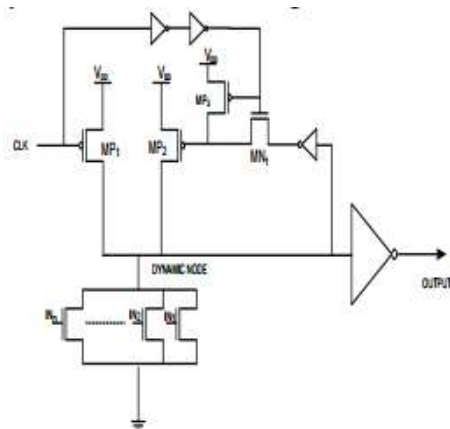

Fig 4: High Speed Domino Logic [7]

Conclusion

In this paper several Domino logic design has been compared. All design is compared in terms of their area, speed and noise immunity. Use of keeper transistor and its drawbacks also discussed. Therefore the all the circuits are design to evaluate the logic in evaluation phase by discharging the dynamic node conditionally.

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