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Design and Analysis of Linear Voltage to current converters using CMOS Technology

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ABSTRACT- Voltage to current converters or TRANSCONDUCTANCE amplifiers, find its applications in both traditional analog ICs e.g. amplifier and filters as well as current analog VLSI e.g. Field programmable analog arrays and various other neural networks. A complete review of different linear V-I converter has been done in this paper. Since the basic V-I convertor circuit uses common source differential pair which shows the nonlinearity effect due to the differential input voltage signal. The different circuits like Linear composite MOSFET TRANSCONDUCTOR, linear V-I convertor including feedback network which are designed to overcome the problem of non linearity has been studied. The basic V-I Converter using source coupled differential pair was synthesized and simulated using Mentorgraphics, Pyxis Schematic and ELDO respectively using 0.25 nm technology.

1.1 INTRODUCTION

In the past decade the CMOS technology has played a major role in rapid expansion and the increased assimilation of very large scale integration (VLSI) system. They are widely used transistor in both digital and analog circuits, and it is the backbone of modern electronics because they offers high input impedance, less power dissipation, small size, less switching power consumption and they are easily scalable. Scaling down the transistors lead to increased integrated circuit components which reduces the cost of the device being manufactured. Moreover the smaller geometry leads to less parasitic capacitance, higher operating speed and lower power consumption .As we reduce the size of transistor not only the channel length and width but also the gate oxide thickness which can lead to transistor breakdown so in order to prevent this the power supply is to be reduced. Linear voltage to current convertor is one of the basic building block as well as interface element in analog circuits. So it is of importance that this interface element should offer a high linear range so that the system can work properly. In addition, V-I converters are useful sub circuits in sensor interface circuits for biomedical applications. Although

the drain current in the transistor are the non linear function of input voltage so in order to achieve the linearity the simplest and the most widely used TRANSCONDUCTOR is the source coupled differential pair as they are less sensitive to the noise and interference using MOSFET. It is assumed that M1 and M2 as shown in **fig 1** must be matched pair and both operate in saturation. Furthermore, the channel length modulation effect is ignored and it is presumed that the drain current of each device follows the simple square law current equation with α=1.So the drain current equation for common source differential pair are

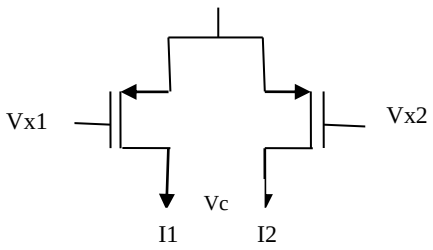

Fig 1:- schematic of the common source differential pair

$$I_1 = \frac{Kp}{2}(V_{x1} - V_{tp} - V_c)^2 \quad \text{--- (1)}$$

$$I_2 = \frac{Kp}{2}(V_{x2} - V_{tp} - V_c)^2 \quad \text{--- (2)}$$

where $Kp = \mu CoxW/L$ and V_{tp} is the threshold voltage of pmos transistor.

Hence differential output current is given as

$$I_1 - I_2 = \frac{K_p}{2}(V_{x1} - V_{x2})(V_{x1} + V_{x2} - 2V_c - 2V_{tp}) \quad \text{--- (3)}$$

1.2 SIMPLE LINEAR VOLTAGE TO CURRENT CONVERTOR

In order to design simple linear voltage to current convertor the source coupled differential pair is being used. This V-I convertor is able to handle the large signals. In order to improve the linearity of differential pair the body effect is being exploited here .If the body effect of PMOS transistor of common source differential air is included than differential output current is given as $I_1 - I_{2=}\frac{K_p}{2\alpha_p}(V_{x1} - V_{x2})V_x$

where $V_x = (V_{x1} + V_{x2} - 2V_c - 2V_{tp})$ --- (1)

According to the above relation if V_x is constant then linear relation between the $V_{x1} - V_{x2}$ and $I_1 - I_2$ can be achieved. It can be achieved by using simple NMOS differential attenuator as shown in figure 2; composed of M1-M5 so that there differential outputs can be used as input to the PMOS differential pair . Where M1-M2 and M3-M4 are matched transistors and M5 act as a current sink being biased by V_{b1}.The variations produced due to body effect in the threshold voltage of M3 and M4 are being characterized over hereby using equation:

$$V_{tn(Vsb)} = V_{tno} + (\alpha_n - 1)\, V_{sb}$$

Applying the KCL equations at nodes V_{x1} and V_{x2} we obtain

$$\frac{k_u}{2\alpha_n}(V_{DD} - V_{x1} - V_{tn}(V_{x1} - V_{ss}))^2 = \frac{k_d}{2\alpha_n}(V_{GS1} - V_{Tno})^2 \quad \text{--- (2)}$$

where $V_G = V_{DD} - V_{x1}$ and $V_S = V_{x1} - V_{ss}$

$$\frac{k_u}{2\alpha_n}(V_{DD} - V_{x2} - V_{tn}(V_{x2} - V_{ss}))^2 = \frac{k_d}{2\alpha_n}(V_{GS2} - V_{Tno})^2 \quad \text{--- (3)}$$

In the above equations $V_{GS1}$and V_{GS2} are the gate–source voltages of M1 and M2. Now by substituting the value of V_{Tno} in the above equation V_{x1} and V_{x2} are given as

$$V_{x1} = \frac{1}{\alpha_n}[V_{DD} + (\alpha_n - 1)V_{ss} - V_{Tno} - \sqrt{\frac{K_d}{K_u}}(V_{GS1} - V_{Tno}) \quad \text{--- (4)}$$

$$V_{x2} = \frac{1}{\alpha_n}[V_{DD} + (\alpha_n - 1)V_{ss} - V_{Tno} - \sqrt{\frac{K_d}{K_u}}(V_{GS2} - V_{Tno}) \quad \text{--- (5)}$$

Since $V_d = V_1 - V_2 = V_{GS1} - V_{GS2}$

$$= V_{GS1} + V_{GS2} = 2V_{Tno} + \sqrt{-V_d{}^2 + \frac{4\alpha_n I}{K_d}} \quad \text{--- (6)}$$

So $V_{x1} - V_{x2} = \frac{1}{\alpha_n}\sqrt{\frac{K_d}{K_u}}V_D$ and

$$V_{x1} + V_{x2} = \frac{2}{\alpha_n}[V_{DD} + (\alpha_n - 1)V_{ss} - V_{Tno}] - \frac{1}{\alpha_n}\sqrt{\frac{K_d}{K_u}}\sqrt{-V_d{}^2 + \frac{4\alpha_n I}{K_d}} \quad \text{--- (7)}$$

$$I_d = I_1 - I_{2=} \frac{k_p}{2\alpha_n\alpha_p}\sqrt{\frac{K_d}{K_u}}\{2V_C + 2V_{TP} - \frac{2}{\alpha_n}[V_{DD} + (\alpha_n - 1)V_{ss} - V_{Tno}] + \frac{1}{\alpha_n}\sqrt{\frac{K_d}{K_u}}\sqrt{-V_d{}^2 + \frac{4\alpha_n I}{K_d}}$$

$\}V_d$ --- (**8**)

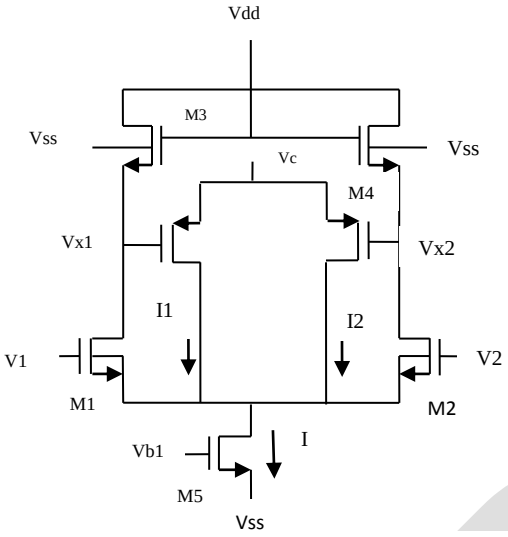

Fig 2 :- Schematic of the V-I convertor using source coupled differential pair

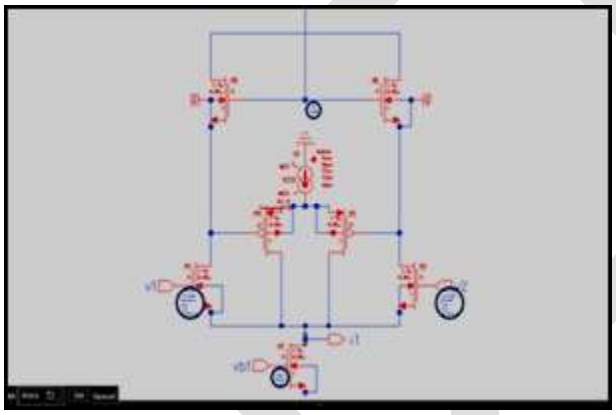

Fig 3:- Schematic of V-I convertor

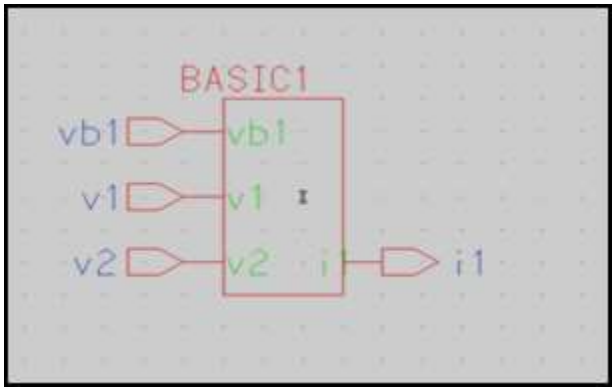

Fig 4:-Symbol of V-I convertor

$$I_d = \frac{k_p}{2\alpha_n\alpha_p}\sqrt{\frac{K_d}{K_u}}(V_K + \Delta V)V_d \qquad \text{--- (9)}$$

Where $V_K = 2V_C + 2V_{TP} - \frac{2}{\alpha_n}[V_{DD} + (\alpha_n - 1)V_{ss} - V_{Tno}]$

$$\Delta V = \frac{1}{\alpha_n}\sqrt{\frac{K_d}{K_u}}\sqrt{-{V_d}^2 + \frac{4\alpha_n I}{K_d}}$$

this ΔV shows the nonlinearity effect in a simple differential pair biased by a constant current source .So in order to reduce the nonlinearity effect we have to selected small K_d/K_u ratio and $\alpha_n > 1$ which is not always possible . In order to achieve more linear VI relation in VI convertor we use the composite MOSFET TRANSCONDUCTORS in the convertors circuit.

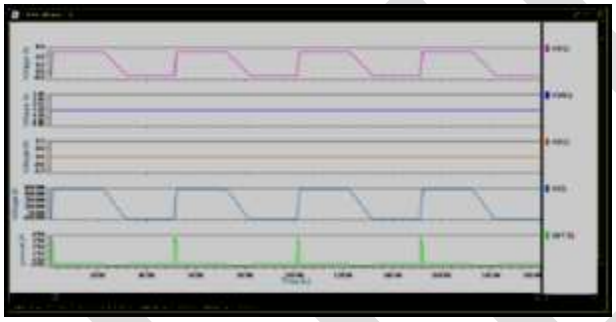

Fig 6 :-Input and output waveforms of V-I convertor.

1.3 LINEAR COMPOSITE MOSFET TRANSCONDUCTOR BASED VI CONVERTOR

In the linear composite MOSFET cell both the transistor M1 and M3 the voltage follower configuration and linear NMOS VI convertor can be realized by cross coupling the two basic composite cells. In this the linear relation between the voltage and current is being achieved if and only if $2V_x = V_{in} + V_c$ where V_c is constant voltage. In this body effect is not been taken into account so the difference in the drain current is being calculated by using α=1 which is given as

$$I_{d1} - I_{d2} = \frac{K_n}{2}(V_c - V_{ss})(V_{in} - V_c - 2V_{tn}) \text{ --- (1)}$$

And the resultant equation shows the differential current and the input voltage V_{in} have the linear relation but with a dc offset voltage. The differential current equation is given as

$$I_1 - I_2 = (I_{d1} - I_{d2}) - (I_{d3} - I_{d4})$$

$$= \frac{K_n}{2}(V_c - V_{ss})(V_1 - V_c - 2V_{tn}) - \frac{K_n}{2}(V_c - V_{ss})(V_2 - V_c - 2V_{tn})$$

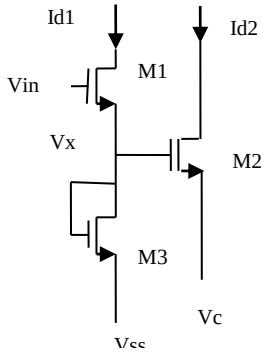

Fig 7:-shows the voltage follower configuration.

$= \frac{K_n}{2}(V_c - V_{ss})(V_1 - V_2)$

$= g_m(V_1 - V_2)$ where $g_m = \frac{K_n}{2}(V_c - V_{ss})$ --- (**2**)

This linear VI convertor has constant g_m which can be electrically tuned by V_c . This circuit also have a disadvantage that the linear input range is limited by the condition that $V_{ss} + 2V_{Tn} < V_{12}$ .In order to turn the transistors M1, M3, M4 and M5.

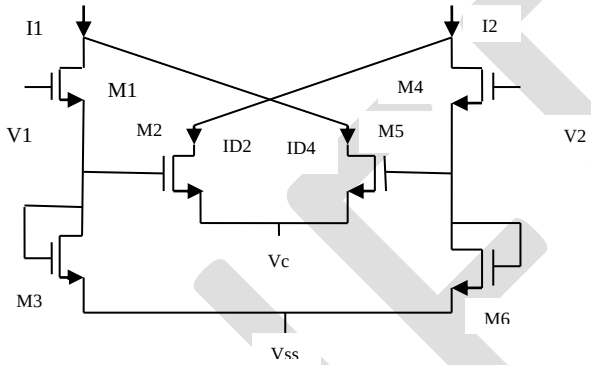

Fig 8:-Schematic of Composite NMOS V-I convertor.

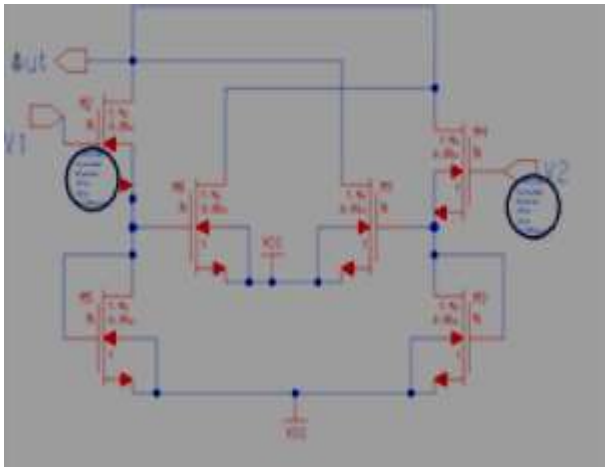

FIG 9:- SCHEMATIC OF COMPOSITE NMOS V-I CONVERTOR.

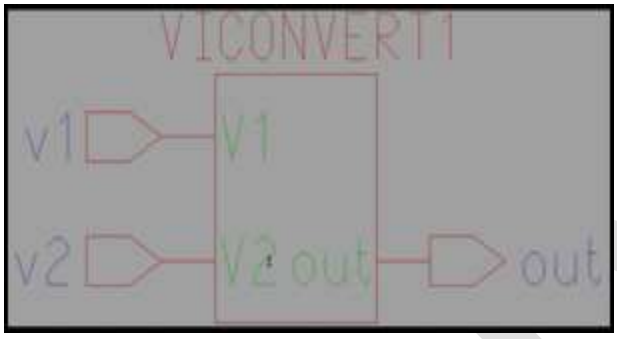

Fig 10:- Symbol of V-I convertor.

1.4 LINEAR VOLTAGE TO CURRENT CONVERTOR INCLUDING FEEDBACK NETWORK

This voltage to current convertor includes three field effect transistors in which the sources are being electrically connected to define a common source node and a feedback network. This voltage to current convertor is capable of receiving both balanced and unbalanced inputs. Fig consist of transistors M1, M2, M3 which are connected at the source to define a common source node. The first balanced voltage input is connected to the gate of M1 and second to M2.The feedback network is connected to the drain of M3 and the common source node .The loop gain and bandwidth of the feedback network determines the convertors accuracy and speed. This feedback network includes M4 which is arranged as a common drain follower with its gate connected to the drain of M3.It also consist of bipolar transistors Q1 and Q2 .The collector of Q1 is connected to the both source of M4 and its own base .Thus the collector of Q2 is connected to the common source node and the base of it is connected to the base of Q1.Emitter of the both bipolar transistor are connected to each other. It also consist of transistors M5 and M6.The drain of the M5 andM3 are connected to each other.M6 is connected as the current mirror with M5.Finally the reference voltage Vdd is connected to the drain of the M4 and the source of the M5 and M6.

The operation of the circuit is described as follow: The transistor M1-M6 operate in the saturation region and bipolar transistor Q1-Q2 operates in active region. Assume Ic is fixed reference current and Vc=0. Initially the current through the transistors M1and M2 is Ic. As the input voltage V1 varies the source terminals of transistor M1, M2 and M3 follows accordingly. The current through M3-M5 are constant, therefore any change in differential inputs V1,V2 is amplified common gate transistor M3 and the result is fed back by M4,Q1and Q2 in order to adjust the current through Q2.as long as the bipolar transistors Q1 and Q2 operate in active region and the MOS transistors M3 and M5 operate in saturation region.Assume MOS transistors M1 and M2 are matched and are operating in the saturation region. The transistor gain current may be characterized

by using the square law drain current expression

$$I_d = K_n(V_{gs} - V_{Tn})^2/2 \qquad \text{--- (1)}$$

where $K_n = \mu eff C_{ox}$W/L assuming $V_{T1} = V_{T2} = V_{T3}$ the dc transfer equations of the voltage to current convertor is:

$$V_1 - V_c = V_{gs1} - V_{gs3} = \sqrt{\frac{2I_1}{K_1}} - \sqrt{\frac{2I_c}{K_3}}$$

$$= V_{gs3} - V_{gs2} = \sqrt{\frac{2I_c}{K_3}} - \sqrt{\frac{2I_2}{K_1}} \quad \text{--- (2)}$$

Vdd

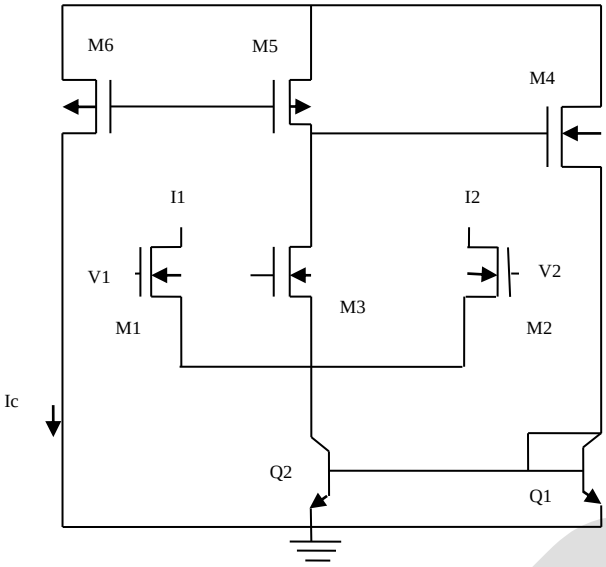

FIG 11:- SCHEMATIC OF THE LINEAR VOLTAGE TO CURRENT CONVERTOR INCLUDING FEEDBACK

$$I_1 = \frac{K_1(V_1 - V_c)^2}{2} + \frac{K_1 I_c}{K_3} + \sqrt{\frac{2I_c}{K_3}} K_1(V_1 - V_c) \quad \text{--- (3)}$$

$$I_2 = \frac{K_2(V_1 + V_c)^2}{2} + \frac{K_2 I_c}{K_3} + \sqrt{\frac{2I_c}{K_3}} K_2(V_1 + V_c) \quad \text{--- (4)}$$

Assuming $K_1 = K_2 = K$ and V2= -V1

The expression for the differential output current is IOUT $= I_1 - I_2 = 2V_1 k\left(\sqrt{\frac{2I_c}{K_3}} - V_c\right)$ --- (5)

If $V_c = 0$ *then* $I_1 - I_2 = 2V_1 k\left(\sqrt{\frac{2I_c}{K_3}}\right)$

thus the reference voltage I_c may be used to control the transconductance. If I_c is fixed then V_c control the TRANSCONDUCTANCE. The linear range of the circuit extends to the values of Vc which provide linear differential output current. The input range limit for VBE1max =VBE2max

$$|V1| \leq \sqrt{\frac{K_{n4}{V_x}^2 - 6I_c + 4V_c\sqrt{2KI_c} - 2K{V_c}^2}{2K}} \quad \text{--- (6)}$$

Where

$$V_x = V_{DD} - V_{t4} - V_{BE1max} - \sqrt{\frac{2I_c}{K_{ps}}} - V_{ss}$$

In Equation (6) it is assumes that the circuit behaves nonlinearly when any MOS device M1-M6 begins to operate outside the saturation region. The linear range is maximized by choosing a large value for K4 and large emitter areas for Q1 and Q2 and small values for Ic and K1.Equation 3 and 4 shows that any mismatch between M1 and M2 results in second order harmonic distortion.
Any mismatch between [M1, M2] and M3 results in DC offset, which can lower the maximum input range.

In an alternative method of using the V-I convertor , the voltage Vc is held to a constant voltage to allow the current source Ic to control the circuit's TRANSCONDUCTANCE. In addition, the TRANSCONDUCTANCE of the circuit may also be controlled by simultaneously varying both the voltage V0 and the current source Ic. Whether varying Ic alone with Vc fixed, varying Vc alone with Ic fixed, or varying both Ic and Vc to control the circuit's TRANSCONDUCTANCE, linearity can be maintained. The converter of FIG. 6 produces good linearity, for example Total Harmonic Distortion 1.3% for 4 Vp-p inputs and 8V supply voltage, and good TRANSCONDUCTANCE tuning range.

In order to achieve the linearity between the voltage and current for unbalanced inputs two voltage to current convertors as discussed previously are connected in parallel to each other. The two convertors of figure are connected by coupling the reference voltages of a first and second voltage to current convertor in parallel. In this the first FET M3a and the second FET M2a have their source connected to define a first common source node similarly M1a and M3b forms the second common source node. The V1a is applied to gates of M3a- M1a and V2a is applied to gates of M2a- M3b. In this the two feedback networks are being used. The current source Ic operates to control the convertors TRANSCONDUCTANCE. In this the control voltage Vc has been eliminated which was being used for the balanced input convertor.The linear DC large signal transfer function of this circuit does not rely on the balanced inputs .Assuming the matched transistors operating in the saturation region (K1=K2=K3=K4=K) ,The dc transfer function is

$$I_1 = \frac{K(V_1-V_2)^2}{2} + I_c + \sqrt{2I_cK}(V_1 - V_2) \qquad \text{--- (6)}$$

$$I_2 = \frac{K(V_1-V_2)^2}{2} + I_c - \sqrt{2I_cK}(V_1 - V_2) \qquad \text{--- (7)}$$

$$\mathrm{I}_1 - I_2 = \sqrt{8I_cK}(V_1 - V_2) \qquad \text{--- (8)}$$

$$g_m = \frac{\mathrm{I}_1 - I_2}{V_1 - V_2} = \sqrt{8I_cK} \qquad \text{--- (9)}$$

Any mismatch between transistors M1a and M2a will degrade the TRANSCONDUCTOR linearity with mainly a second order harmonic distortion. The linear input range constraint of the converter of this circuit is

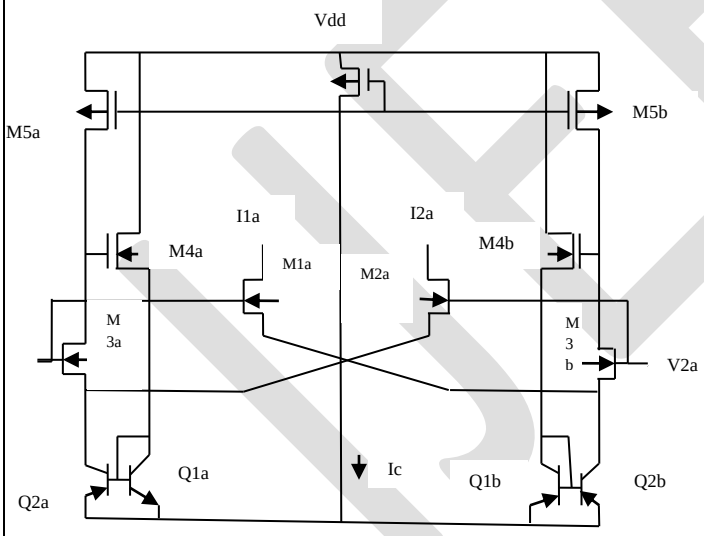

FIG 12:-SCHEMATIC OF LINEAR VOLTAGE TO CURRENT CONVERTOR INCLUDING FEEDBACK NETWORK FOR UNBALANCED INPUT

$$|V_1 - V_2| \leq$$

$$Min\ |[(\sqrt{\frac{2I_c}{K}} - \sqrt{\frac{K_{n4a}}{K}\left(V_{dd} - V_{4a} - V_{\boldsymbol{BE1amax}} - \sqrt{\frac{2I_c}{K_{p5a}}}\right)^2} - \frac{2I_c}{K})(\sqrt{\frac{2I_c}{K}} -$$

$$\sqrt{\frac{K_{n4b}}{K}\left(V_{dd} - V_{T4b} - V_{\boldsymbol{BE1bmax}} - \sqrt{\frac{2I_c}{K_{p5a}}}\right)^2} - \frac{2I_c}{K})$$

--- (**10**)

Equation is derived with no balanced input constraint.

CONCLUSION

In simple linear V-I convertor the non linearity effect has arise due to ΔV .In order to reduce the nonlinearity effect we have to selected small K_d/K_u ratio and $\alpha_n > 1$ which is not always possible .So In order to achieve more linearity in V-I convertor we use the composite MOSFET TRANSCONDUCTORS in the convertors circuit but this circuit also have a disadvantage that the linear input range is limited by the condition that $V_{ss} + 2V_{Tn} < V_{12}$ .So we have used V-I convertor using feedback network which is better than all others discussed above as it shows the large reduction in the non linearity effect .

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