International Journal of Engineering Research and General Science Volume 3, Issue 3, May-June, 2015
ISSN 2091-2730

Monte Carlo Based Single Electron Transistor Modelling of Decision Making Hardware Design and its Performance Analysis

Dr. Jayanta Gope[1], Mr. Anubhab Mandal[2], Mr. Sanjay Bhadra[3]

[1]Prof. ECE Dept. Camellia School of Engg & Tech., Barasat, Kolkata, jayantagope.etce.ju@gmail.com, +91 9831205967

Abstract— SET is predicted as meritoriously flourishing technology in contemporary electronics with modern physical effects of electron charge transport. It renders countless development in device integrity, robustness and depicts extreme low power consuming features. Most interestingly, the straightforward circuit construction validates single electron charging effects in the single electron box. It demonstrates all pros of large scale electronic circuits that consist in CMOS technology built ICs. Thus SET ushered new scopes in replacing age old CMOS. The authors here attempted in designing one decision making subsystem using SET technology. Further the proposed model was validated using SIMON simulation tool.

Keywords— CMOS, Single Electron Tunneling, Threshold Logic Gates, Tunnel Junction, Coulomb Blockade, SIMON, Decision Making Hardware.

INTRODUCTION

Incorporation of SET in logic realization is a comparatively new paradigm to ponder over. The topological formulations are comprised of tunneling phenomena and electron transport properties. With the realization of conventional logic devices of SET, new heights can be achieved in the field of post CMOS era; thereby the monolithic advancement of low power consuming, easy portable, economic and high speed device manufacturing is attained both in academia and industry. Many products are ready to hit the market in this decade. Research labs have been set up worldwide and Researchers have been receiving large funds to make the revolution happen in the very dawn [1-5].

This letter enumerates a structural modeling of SET based 'Decision Making' hardware to be implanted in modern era. Following sections briefly outlines the structure of an SET and its logical realizations. Subsequently few equations have been tabulated in designing the SET based decision making subsystem.

SINGLE ELECTRON TUNNELING PHENOMENA IN SETs

Conveniently, SET phenomena can be clarified by fig 1. The small metallic sphere in the fig.1 is primarily electro-neutral i.e. the total charge on this sphere is absolutely zero because of the equilibrium of same number of electrons and protons in it. In such if a single electron lies close to the sphere; the electron is dragged into the sphere. This single electron now leaves a negative charge of –e on the sphere. The manifestation of this negative charge creates an electric field round the sphere. Now if any other electron lies proximity to this sphere, it will be repulsed strongly by the electric field formed around the sphere.

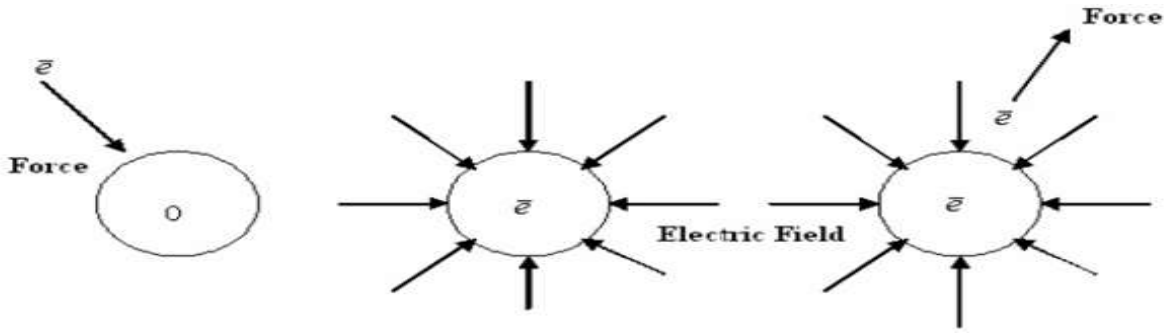

Fig.1: Hypothetical deliberation of SET phenomenon

SETs, like the FETs are three terminal switching devices having the effects of Coulomb Blockade. But unlike other FETs, a tunnel junction lies amid the source and drain. The tunnel junction can be thought similar to a metal granule and is made up of thin insulator of 1nm thickness. Electrons can tunnel into it through one side of the junction singly i.e., electrons can populate the granule one after one. Two tunnel junctions are capacitively coupled to form the simple SET circuit and most interestingly the capacitor is considered to be much thicker than that of the tunnel junction so that no electron can tunnel through it. The operational aspect of SETs are based on an intrinsically quantum phenomenon convincingly referred as "Tunnel effect" [6-14]. This is how the three terminal switching device, i.e., the SET can transfer electrons form source to drain one after one. The representation of SETs is drafted in fig. 2.

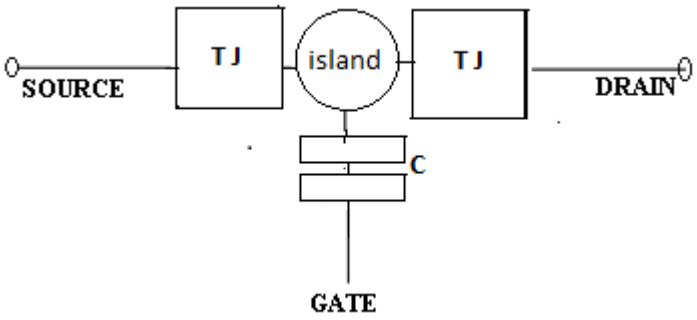

Fig 2: Simple SET prototype

Based on the simplistic nature of SET and its robustness, Scientists motivated themselves to realize SET based logical designs [15-21] to comply with the future logical elements. They mimic the CMOS logical realizations in the nano regime. Below are few SET based logic realizations of digital structures.

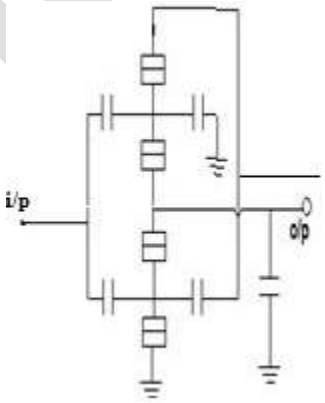

Fig.3: SET based NOT realization

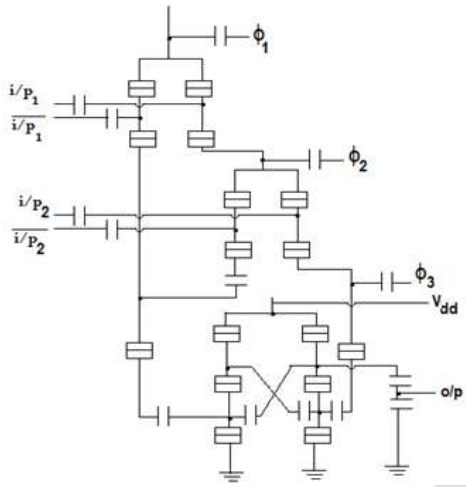

Fig.4: SET based AND realization

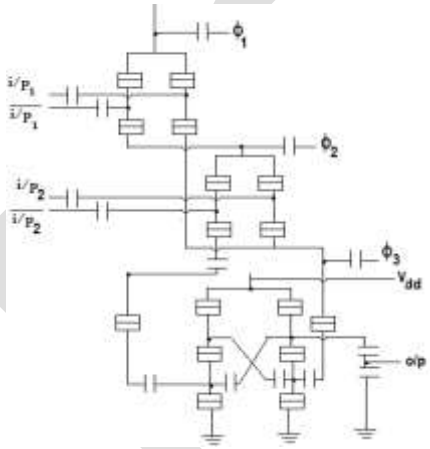

Fig.5: SET based OR realization

SET SIMULATION USING SIMON

SIMON, a Monte Carlo equation based SET simulator has introduced every possible answers on SET technology for a wide variety of important design questions. The virtue of SIMON is that it consists of a graphical user interface and graphical circuit editor that allow easy and error free usage. Different circuit elements like tunnel junctions, capacitors, voltage sources, and measuring devices for current, voltage, and charge, can be arbitrarily connected through nodes. Thus SIMON is a sophisticated multipurpose simulator for single-electron devices and circuits having numerous features of a graphical circuit editor embedded in a graphical user interface as well as the simulation of co-tunnel events and a single step interactive analyses mode is also made available for diagnosis. Convincingly, it supports energy dependent density of states and is able to calculate stability plots. This is a unique creation of eminent scientist Dr. Christoph Wasshuber [22-25]. Few noteworthy characteristics of SIMON are –

1. STABILITY PLOT

   - traditional stability plot with two voltages as x- and y-axis
   - one axis can be the temperature
   - one or both axis can be a capacitance or resistance
   - differentiation in x or y direction possible

2. NORMAL RESISTORS
   - normal resistors allow the modeling of more complex and realistic circuits

3. CURRENT SOURCES
    - current sources can be specified with a certain charge-granularity, which allows the modeling of electron injectors/pumps/turnstiles in a very easy manner
4. ENERGY DEPENDENT DENSITY OF STATES
    - The tunnel model has been improved by incorporating three kinds of density of states functions
        - constant with optional band gap (metallic)
        - square-root with band gap (semiconductor-like)
        - $x/(x^2-1)^{1/2}$ with band gap (superconductor-like)
    - Discrete energy levels are modeled as Gaussian functions, with mean, width, and height.

REAL TIME ANALYSIS OF SET AND GATE USING SIMON:

The SIMON simulated SET AND gate is shown in fig. 6 and it comprises of five islands $N_1 – N_5$ bounded by five tunnel junctions $J_1 – J_5$ and nine capacitors $C_1 – C_9$. The authors considered the junction resistance and capacitance of tunnel junctions J_1, J_2 and J_5 are 10^5 Ω and 10^{-19} F respectively and for J3 and J_4 are 10^5 Ω and 0.5 aF. The supply voltage of the circuit V_b is 16 mV, a constant value.

A and B are the consecutive two inputs of AND gate and Y provides the output of this circuit. The input voltages are driven into the gate through the capacitors C_1, and C_2 which are identical in true nature and their capacitances are limited to 0.5 aF. The gate output is obtained across capacitor C_8 or from island N_4. The authors here made the inputs piece-wise constant that apply the combinations of logic '0' and logic '1'. Fig. 7(a) and Fig. 7(b) depicts the input voltages of A, and B respectively. Fig. 8 shows the charge at output node. As revealed that in this node the charge is positive when the input vectors are 1 & 1; it changes to zero when the input vectors are 0 & 0, 0 & 1and 1 & 0 respectively. Consequently, the output waveform truly reflects the behavior of two input AND gate.

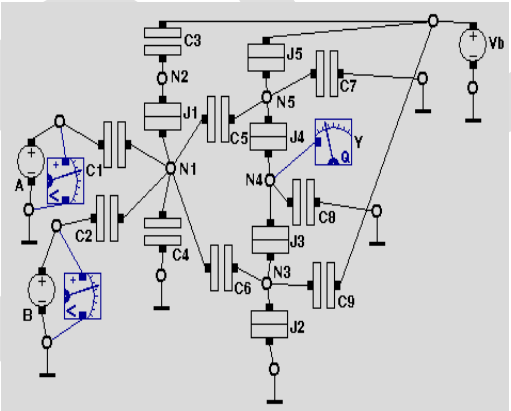

Fig. 6 Two input AND gate circuit

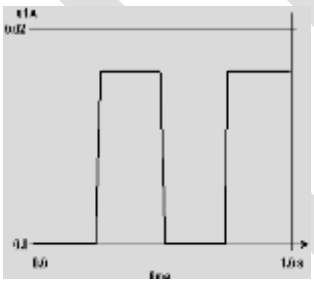

Fig. 7(a) AND input A

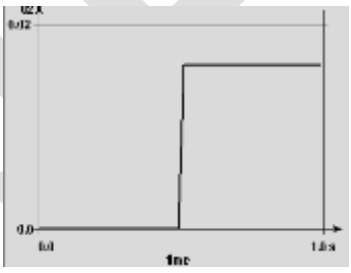

Fig. 7(b) AND input B

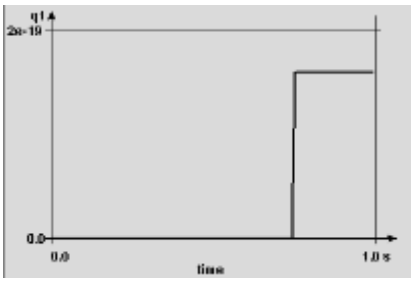

Fig. 8 AND gate output

INCORPORATING SET IN DECISION MAKING AND ITS SIMULATION USING SIMON:

The triumph of SET over all other existing technologies has been evidenced in several SCI journals since the last decade. Following the same note here the authors would like to report its application in designing SET based decision making ICs.

Let us consider the simple operation of a lawn-sprinkling system which is controlled automatically by certain combinations of the following variables –

For easement let the season be denoted as S, the moisture content of soil is M, the outside temperature is T and the Outside humidity is H; S remains 1 only for summer; whereas M,T and H remains 1 at high. The automatic sprinkler is expected turned on under any of the following circumstances.

1. The moisture content is low in winter.
2. The temperature is high and the moisture content is low in summer.
3. The temperature is high and the humidity is high in summer.
4. The temperature is low and the moisture content is low in summer.
5. The temperature is high and the humidity is low.

The authors here corroborated the simplest possible logic expression involving the variables S, M, T and H for turning on the sprinkler system. The given circumstances are straight forward realizations of 1,2,3,4 and 5 which are categorically expressed in terms of the defined variables S, M, T, and H as M S, TMS, THS, TMS, and TH, respectively. The Boolean expression is

$$f = \bar{S}\bar{M} + S\bar{M}T + STH + S\bar{M}\bar{T} + T\bar{H} \quad (1)$$

The expressions in terms of minterms and maxterms are obtained as-

$$fmax = \bar{M} + ST + T\bar{H} \quad (2)$$

$$fmin = (\bar{M} + T)(S + \bar{M} + \bar{H}) \quad (3)$$

Hereafter the authors represent the SIMON based modeling of the above proposed automatic sprinkler in Fig 9 and fig.10 respectively as obtained in equation 2 and 3.

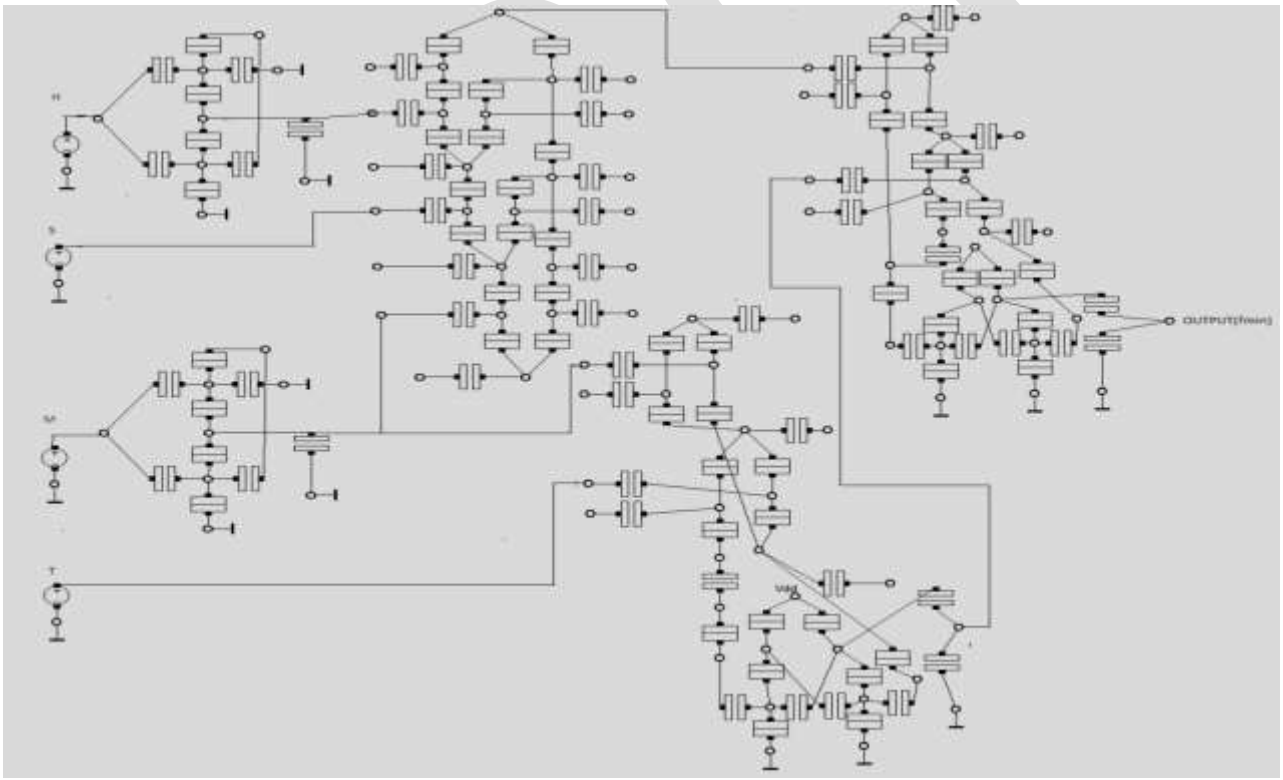

Fig 9: Realization of SET based equation 3 using SIMON 2.0

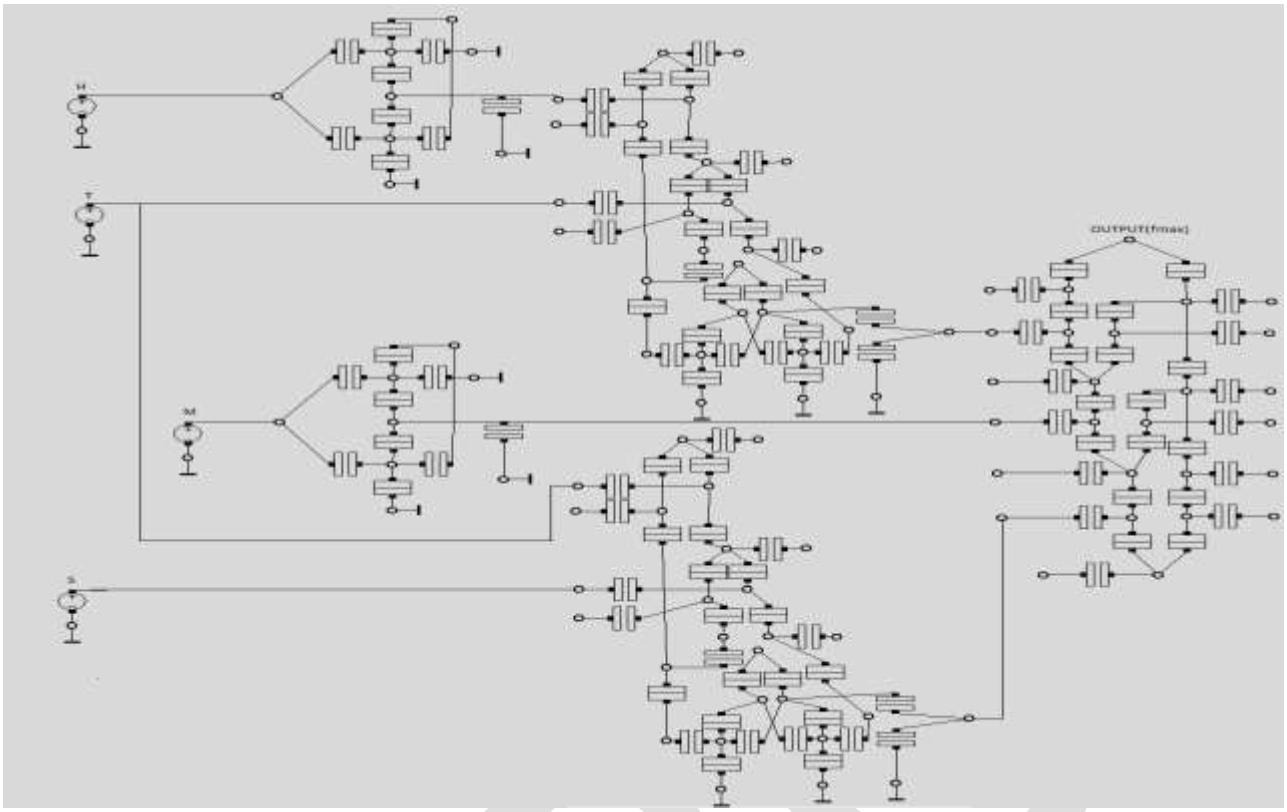

Fig10: Realization of SET based equation 2 using SIMON 2.0

CONCLUSION

Decision making hardware have attracted consumers owing to its mammoth features and excellent interfacings with human brain since last few years. Thus it can be more conveniently described as perfect automatic brain mapping system. The authors have moved a step forward to incorporate the same decision making sub system using next generation SET devices. The designed model shows a greater trade off. More complexity can be achieved in further.

REFERENCES:

[1] Ono, Y.; Takahashi, Y., "Single-electron pass-transistor logic and its application to a binary adder" Symposium on VLSI Circuits, 2001. Digest of Technical Papers. 2001.

[2] Degawa, K. ; Aoki, T. ; Higuchi, T. ; Inokawa, H. ; Takahashi, Yasuo, "A single-electron-transistor logic gate family and its application - Part I: basic components for binary, multiple-valued and mixed-mode logic", 34th International Symposium on Multiple-Valued Logic, 2004.

[3] Sulieman, M.H. ; Beiu, V. "On single-electron technology full adders", IEEE Transactions on Nanotechnology, Volume:4, Issue: 6, 2005.

[4] Lee, C.K. ; Kim, S.J. ; Shin, S.J. ; Choi, J.B. ; Takahashi, Y., "Single-electron-based flexible multivalued logic gates", Applied Physics Letters, Volume:92, Issue: 9, 2008.

[5] Tsiolakis, T. ; Konofaos, N. ; Alexiou, G.P., "A complementary single-electron 4-bit multiplexer", 2nd Asia Symposium on Quality Electronic Design (ASQED), 2010

[6] K.K.Likharev : "Single electron devices and their applications" Proc. IEEE vol 87, pp.606-632, Apr. 1999.

[7] P. Hadley, G. Lientschnig, and M. Lai, "Single-Electron Transistors," pp. 1–8.

[8] Liu, R.S. ; Pettersson, H. ; Suyatin, D. ; Michalak, L. ; Canali, C.M. ; Samuelson, L., "Nanoscaled ferromagnetic single-electron transistors", 7th IEEE Conference on Nanotechnology, 2007. IEEE-NANO 2007.

[9] M. Saitoh, N.Takahashi, H.Ishikuro and T. Hiramoto : Japan J. appl. Phys. 40, 2010, 2001.

[10] D.H. Kim, S.K. Sung, K.R. Kim, J.D. Lee, B.G. Park, B.H. Choi, S.W. Hwang and D. Ahn, IEEE Trans.E.D. 49, 627,2002.

[11] A. Tilke, R.H. Blick , H. Lorenz, J.P. Kotthaus, D.A. Wharam, Appl. Phys. Lett. 75, 3704,1999.

[12] K. Uchida, K. matsnzawa, J. Koga, R. Ohba, S. Takagi and A. Toriumi: Japan J. Appl. Phys. 39,2321,2000.

[13] Y. Nakamura, D.L. Klein and J.S. Tsai : Appl. Phys. Lett. 68,275,1996.
[14] A. Amar, D.Song , C.J . Lobb, and F.C. Wellstood : phys. Rev. Lett. 72, 3234,1994.
[15] Debasis Samanta, A.K.De, Giriprakash HD and Subir Kumar Sarkar "Design and implementation of a sequence generator using single electron device based threshold logic gates" – Far east journal of electronics and Communications, vol. 1, issue 3, December 2007.
[16] Casper Lageweg et al "A Linear Threshold Gate Implementation in Single Electron Technology" – IEEE proc. Computer society workshop on VLSI, April 2001, pp. 93-98.
[17] A.K.Biswas, S.K.Sarkar "An arithmetic logic unit of a computer based on single electron transport system" – Semiconductor physics, Quantum electronics and optoelectronics Vol. 6, 2003.
[18] Ono, Y. ; Takahashi, Y., "Single-electron pass-transistor logic and its application to a binary adder" Symposium on VLSI Circuits, 2001. Digest of Technical Papers. 2001.
[19] Dae Hwan Kim ; Suk-Kang Sung ; Kyung Rok Kim ; Jong Duk Lee ; Park, Byung-Gook, "Single-electron transistors based on gate-induced Si island for single-electron logic application", IEEE Transactions on Nanotechnology,2002.
[20] Degawa, K. ; Aoki, T. ; Higuchi, T. ; Inokawa, H. ; Takahashi, Yasuo, "A single-electron-transistor logic gate family and its application - Part I: basic components for binary, multiple-valued and mixed-mode logic", 34th International Symposium on Multiple-Valued Logic, 2004.
[21] Lageweg, C. ; Cotofana, S. ; Vassiliadis, S., "Binary addition based on single electron tunneling devices" 4th IEEE Conference on Nanotechnology, 2004.
[22] Chirstoph Wasshuber et al "SIMON – A simulator for single-electron tunnel devices and circuits" - IEEE trans. On computer aided design of integrated circuits and systems, vol 16, no.9, September 1997, pp.937-944.
[23] Subir Kumar Sarkar, D. Samanta, S. Sarkar, K. Senthil Kumar, J. Gope and Ankush Ghosh, "Single electron device based string detector for the identification of Frame Delimiters in Data Transfer Protocols", National Conference on Digital Information Management (NCDIM'07), Thadomal Shahani Engineering College & Computer society of India, Mumbai-400050, during 23-24th March 2007.
[24] Nakajima, F. ; Miyoshi, Y. ; Motohisa, J. ; Fukui, T., "Single-electron AND/NAND logic circuits based on a self-organized dot network", Applied Physics Letters, Volume: 83, Issue: 13, 2008.
[25] N. Basanta Singh, Sanjoy Deb, Asish Kumar De and Subir Kumar Sarkar, "Design and Simulation of 2–to-4 Decoder Using Single Electron Tunnelling Technology based Threshold Logic Gate" Journal of Electron Devices, Vol. 9, 2011, pp. 342-351