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Predictive Analysis of an Efficient Rank Based Fault Tolerance Network on Chip System

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Abstract— Network on Chip (NoC) are the integrated communication systems on a single chip. This paper presents a study of an Efficient Rank Based algorithm to reduce the area and the power consumption of the overall Network on Chip. The main motive of the research is to reduce the computation complexity for the fault tolerance. The Conventional algorithms are based on the table based routing that consumes much more time in calculating the routing path. We developed the rank based approach which will not depend on any tabular calculations for their routing. The paper presents the various considerations faced during the designing of a cost effective and scalable Rank Based Network on Chip architecture

Keywords— FTDR, Wormhole Routing, Network-on-Chip, HARQ, Rank Based Routing

INTRODUCTION

There were not any promising techniques and methods to integrate a large number of cores on a single chip before the existence of Network on chip and nor any technique could achieve the performance in comparison to the Network-on-Chip (NoC)However, as the CMOS technology scales down to the nanometer domain, smaller feature size, lower voltages and higher frequencies increase the number of occurrence of intermittent and transient faults, besides manufacturing defects and wear out erects which lead to permanent faults are also inevitable. The inherent structure redundancy of NoC provides the potential to design a fault-tolerant routing algorithm to enhance the reliability.

Recently, buffer less routing, also called detection routing, has been widely used for reducing the hardware overhead and power consumption of NoC. In detection routing, an incoming packet is always routed to a free output port even though it is far away from the destination. Because of its non-minimal routing characteristic, detection routing can be easily modified to achieve fault-tolerance.

This paper proposes a reconfigurable fault-tolerant detection routing algorithm (FTDR) based on a kind of reinforcement learning Q-learning. It is a table-based routing algorithm, which reason figures the routing table through Q-learning and uses 2-hop fault information to make efficient routing decision to avoid faults. In order to reduce the routing table size, we also propose a hierarchical Q-learning based detection routing algorithm (FTDR-H) with area reduction up to 27% for a switch in an 8*8 mesh compared to the original FTDR.

MOTIVATION

The main motive of the research is to reduce the computation complexity for the fault tolerance. The Conventional algorithms are based on the table based routing that consumes much more time in calculating the routing path. We developed the rank based approach which will not depend on any tabular calculations for their routing.

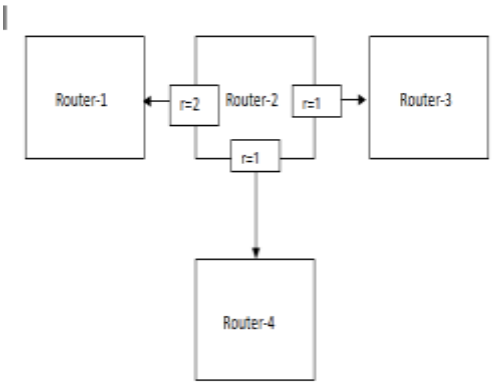

Fig.1. Rank Based Routing

The fig. given below depicts the rank based routing architecture for the network on chip system. Data will be transferred through the highest Rank port and the Rank will be decided according to neighbouring conditions.

NoC Architecture

The fig. given below describes the routing scheme in a network on chip architecture. The NoC architecture is based on Nostrum NoC, which is a 2D mesh topology. Each process element (PE) is attached to a switch (S), as shown in Fig. 1.

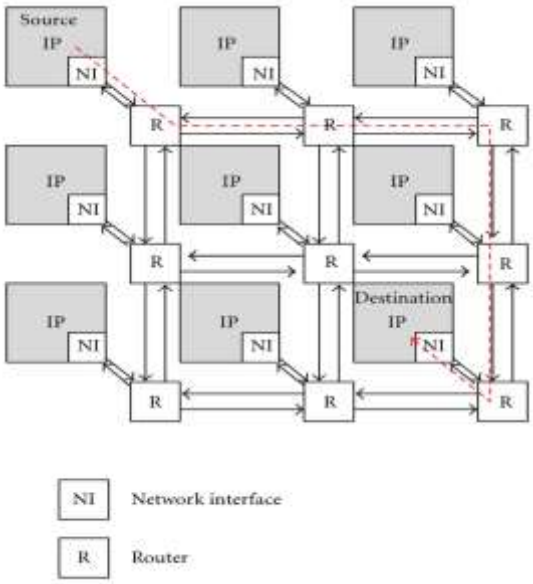

Fig. Routing in NoC

The difference from the ordinary 2D mesh is that the boundary output is connected to the input of the same switch, which can be used as a packet buffer. All incoming packets are prioritized based on its hop counts which record the number of hops the packet has been routed. The switch makes routing decision for each arriving packet from the highest priority to the lowest. If a desired output port has already been occupied by a higher priority packet, a free port with the smallest stress value, which is the traffic load of neighbour switches in last 4 cycles, will be chosen, which means the packet has to be detected.

BUFFERLESS ROUTING

Buffers in on-chip networks consume significant energy, occupy chip area, and increase design complexity. In this paper, we make a case for a new approach to designing on-chip interconnection networks that eliminates the need for buffers for routing or flow control.

We describe new algorithms for routing without using buffers in router input/output ports. We analyze the advantages and disadvantages of bufferless routing and discuss how router latency can be reduced by taking advantage of the fact that input/output buffers do not exist. Our evaluations show that routing without buffers significantly reduces the energy consumption of the on-chip cache/processor-to-cache network, while providing similar performance to that of existing buffered routing algorithms at low network utilization (i.e., on most real applications). We conclude that bufferless routing can be an attractive and energy-efficient design option for on-chip cache/processor-to-cache networks where network utilization is low.

HOW RANK WILL CHANGE AUTOMATICALLY IN RANK BASED NOC

As the address of the receiver router is sent with every data packet it knows the exact destination of departure. Also, on the hardware, all the blocks get implemented at the place and routing phase every router knows about their neighbor router. The rank based algorithm assumes its data path in no fault condition. While traveling through the different routers the data packet assign ranks to the ports of the router according the shortest path to the destination. As any fault detected in any port of the router immediately switches their path to the lower rank of the path and this process goes on.
The approach do not use any table based routing neither any complex algorithm it only uses the dynamic rank assignments at the run time. The algorithm satisfies both less area and less computation time.

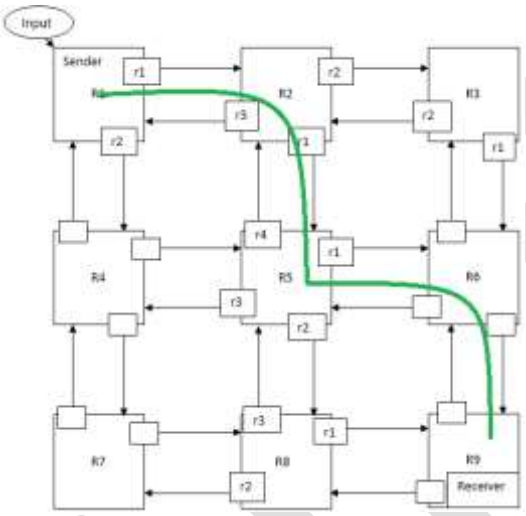

Fig. A Fault Less Rank Based NoC Architecture

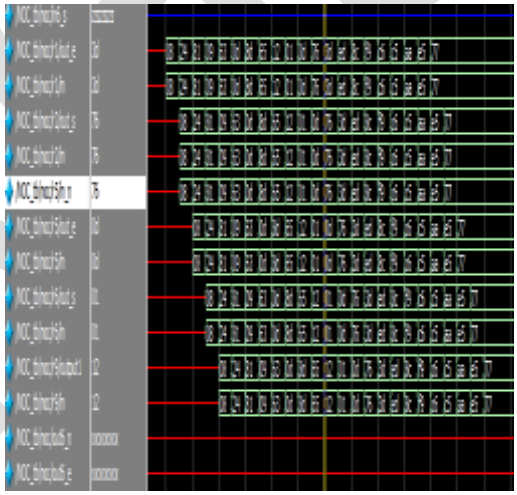

Fig. Output of a Rank Based NoC architecture

The figures above depicts the basic architecture of a rank based NoC router and its output waveforms.

Congestion Condition1- When data input on R5 from both the sides viz. SOUTH and NORTH

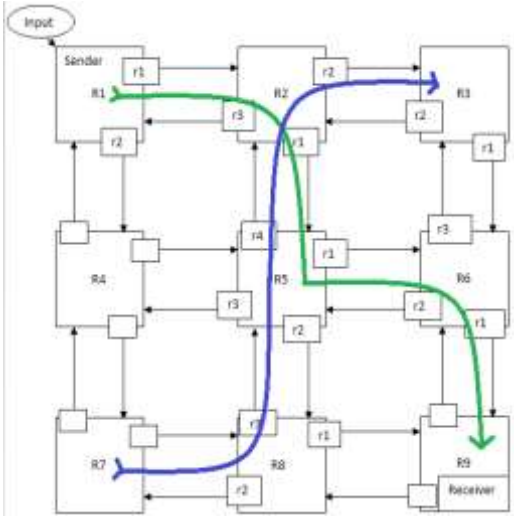

Fig. Congestion condition -1

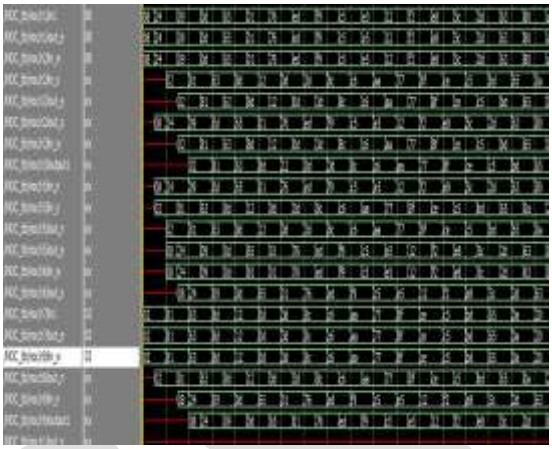

Fig. Output waveforms for Congestion condition-1

METHODOLOGY

This project implemented using HDL (Hardware Description Language), it can work live once it get fabricated to become a real chip. The algorithm is written in Verilog HDL to write the behaviour of NoC router. The rank based routing assigns the dynamic rank to each router sending the packets and when each packet is assigned with the shortest path. Thus, with the shortest path and rank assigned to each packet decreases the latency and improves the efficiency of the NoC architecture.

CONCLUSION

In this paper, we have discussed some of the issues generated in an Efficient Rank Based fault-tolerant solution for a bufferless NoC to protect it from faults and achieved low latency. The Rank based NoC is a complete new approach in the routing of a network to transmit the packets on the basis of their ranks to avoid the congestion in the network. This study will surely clear some doubts of the research associates working in Networking and will provide them an extra edge for the further research in the NoC architectures. The proposed NoC architecture will be the cost effective and more scalable when brought on hardware as it will transmit the packets according to their rank and need of the information at the receiver end.

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