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Pursuance of 36-bit RISC processors in collaboration with application of DSP using FPGA

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Abstract— Abstract—RISC has become main stream in scientific and engineering applications. The demand for (DSP) has increased with advent of computer, smartphone, gaming and other multimedia devices. Today, FPGA s has become an important platform to implement high end DSP processors due to their inherent parallelism and fast operating speed. This paper focuses on Pursuance of three stage 36-bit RISC processor with some of the applications of DSP using FPGA.The coding is done in Verilog synthesized by Xilinx ISE 12.2 and simulated using ISim.

Keywords—Arithmetic Logic(AL); Central Processing Unit(CPU);Control Unit(CU); Field Programmable Logic Array(FPGA); General Purpose Register(GPR); Program Counter(PC); Instruction Register(IR); Reduced Instruction Set Computer(RISC); Register Set(RS); Configurable Logic Blocks (CLBs).

INTRODUCTION

This is the era of high speed computing systems, the need for real-time embedded systems operate within rigorous requirements are often at the conflict between speed and area. Increasing complexity of signal, image or control processing in real-time applications requires high computational power witch can be achieved by high performance programmable components like RISC, DSPs and non-programmable specific chips such as FPGA based hardware. Thus RISC has become main stream in scientific and engineering applications. The demand for (DSP) has increased with advent of computer, smartphone, gaming and other multimedia devices. Todays, FPGA s has become an important platform to implement high end DSP processors due to their inherent parallelism and fast operating speed. This paper focuses on Pursuance of 36-bit RISC processor with some of the applications of DSP using FPGA .The coding is done in Verilog, synthesized by using Xilinx ISE 12.2 and simulated using ISim .

REMAINING CONTENTS

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What is the Reduced Instruction Set Computer (RISC)?

RISC-Reduced Instruction Set Computer is a microprocessor architecture which exploits a small, simple and highly-optimized set of instructions; these simple instructions fairly take the same amount of time for execution, making them ideal for pipelining

Main features of a RISC processor are-

- Most instructions are register based.
- Less number of addressing modes.
- Enhanced computation.
- Fixed length easily decoded and fixed instruction format.
- All operation done within the registers.
- Efficient and optimized instruction due to pipelining
- Best suited for parallelism, pipelined and superscalar architectures.

What is the Field Programmable Gate Array (FPGA)?

FPGA - Field Programmable Gate Array. Hypothetically it can be considered as an array of Configurable Logic Blocks (CLBs) that are connected together to form complex digital circuits by vast inter connection matrix. It is an Integrated circuit designed which can be configured either by a customer or by a designer after manufacturing hence the name "field programmable". The FPGA configuration is generally specified by using a hardware description language like Verilog.

Main features of FPGA are-

- FPGAs are Simple Programmable Logic Blocks.
- FPGAs have innovative logic structure.

- Larger Logic Functions can be built up by connecting many smaller Logic Blocks together.
- FPGAs support Massive Fabric of Programmable Interconnection.
- FPGAs include rich feature set such as high-performance DSP blocks and on-chip memories.
- FPGAs are best suited for rapid prototyping of digital circuits.

What is the Digital Signal Processor (DSP)?

DSP-Digital Signal Processor is a specialized microprocessor developed for fast operational needs of digital signal processing. A Digital Signal Processor is predominantly for those applications which cannot tolerate delays because the main feature of DSP is to process the data in real time. The different kinds of programmable digital signal processors are image signal processor, radar processor, pixel processor, piccolo processor ARM versatile cortex processor.

Main features of DSP are-

- Performs special arithmetic operations like Multiply accumulates (MACs)
- Implements DCT (Discrete Cosine transform) and IDCT (Inverse Discrete Cosine transform).
- Executes FFT (Fast Fourier Transform) and IFFT (Inverse Fast Fourier Transform).
- Uses VLIW (Very Large Instruction Word) techniques such that each instruction drives multiple arithmetic units in parallel.

1. DESIGN ARCHITECTURE

This proposed Design is of 36 bit RISC Processor using Verilog HDL, the designed module will be synthesized using Xilinx ISE 12.2 Web pack, [4] and the verification will be done on Isim simulator, the architecture attempt to produce more CPU power by simplifying the instruction set of the CPU. Figure: 1.1 shows the Block Diagram of RISC system [4]. It includes Decoder, fetch machine, Arithmetic and logic machine, and register set.

The control unit generates all the control signals required to control the coordination amongst the component of the processor. This is basically carried out through three main steps viz,1) Fetch an instruction; 2) Decodes the instruction; and 3) Executes the instruction. Each step is finished within a single state of the finite-state machine and each instruction is usually executed in one clock cycle, while some of the memory access instructions may oblige two or more clock cycles to complete, henceforth they may require quite a few states for correct timing. For fetching the instruction the control unit basically reads the memory location stated by the Program Counter (PC), and copies the content of that location into the instruction register (IR). The Program Counter (PC) is now incremented by 1. For decoding, the control unit abstracts the opcode bits from the instruction register and defines what the current instruction is jumping to the state which is assigned for executing the instruction. Once in that particular state, the control unit performs execution by simply emphasizing the appropriate control signals for controlling the data path to execute that instruction. Control unit consists of controller, instruction register, multiplexer, program counter [1].

- **BLOCKDIAGRAM**

The block diagram of 36 - bit RISC processor is shown in Fig. 1. The RISC processor architecture consists of Arithmetic Logic Unit (ALU), Control Unit (CU), Barrel Shifter, Booth's Multiplier, Register File and Accumulator. RISC processor is designed with load/store (Von Neumann) architecture, signifies that all operations are executed on operands held in the processor registers and the main memory can be accessed only through the load and store instructions. One shared memory for instructions (program) and data with one data bus and one address bus between processor and memory. Fetching instruction and data in sequential order so that the latency acquired between the machine cycles can be reduced. For increasing the speed of operation RISC processor is designed with three stage pipelining. The pipelining stages are Instruction Fetch (IF), Instruction Decode (ID), Execution (EX),

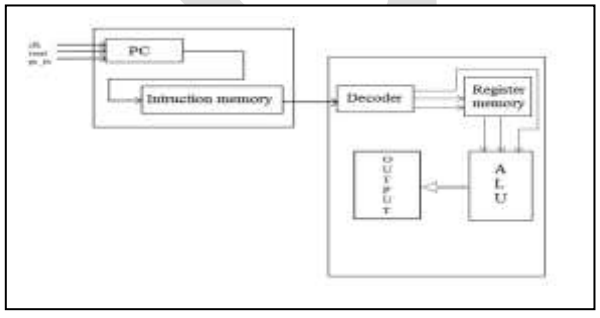


Fig. 1. Block diagram of RISC processor

- **WORKING**

Instruction Fetch Machine: This machine fetches an instruction from external memory, using the address that is currently being stored in the Program counter (PC), and upon completion of the instruction fetch cycle this machine signals the decoder to decode the instruction. On the completion of the fetch operation, the Program counter (PC) points to the successive instruction that will be read at the subsequent cycle.

Decoder: Upon accomplishment of the instruction fetch cycle, the instruction is decoded. This machine utilizes a 7-bit up counter with an active low reset. The decoder reads 4-bits of the IR and decides which of the sixteen operations the CPU requests to perform, and signals one of the next states to initiate its operation.

Execution of the instruction: The control unit of the CPU decoded the information as a sequence of control signals to the relevant function units of the CPU for execution of the actions which are required by the instruction such as reading values from registers, passing them to the ALU etc.,. On the basis of opcode the ALU can carry out Arithmetic, Logic and DSP operations. If the opcode obtained after decoding the instruction represents the DSP operation the input data is obtained from DSP memory by enabling RISC_DSP signal and writing the back the results into a register.

- **INSTRUCTION SET AND INDTRUCTION FORMAT**

RISC & DSP System perform 16 operations. It comprises of 11 Arithmetic and Logic operations and 4 DSP Operations. The instruction set use 4 bit Opcode to perform various operations for selection of instructions as shown in table below

TABLE I.INSTRUCTION SELECTION

Instruction	*Opcode*	*Operation undertaken*
OR	0000	OR operation of two registers
AND	0001	AND operation of two registers
NAND	0010	NAND operation of two registers
NOR	0011	NOR operation of two registers
XOR	0100	XOR operation of two registers
XNOR	0101	XNOR operation of two registers
ADD	0110	ADD operation of two registers
SUBTRACT	0111	SUBTRACT operation of two registers
NOT	1000	NOT operation
INCREMENT	1001	Increment the value by 1
ECREMENT	1010	Decrement the value by 1
FFT	1011	Perform FFT Operation
IFFT	1100	Perform IFFT Operation
DCT	1101	Perform DCT Operation
IDCT	1110	Perform FFT Operation

2. DSP OPERATIONS

- **DFT and FFT**

The discrete Fourier transform is the technique of interpreting any sequence of discrete values into its frequency domain, FFT is the more efficient method of generating a DFT. An FFT calculates the DFT and products is precisely the same results as that of calculating the DFT and the vital dissimilarity is that an FFT is much faster. The formula for DFT is defined as,

$$X(k) = \sum_{n=0}^{N-1} x(n).e^{-j\left(\frac{2\pi}{N}\right)nk} \quad (k = 0,1,\dots,N-1)$$

The calculation of X(K) requires N² complex multiplications and N (N-1) complex additions. In order to avoid this complication, Radix-2 DIT FFT Algorithm is used. The butterfly method of 8-point radix-2 DIT FFT algorithm is shown below

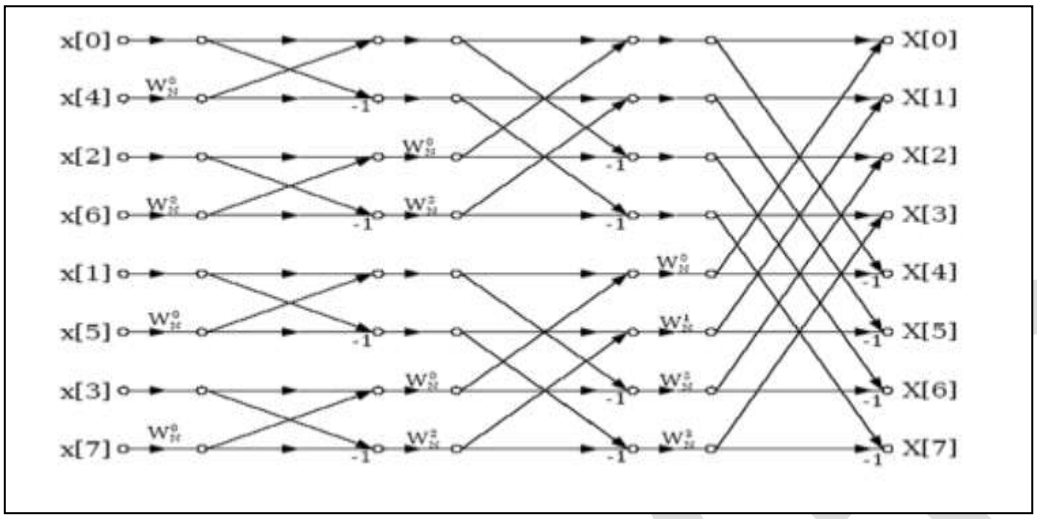


FIG 2.1 Butterfly method.

- **DCT AND IDCT**

The discrete cosine transform is similar to the discrete Fourier transform; DCT transforms a sequence or an image from the spatial domain to the frequency domain. The N point 1-D DCT is defined as

$$F(u,v) = \frac{2}{N} C(u)C(v) \sum_{x=0}^{N-1} \sum_{y=0}^{N-1} f(x,y) \cos\frac{(2x+1)u\pi}{2N} \cos\frac{(2y+1)v\pi}{2N}$$

The N-point 1-D IDFT is defined as

$$f(x,y) = \frac{2}{N} \sum_{u=0}^{N-1} \sum_{v=0}^{N-1} C(u)C(v)F(u,v) \cos\frac{(2x+1)u\pi}{2N} \cos\frac{(2y+1)v\pi}{2N}$$

$$C(u), C(v) = \begin{cases} \frac{1}{\sqrt{2}} & \text{for } u,v = 0 \\ 1 & \text{otherwise} \end{cases}$$

3. RESULTS

The proposed operation of RISC processor and DSP processor is been simulated and synthesized using Xilinx ISE version 12.2. and the RISC RTL schematics is shown in figure 3.1. The RISC-DSP System executes 4 DSP operations viz, FFT, IFFT, DCT & IDCT. Firstly the 8 point FFT is designed and simulated using Decimation in Time Radix-2 Algorithm using designed 2- point FFT with the help of butterfly diagram. The design of 4 point FFT is done using two 2-points FFT and so on. Simulation of 8-Point FFT and IFFT are shown in figure3.2 and 3.3. Simulation result of various ALU operations and DSP operations performed by the RISC system is shown figure 3.4.

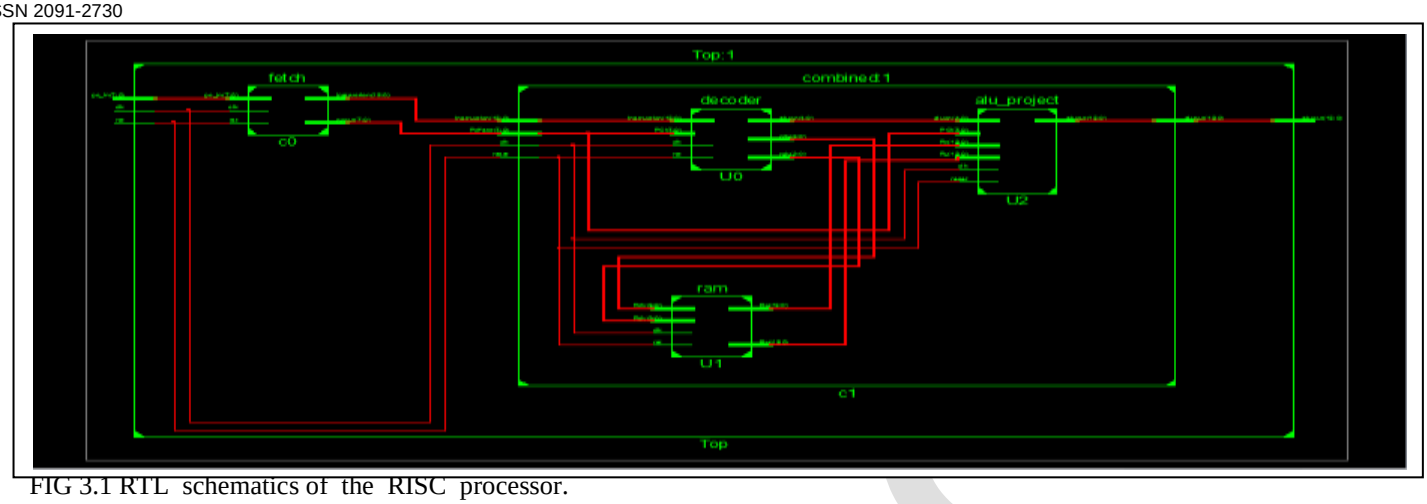


FIG 3.1 RTL schematics of the RISC processor.

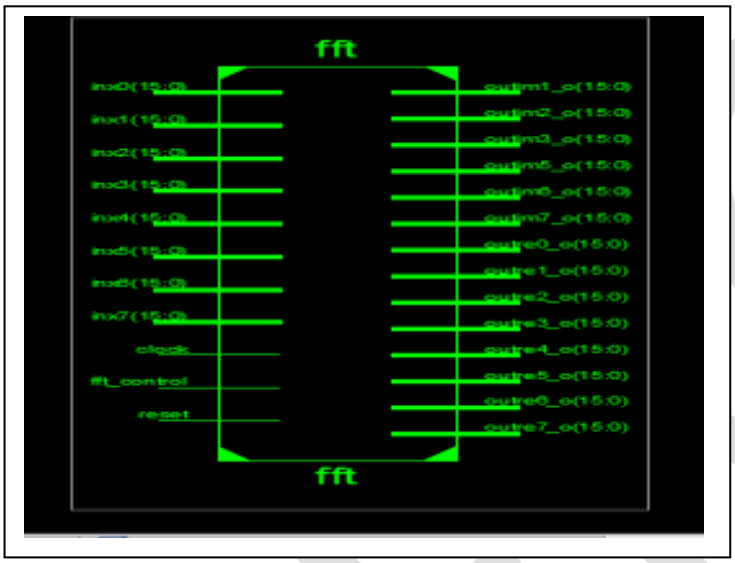
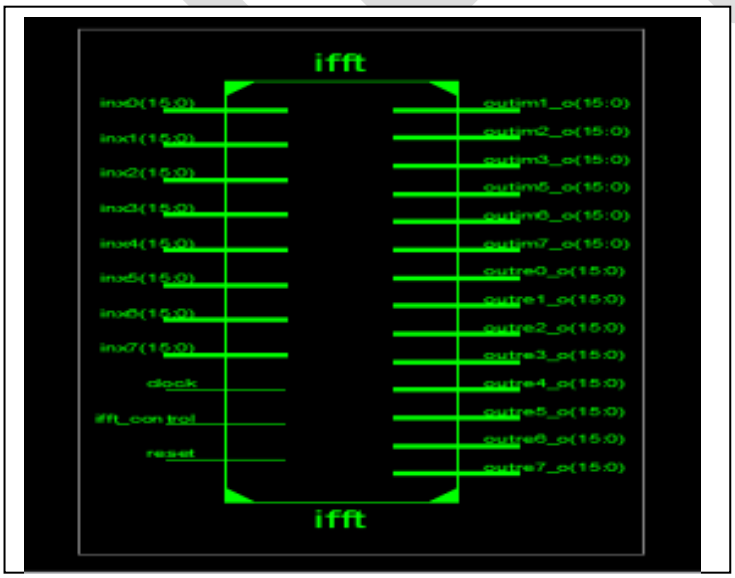


FIG 3.2 FFT RTL Schematics .



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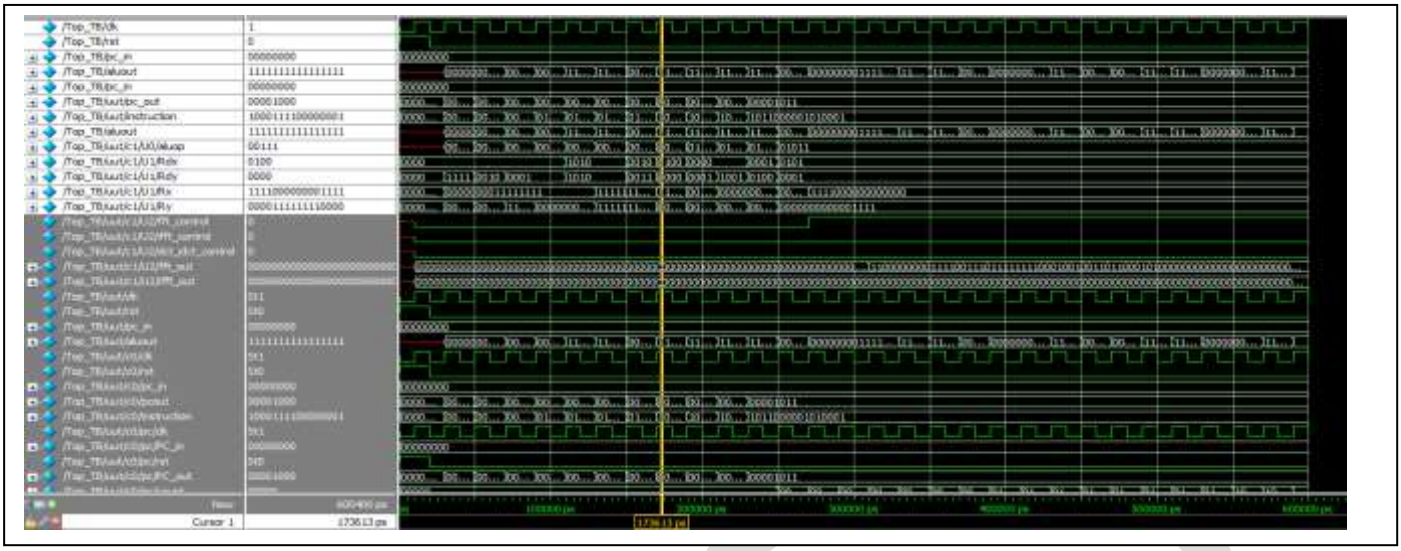

FIG 3.4 Simulation of ALU and DSP operations .

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CONCLUSION

The design of 36-bit RISC processor is implemented using the Xilinx ISE 12.2 and it is been realized using Verilog and simulated with ModelSim. This paper helps in understanding the processor development using Verilog. The Instructions are all executed the in one clock cycle, comprising of jumps, returns from subroutines and even external accesses. The simulations and results of this processor provide various features including ALU, DSP operations. The processor also supports signal processing applications. The design implemented can be easily seen in the Xilinx window. The value of the output and input bits is effortlessly elevated by increasing the memory of the processor.

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