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Study of Differential Amplifier using CMOS

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Abstract— The Differential amplifier is one of the versatile circuits in analog circuit design. A differential amplifier is a circuit that can accept two input signals and amplify the difference between two input signals. The circuit consists of NMOS and PMOS devices, where n-channel MOSFET is used to form differential pair and p-channel current mirror load is used. The technology used, is 0.18µm and 1.8V supply voltage is applied. The design and simulation has been carried out in ADS tool.

Keywords— Differential Amplifier, CMOS, NMOS, PMOS

INTRODUCTION

The amplifier, which amplifies the difference between two voltages is called Differential Amplifier. It is used to provide high voltage gain and high common mode rejection ratio. It has another characteristic such as very low input bias current, very low offset voltage and very high input impedance. Differential amplifier can operate in two modes which are differential mode and common mode. Common mode type gives result of zero output while differential mode gives a result of high output, hence this amplifier has high common mode rejection ratio. If two input voltages are equal, then the differential amplifier gives an output voltage of almost zero volt and if the two input voltages are not equal the differential amplifier gives high output voltage.[1]

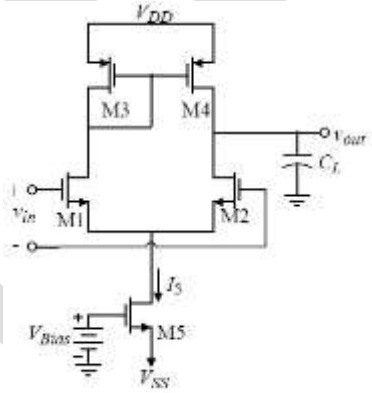


Fig.1. Circuit diagram of Differential amplifier

II. Circuit Operations

The figure shown above is an active load MOSFET differential amplifier. MOSFET M1 and M2 formed differential amplifier pair. MOSFET M5 is a current sink used to provide bias current to the amplifier. MOSFET M3 and M4 form a current mirror. Considering that all transistors are in saturation region. The Bulk of all transistor connected to their sources. The current flowing from transistor M5 is divided into two equal parts and flows through M1, M3 and M2, M4 respectively. Transistor M3, M4 connects to the V_{DD} supply, whereas transistor M5 connected to V_{SS}. The circuit is made up of NMOS and PMOS hence their design and simulation results are given below.[2]

1. NMOS

The NMOS transistor is biased with positive gate to source voltage (Vgs=1.8V) and drain to source voltage (Vds=1.5V) whereas the body is connected to a source. The I-V characteristics show the result between Id vs Vds for different values of Vgs and another graph of Id vs Vgs. As the gate to source voltage is positive the current Id flows only when Vgs voltage is greater than the threshold voltage. The NMOS transistor is simulated using the BSIM-3 model as all parameter values are taken from model file of TSMC with 0.18 micron technology. The length of NMOS is considered as 1µm and width is 10µm. After simulation, we are getting values of threshold voltage, β which will used in future calculations.[1,2]

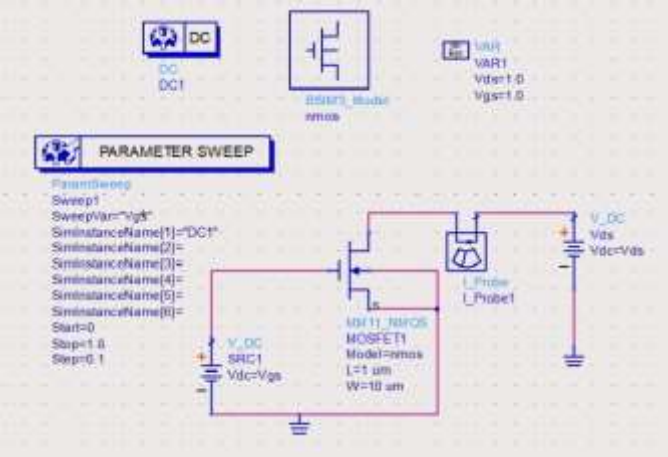


Fig.2. NMOS Design

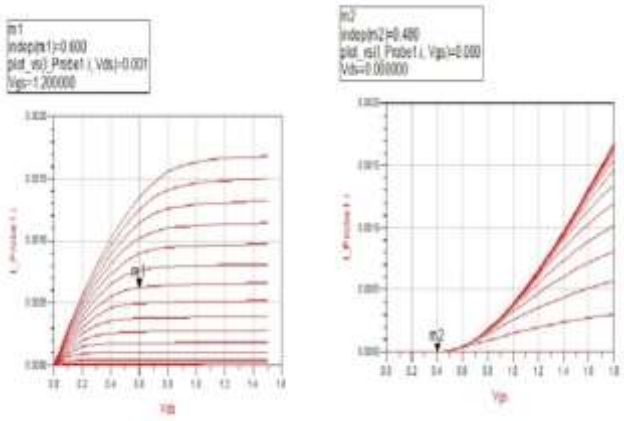


Fig.3. NMOS Simulation

The simulation result shows that when positive gate voltage applied to NMOS with Vgs=0, Id is non-existent even when some positive Vds voltage is applied. It is found that for getting significant amount of drain current Id, we have to apply sufficiently high positive gate voltage Vgs. The minimum gate to source voltage which produce N-type inversion layer and hence drain current flows is called threshold voltage when Vgs=Vt. When Vgs<Vt, Id=0. Drain current only start when Vgs>Vt. For a given Vds, as Vgs is increased, virtual channel deeps and Id increases.[4]

1. PMOS

The PMOS transistor is biased with negative gate to source voltage (Vgs=-1.8V) and drain to source voltage (Vds=-1.5V) whereas body is connected to source. The I-V characteristics show the result between Id vs Vds for different values of Vgs and another graph of Id vs Vgs. As the gate to source voltage is negative the current Id flows only when Vgs voltage is greater than the threshold voltage. The PMOS transistor is simulated using the BSIM-3 model as all parameter values are taken from model file of TSMC with 0.18 micron technology. The length of PMOS is considered as 1µm and width is 10µm. After the simulation, we are getting values of threshold voltage, β which will use in future calculations.[1,2]

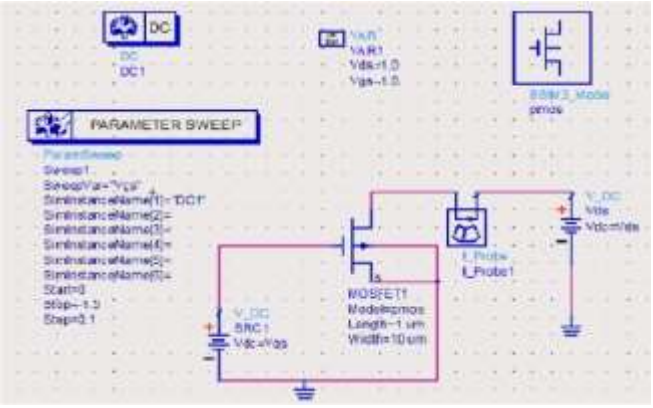


Fig.4. PMOS Design

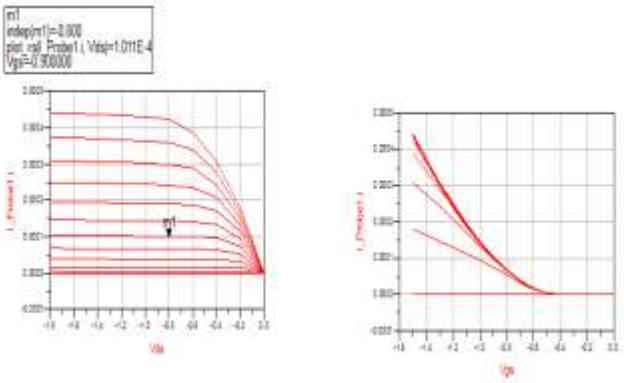


Fig.5. PMOS Simulation

The simulation result of PMOS is shows that when negative gate voltage applied with Vgs=0, ID is non-existent even when some negative Vds is applied. It is found that for getting significant amount of drain current Id, we have to apply sufficiently high negative gate voltage Vgs. The minimum gate to source voltage which produce P-type inversion layer and hence drain current flows is called threshold voltage when Vgs=Vt. When Vgs<Vt, Id=0. Drain current only start when Vgs>Vt. For a given Vds, as Vgs is increased, virtual channel deeps and Id increases

1. Differential Amplifier Design

The Differential amplifier design consists of NMOS, PMOS transistor. The NMOS current mirror circuitry is used to provide constant current to differential amplifier. Whereas all transistor body are connected to source of respective transistors. The Vdd supply voltage is given as 1.8V. Both input terminal of the differential amplifier i.e Vin1 and Vin2 connect to sine wave having Vdc=0.8V with amplitude 1mv and Vdc=0.5v having an amplitude 1mV with 180 phase shift respectively. The output is taken from the Vout terminal where 10pf capacitive load is connected. Similarly here BSIM3 NMOS and PMOS model are used to simulate differential amplifier. Considering all MOS are in saturation region. Transient analysis is done and simulation graph shows output Vout vs Time. For calculation of gain AC analysis also done and result shown below.[3]

From slew rate and capacitance we can find current flowing through transistor. Assuming slew rate is 10v/µsec.

$$slew\ rate\left(\frac{dv}{dt}\right) = \frac{I}{CL} \quad \ldots\ldots\ldots \quad 1$$

By ICMR+ we can find (W/L) for M3 and M4 considering ICMR+=1.6v and ICMR-=0.6v.

As M1 and M2 are in saturation region using equation Vds>Vgs-Vt, as Vt=0.4v

The current equation in saturation region is(2 &3)

$$Ids = \frac{\beta}{2(Vd - Vs)}^2 \quad \ldots \quad \ldots\ldots\ldots \quad \ldots\ldots 2$$

$$Ids = \frac{\mu Coxw}{2L(Vd - Vs)}^2. \quad \ldots\ldots\ldots\ldots \quad \ldots 3$$

$$gm = \frac{\partial Ids}{\partial Vgs} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 4$$

Gain bandwidth = $\frac{gm}{2\pi fCl}$ ……5

$$\frac{W}{L} = \frac{gm^2}{2Idsμ Cox} \quad \text{.....6}$$

For calculating (W/L) ratio of M3 &M4 eq. (1&2) will used. For M1 & M2 eq.(3,4,5,6) will uesd and for M5,M6 eq.3 will uesd. Where Ids6=100µAmp, Vdd=1.8v, Gain bandwidth=4Mhz.

$(W/L)_{1,2} = 4$, $(W/L)_{3,4} = 28$, $(W/L)_{5,6} = 5$ respectively.

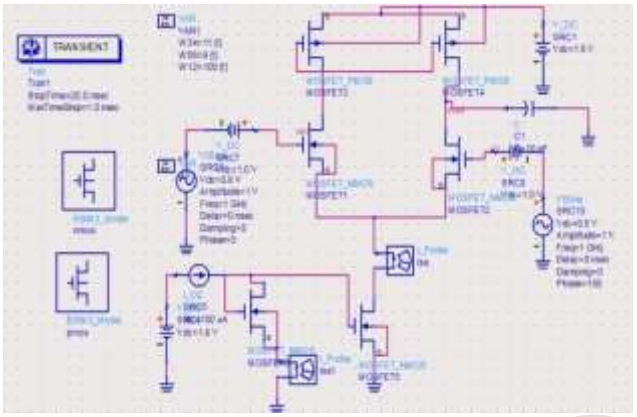


Fig.6. Transient Analysis

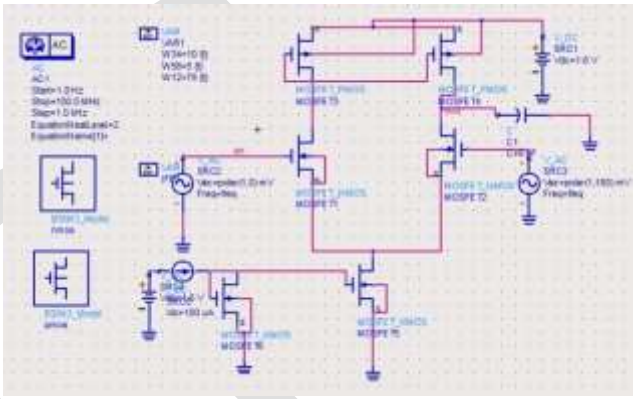


Fig.7. AC Analysis

Differential Amplifier Simulation

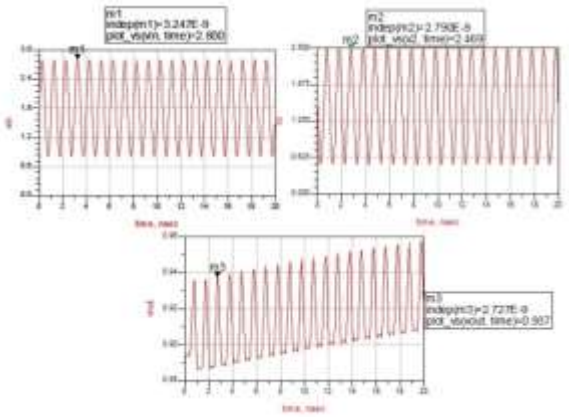
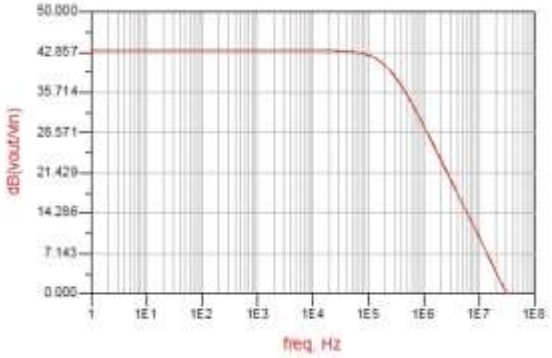


Fig.8. Simulation of Transient Analysis



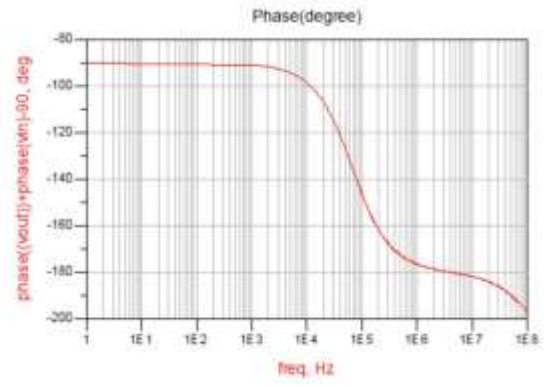


Fig.9. Simulation of AC Analysis

CONCLUSION

In this work differential amplifier is designed for the opamp application. The specifications are decided as required for OPAM application. The theoretically W/L ratios are decided for amplifier. By using this values amplifier is designed. The accuracy of results are improved by Agilent ADS.

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