

# Low Power-Delay-Product CMOS Full Adder

Ankita Bhati, Prof. Vinod Kr. Pathak, Dr. Rita Jain

Department of Electronics and Communication, LNCT, Bhopal, India, aankita.bhati@gmail.com

**Abstract**— This paper shows an effective and improved circuit design for 1-bit full adder circuit with lesser energy required. The circuit is designed using total number of 9 transistors. The proposed circuit performance better in terms of power, delay, power delay product which is very easily shown by the simulation results. There is comparison of performance among proposed circuit with other pre-exist circuits in various literatures and this comparison shows higher reduction in Power-Delay-Product (pJ) of our proposed design. It has remarkably improved power consumption and temperature sustainability when compared with existing design. BSIM standard models are used for simulations. The proposed design gives faster response for the carry output and can be used to reduce more at higher temperature.

**Keywords**— nMOS; pMOS; Adder; PDP, Delay.

## INTRODUCTION

Addition is one of the fundamental arithmetic operations. It is used extensively in many VLSI systems such as microprocessors and applications specify DSP architecture. In addition to its main task which is adding two numbers, it is the nucleus of many other useful operations such as, subtraction, multiplication etc. In most of these systems the adder lies in the critical path that determines the overall performance of the system. The XOR gate is the basic building block of the full adder circuit. The performance of the full adder can be improved by enhancing the performance of the XOR gate. The main intention of reducing this transistor count is to reduce the size of XOR gate so that large number of devices can be configured on a single silicon chip thereby reducing the area and delay.[1]. Most of the time increasing the threshold voltage could limit performance loss but results get increased leakages [2]. There are some other techniques as well which are used for design of low power which includes clock gating along with dynamic voltage or frequency scaling [3] and [4]. Energy-efficiency is one of the most required features for modern electronic systems designed for portable applications. 1bit Full Adder (FA) cell is the building block for most implementations of subtraction, addition operations. Full adder circuit is functional building block and most critical component of complex arithmetic circuits like microprocessors, digital signal processors or any ALUs. Almost every complex computational circuit requires full adder circuitry. The entire computational block power consumption can be reduced by implementing low power techniques on full adder circuitry To meet the rising demand, we advise a new energy efficient power adder by reducing the number of the MOS Transistor which reduces loss problem, considerably diminishing the power consumption compared to its peer design. So a new improved 9T 1-bit full adder cell is presented in this paper. We have conducted simulation runs in different input patterns, varying voltages and temperatures. The reason to do these many simulations is to give a better confidence to how this new adder would perform under all possible practical applications. Results demonstrate improvement in threshold loss, power consumption and temperature sustainability.

## THEORETICAL BACKGROUND

Full Adder circuit adds a pair of matching bits of the two different numbers which are expressed in binary form and carry from the earlier stage producing a sum with a new carry. Hence, it is also called a two input adder. Basically adder topologies are based on two XOR circuits (Module I and Module II) generating the sum and Module 3 made up of different topologies to generate the carry out as shown in fig.1. The Carry signal can be obtained by using one MUX and one XOR output.

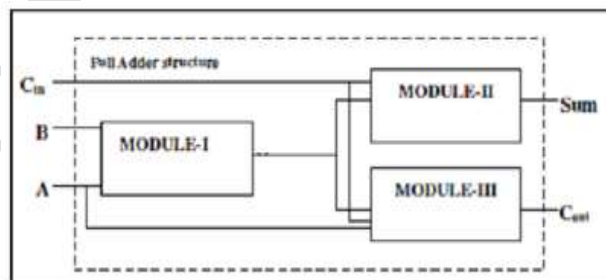


Fig.1: Structure of Full Adder

**PREVIOUS WORKS**

Full adder circuit is designed for addition binary logics. Sum signal (SUM) and carry out signal (COUT) are the output of I-bit full adder. Both of them are generated by input A, B and C<sub>IN</sub> following Boolean equation as:

$$SUM = A \oplus B \oplus C_{IN} \tag{1}$$

$$C_{OUT} = AB + BC_{IN} + AC_{IN} \tag{2}$$

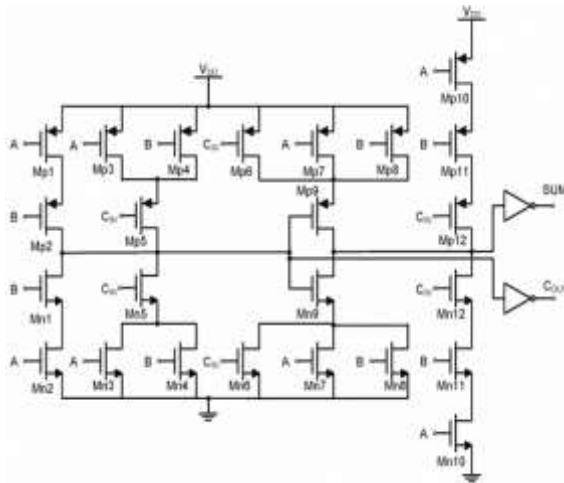


Figure 2. Conventional CMOS full adder [1][5][6][7]

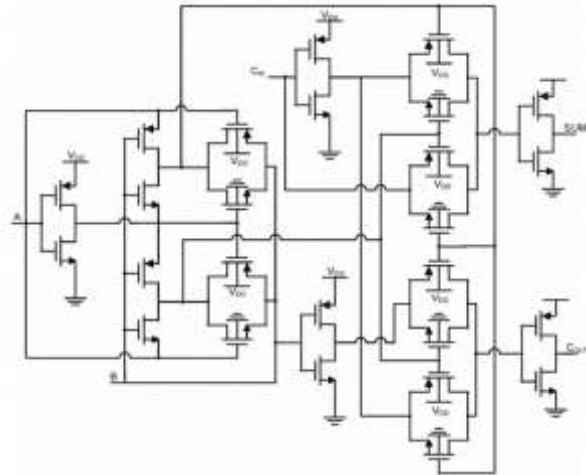


Figure 3. Transmission gate full adder [8]

Conventional CMOS full adder [1] [5] [6] [7], as shown in Fig. 2, is the complementary CMOS structure, which combines transistor PMOS pull-up and transistor NMOS pull-down network to produce output. The complementary CMOS logic circuit has the advantage of layout regularity and stability at low voltage. It has a high transistor count which consumes area and power. The problem of this adder is delay imbalance. Because SUM signal relies on the generation of COUT signal; there is a delay between two signals. The transmission gate full adder is illustrated in Fig. 3, which based on transmission gate [8]. It has lower-transistor count and lower loading of the input. After generated, SUM and COUT signal are balanced than the Conventional CMOS full adder. It provides transistor buffer output of SUM and COUT for a high driving capability. In Fig 4 shows Hybrid transmission gate/pass transistor logic full adder [7]. It is developed from transmission gate, pass transistor logic and enhance the driving capability by insert inverters at output. Its drawback is high power consumption.

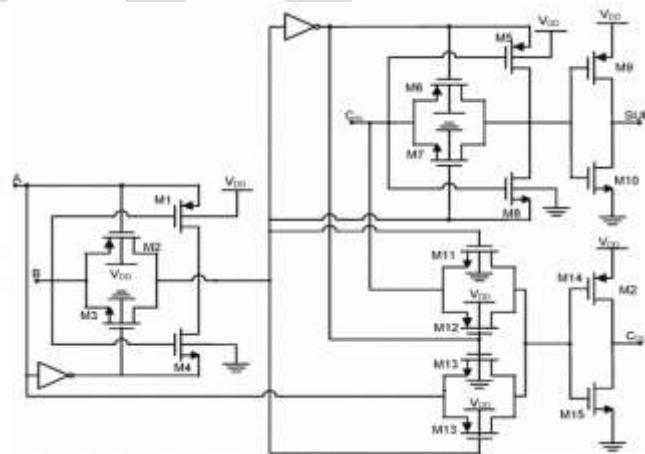


Figure 4. Hybrid transmission gate/pass transistor logic full adder [7]

## PROPOSED WORK

The Full adder design in static CMOS with complementary PMOS and NMOS [13]. This adder is based on regular CMOS structure (pull-up and pull-down network), which uses both NMOS and PMOS transistors. These transistors are arranged in a structure formed by two complementary networks. In static CMOS, the NMOS transistors only need to pass 0's and the PMOS only pass 1's, so the output is always strongly driven and the levels are never degraded. This is called a fully restored logic gate. Pull-up network is complement of pull-down. Below schematic, fig 5, is a Full adder cell of 9 transistors which is implemented by using CMOS technique (used sum and carryout equations).

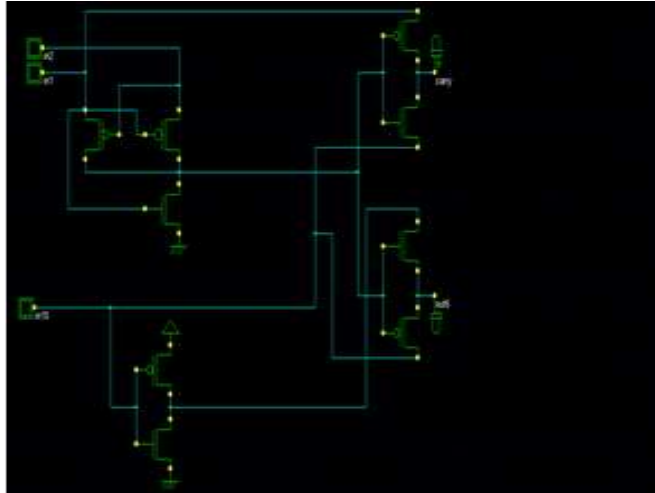
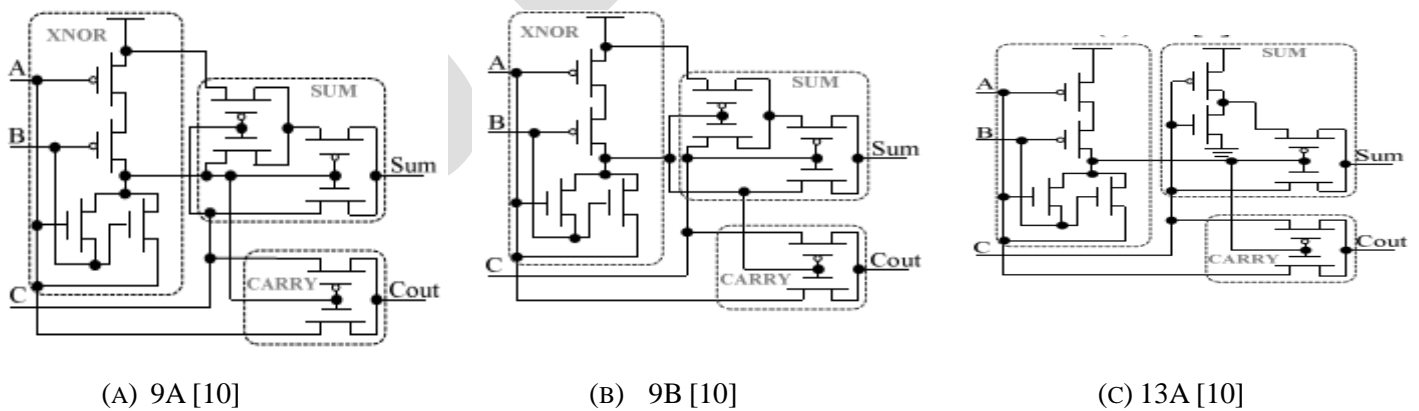
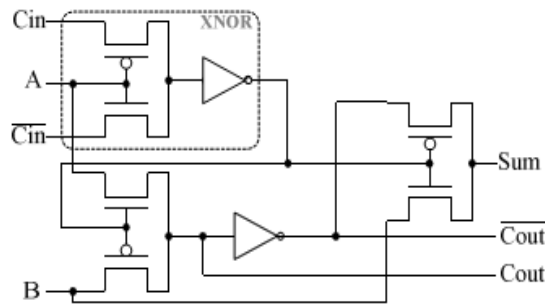


FIG 5: PROPOSED 9 TRANSISTOR FULL ADDER

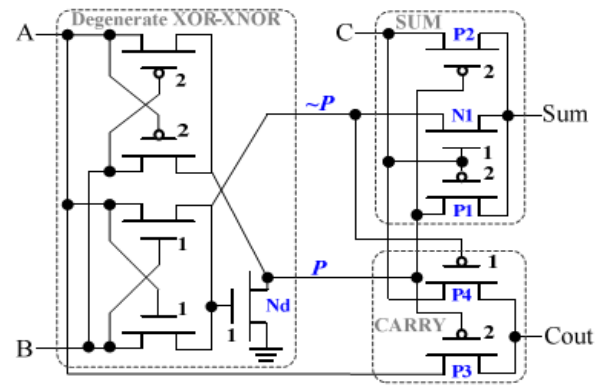
## SIMULATION AND RESULTS

The proposed full adder circuit as well as other reported circuits is simulated by using Microwind2 and Dsch2 tools for power consumption, area, and delay at 120nm and 70nm technologies with appropriate supply voltages and the results are given in Table 1. The proposed 1 bit adder cell consumes lower power compared to other reported circuits and also gives faster response for carry out and degrades sum output response compared to 9A [10], 9B [10], 13A [10], CLRCL [11] and CP-FA, respectively. CLRCL (Complementary and Level Restoring Carry Logic) is previous version of 10-T full adder [12] design featuring low power operations and fast carry signal propagation. Typical transistor sizes, i.e. (pMOS/nMOS)=1.0 $\mu$ m/0.5 $\mu$ m in width and 0.18 $\mu$ m (minimum feature size) in length are applied to all.





(D) CLRCL [11]

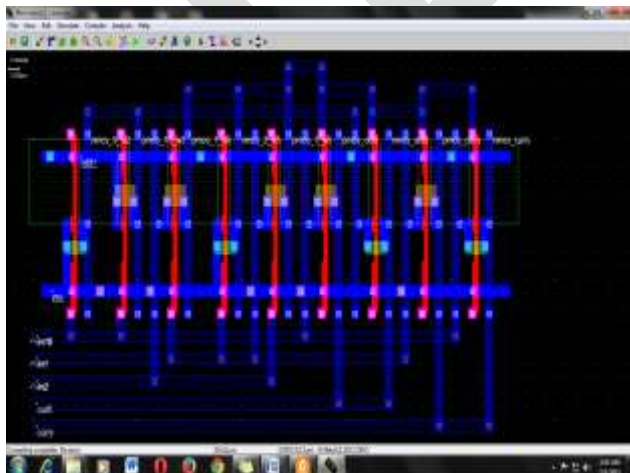


(E) 10-T FULL ADDER

**Fig 6: Various Full Adder Design**

TABLE I. 6 FULL ADDERS SIMULATION RESULTS

Full Adder Designs	9A	9B	13A	CLRCL	10-T	PROPOSED
$C_{out}/CARRY$ DELAY (nS)	4.11	3.92	3.84	1.52	0.85	.0023
Power Consumption (uW)	36.68	43.07	39.01	39.82	33.25	1.34
Power-Delay-Product (pJ)	150.75	168.83	149.8	60.53	28.26	0.003082



Simulation waveforms of proposed 9-Transistor full adder design

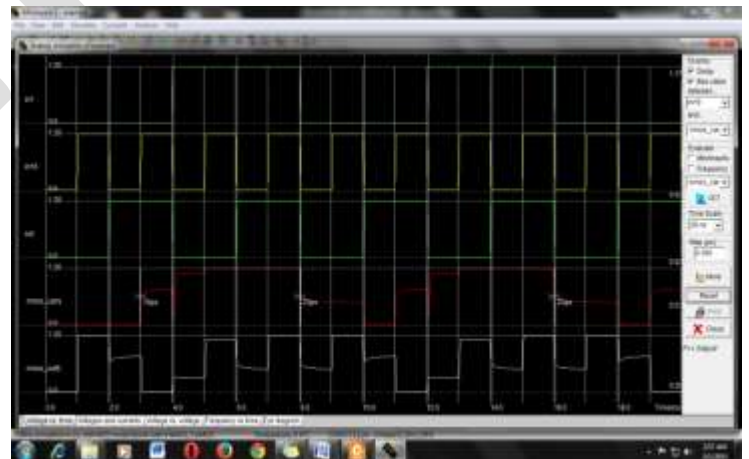


Fig 7: Layout of proposed full adder circuit

Fig 8

The PDP (Power-Delay-Product) was calculated and simulated plotted. We constructed full adder cells with the basic techniques and our proposed technique. Table I, Figure. 6 and Figure 7 show the comparison of delay of all the reference circuits, the basic circuits and the proposed circuit. Table I compares the power consumption of the circuits. At the same time, Table I in association with figure 7 compared the power delay product (PDP) of the proposed adder with the conventional adders. When compared to the other circuits it can be seen that the power-delay-product (PDP) can be reduced many-many times in the proposed adder circuit.

## ACKNOWLEDGMENT

The authors wish to thank Dr. Rita Jain (Prof. and Head, Department of Electronics and Communication, LNCT, Bhopal, India) and Piyush Jain(Director ITDTC, Bhopal, India) for sharing technical ideas in line with the proposed work.

## CONCLUSIONS

In this paper, the current work simulated the design of 9 transistors full adder, which is used low transistor count. With the help of 9 CMOS transistors, we have realized the circuit and compared proposed work with the previous, conventional adder circuits. The simulation results shows that this proposed adder has better performance than the previous proposed conventional circuits. This improvement is lots more time the available existing designs of various full addresses. XOR gate which is implemented by PMOS pass transistors has a less delay .The main aim of this paper is to design a high performance and low Power-Delay-Product.

## REFERENCES:

- [1] N. Weste and K. Eshraghian, "Principles of CMOS digital design," MA: Addison Wesley, pp.304–307.
- [2] S. Goel, M. A. Elgamel and M. A. Bayoumi, "Design Methodologies for High-Performance Noise-Tolerant XOR–XNOR Circuits," IEEE Transl. on Circuits and Systems—I: Regular Papers, vol. 53, No. 4, April 2006.
- [3] Q. Wu, P. Massoud, X. Yu, "Clock-Gating and Its Application to Low Power Design of Sequential Circuits," Proc. of the IEEE Custom Integrated Circuits Conference, pp. 425-435, 1997.
- [4] V. Gutnik, A. Chandrakasan, "Embedded Power Supply for Low Power DSP," IEEE Transl. on VLSI Systems, vol. 12, pp. 425-435, Dec. 1997.
- [5] AP. Chandrakasan, S. Sheng, and R.W. Brodersen, "Low-Power CMOS digital design," IEEE 1. Solid-State Circuit, vol. 27, pp. 473-483, Apr. 1992.
- [6] J.B Kuo and I.-H. Lou, "Low-Voltage CMOS VLSI Circuit," John Wiley & Sons, Inc., 1999.
- [7] S.M. kang, and L. Yusuf, "CMOS Digital integrated Circuit Analysis and Design," McGraw-Hill, 1999.
- [8] M. Zhang, I. Gu, and C. H. Chang, "A novel hybrid pass logic with static CMOS output drive full-adder cell," Proc. 36th IEEE Int Symp. Circuits and Systems, vol. Y, Bangkok, Thailand, May 2003, pp. 317-320.
- [9] J. F. Jiang, Z. G. Mao, W. F. He, Q. Wang, "A new full adder design for tree structured arithmetic circuits," Proc. 2nd Int Conf on (ICCET 2010), vol. 4, pp. 246-249, 16-18 April, 2010.
- [10] H. T. Bui, Y. Wang, and Y. Jiang, "Design and analysis of low-power 10-transistor full adders using XOR–XNOR gates," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 49, no. 1, pp. 25–30, Jan. 2002.
- [11] J.-F. Lin, Y.-T. Hwang, M.-H. Sheu and C.-C. Ho, "A novel high speed and energy efficient 10-transistor full adder design," IEEE Trans. Circuits Syst. I, vol. 54, no. 5, pp. 1050–1059, May 2007.
- [12] Jin-Fa Lin, Yin-Tsung Hwang and Ming-Hwa Sheu, "Low Power 10-Transistor Full Adder Design Based on Degenerate Pass Transistor Logic," 2012 IEEE.
- [13] Keivan Navi and Omid Kavehei, "Low-Power and High-Performance 1-Bit CMOS Full-Adder Cell", Journal of Computers, Vol. 3, no. 2, February 2008, PP 48-54