International Journal of Engineering Research and General Science Volume 3, Issue 2, March-April, 2015
ISSN 2091-2730

Multilevel Inverters for High Power Applications with Improved Power Quality Using Lesser Number of Switches

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Abstract - In this paper a new three- phase multi-level inverter topology is proposed. With the increasing requirements for high power at high power quality, such a converter is inevitable. The major advantages of the proposed topology are improved power quality and lesser number of switches. This leads to lesser complexity of the control circuitry, reduction in switching harmonics and reduction in the cost. Also here the number of voltage sources required is very less compared to conventional methods. This method gives THD of output voltage about 3%. Output of the proposed three phase 31-level inverter has been verified by MATLAB simulation results.

Keywords-H-bridge, Multi-level inverter, cascading, pwm technique, power quality, Total Harmonic Distortion (THD).

I.INTRODUCTION

Power converters are spreading technology for handling high power applications [5] in different field of growth and development of electric power utilization. They are widely being used in manufacturing, automotive traction, industrial applications etc. These power converters should possess high output power quality, high efficiency and low cost.

The conventional converter topologies were two level voltage source inverters [7] and current source inverters [6] with new high rating semiconductor devices. These high rating new semiconductor devices are very costly as well as difficult in fabrication and development. With technical advancements new topologies with traditional low rating semiconductor devices [4] are introduced. These topologies are known as multi-level converters. Now multi-level converters are being used with higher and higher levels like – 3-levels, 4-levels etc. up to even 13-level have been reached. They are able to handle about 30 MW with high voltage output and cheaper semiconductor devices. The most noticeable drawbacks of such converters are complex circuits for controlling the switching devices and the losses due to larger number of switching devices. This leads to introduction of harmonics into the supply as well as load.

The proposed method is a three phase 31-level inverter with reduced number of switches. Hence the complex circuitry and switching losses are reduced. Also being of higher level, they possess advantages like high power quality, reduction in harmonics and lesser electromagnetic interference [14].

In this paper the next section will present the multilevel converter background and their features, characteristics and drawbacks. The third section will deal with the proposed topology of three phase 31-level inverter. The fourth and fifth sections will deal with simulation and simulation result analysis respectively. And finally with the future scope the paper is concluded.

II. MULTI-LEVEL INVERTER BACKGROUND

There are so many methods for combining semiconductor devices to form multilevel topologies. Some of them are cascaded H-bridge multilevel inverter [9], neutral clamped multilevel inverter [8], flying capacitor type inverter [11] and most recent cross switched multilevel inverter with reduced number of switches [10].

A simple 3-phase, 3-level cascaded inverter topology is discussed here. It consists of 36 switching devices and 9 dc sources. During switching of these switches there will be a high switching loss which may reduce the overall efficiency of the system as well as introduce harmonics into the supply system.

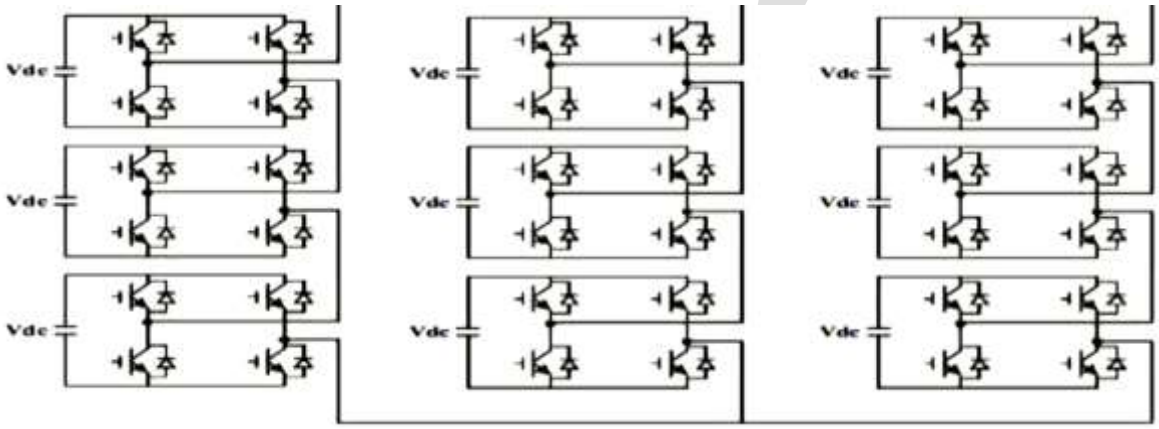

Fig.1 3-phase 3-level cascaded H-bridge inverter

Another advanced topology, cross switched multi-level inverter [10] is shown in the fig. 2 which consists of 12 switches and 5 dc source for one phase of the 3-phase 11-level inverter. In this method the power losses are lesser compared to the previous topologies, but not as low as in the proposed topology.

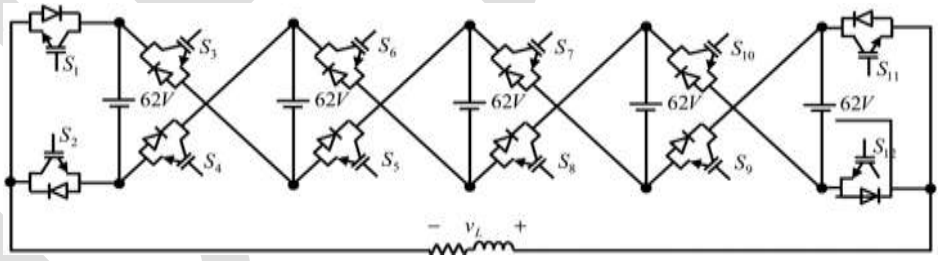

Fig. 2 One leg of 3-phase 11-level cross switched inverter

Figure 3 and figure 4 show two more multilevel inverter topologies. Here, even though the numbers of switches are less compared to the conventional methods, the number of switches is much greater in comparison with the proposed topology. The ladder type multi-level inverter [15] in figure 3 consists of "n", number of switching devices for n-level output. In figure 4, an n-level staircase type inverter topology requires 2n-2 number of switching devices

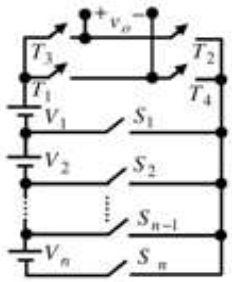

Fig. 3 Ladder Topology

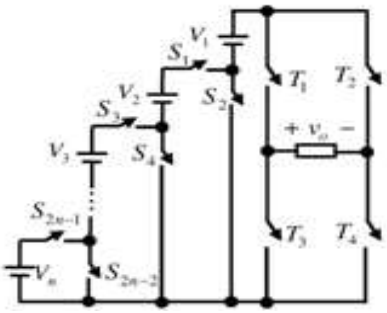

Fig. 4 Staircase topology

III. PROPOSED TOPOLOGY

The basic building block of the proposed topology is derived from H-bridge. The proposed method is a modified H-bridge topology [3]. Compared to the conventional H-bridge cascaded multi-level inverter topology [9], the modified H-bridge requires lesser number of switches. Hence the control circuitry becomes less complicated and cheaper. Here a 3-phase 31-level modified H-bridge, derived from a 7-level inverter is presented [1]. As the number of level increases the output wave form becomes more and more smooth. And hence the harmonics introduced in the supply systems and the loads are reduced [12]. This leads to improved power quality and power factor. One phase of the 3-phase proposed inverter is given in fig. 5. It consists of only 10 switches and 4 dc sources.

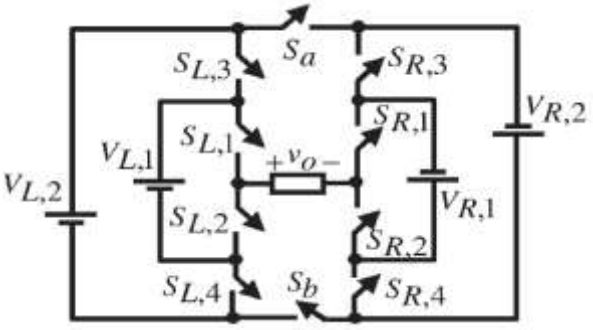

Fig.5. One phase of the 3-phase 31-level inverter

Here four switches and two dc sources are added to the conventional, two level H-bridge inverter to get the 31-level modified H-bridge inverter. In this method peak value of the output voltage waveform is obtained as VL2+VR2. Here VL2 and VR2 are source voltages. The total cost of the proposed method can be reduced because the magnitudes of the voltage sources required are low. As seen from figure 5 it is clear that simultaneous turn ON of SL1 and SL2 or SR1 and SR2 will lead to short circuiting of the dc sources. So this should be taken care of while selecting the switching sequence. Similarly simultaneous turn ON of Sa and Sb should be avoided. PWM scheme [2] is used for switching. Table 1 shows the excitation table of the switches and the corresponding output voltage levels. In table.1, the notation '1' stands for ON and '0' stands for OFF condition of the switch.

TABLE I

Switching sequences and corresponding output voltage levels of the proposed 31-level inverter phase-R

No	SL1	SL2	SL3	SL4	SR1	SR2	SR3	SR4	Sa	Sb	Vo
1	1	0	1	0	1	0	1	0	1	0	0
2	1	0	0	1	0	1	0	1	0	1	Vdc
3	0	1	0	1	1	0	0	1	0	1	2Vdc
4	1	0	0	1	1	0	0	1	0	1	3Vdc
5	0	1	1	0	0	1	0	1	0	1	4Vdc
6	1	0	1	0	0	1	0	1	0	1	5Vdc
7	0	1	1	0	1	0	0	1	0	1	6Vdc
8	1	0	1	0	1	0	0	1	0	1	7Vdc
9	0	1	0	1	0	1	1	0	0	1	8Vdc
10	1	0	0	1	0	1	1	0	0	1	9Vdc
11	0	1	0	1	1	0	1	0	0	1	10Vdc
12	1	0	0	1	1	0	1	0	0	1	11Vdc
13	0	1	1	0	0	1	1	0	0	1	12Vdc
14	1	0	1	0	0	1	1	0	0	1	13Vdc
15	0	1	1	0	1	0	1	0	0	1	14Vdc
16	1	0	1	0	1	0	1	0	0	1	15Vdc
17	0	1	1	0	1	0	1	0	1	0	-Vdc
18	1	0	1	0	0	1	1	0	1	0	-2Vdc
19	0	1	1	0	0	1	1	0	1	0	-3Vdc
20	1	0	0	1	1	0	1	0	1	0	-4Vdc
21	0	1	0	1	1	0	1	0	1	0	5Vdc
22	1	0	0	1	0	1	1	0	1	0	-6Vdc
23	0	1	0	1	0	1	1	0	1	0	-7Vdc
24	1	0	1	0	1	0	0	1	1	0	-8Vdc
25	0	1	1	0	1	0	0	1	1	0	-9Vdc
26	1	0	1	0	0	1	0	1	1	0	-10Vdc
27	0	1	1	0	0	1	0	1	1	0	-11Vdc
28	1	0	0	1	1	0	0	1	1	0	-12Vdc
29	0	1	0	1	1	0	0	1	1	0	-13Vdc
30	1	0	0	1	0	1	0	1	1	0	-14Vdc
31	0	1	0	1	0	1	0	1	1	0	-15Vdc

In the proposed method dc source VL1 is designed for Vdc, VL2 for 5Vdc, VR1 for 2Vdc and VR2 is designed for 10Vdc as per the general topology for N-level modified H-bridge [1]. According to the general topology for N-level modified H-bridge**.**

$$\text{Number of sources} = 2n \quad (1)$$

$$\text{Number of output voltage levels } N = 2^{(2n+1)} - 1 \quad (2)$$

$$\text{Number of switches} = 4n + 2 \quad (3)$$

$$\text{Voltage source } VL1 = Vdc \quad (4)$$

Voltage source VL2 = 5Vdc (5)

Voltage source VR1 = 2Vdc (6)

Voltage source VR3 = 10Vdc (7)

Where 'n' is the number of sources in the left half of the circuit diagram and Vdc is the voltage level of first step from the zero level.

IV. SIMULATION DIAGRAM OF 3-PHASE 31-LEVEL INVERTER

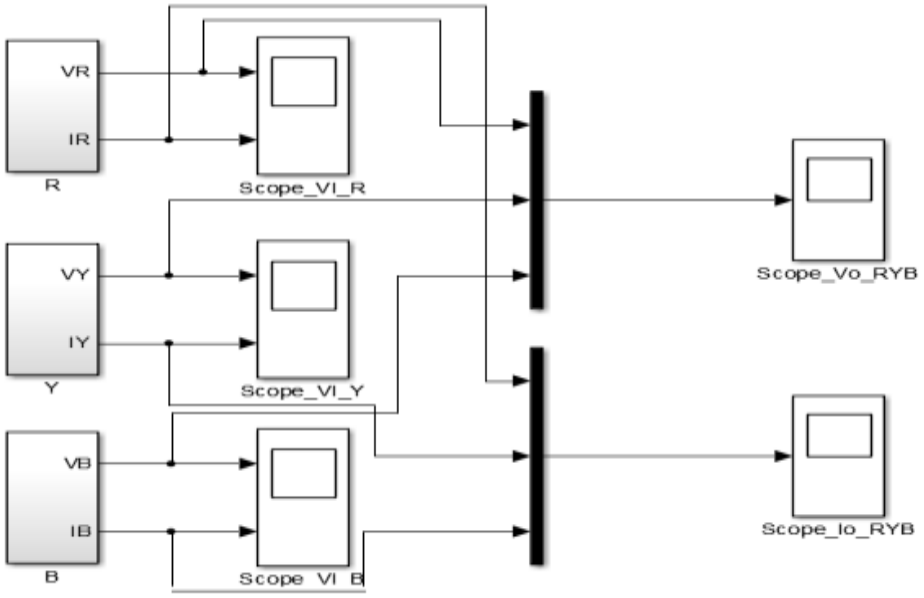

Fig.6. Simulation diagram of 3-phase 31-level inverter

In figure 6 there are three sub systems R,Y and B. All these subsystems are of the basic 31-level modified H-bridge. Here for simulation Vdc is selected as 15V, so that each step of the out put voltage will vary with 15V. During simulation, for each phase the PWM [13] reference sinusoidal waveform taken is 120^0 displaced with each other. So that the out put waveform of each phase will be displaced from each other by120^0 . Through a multiplexer the three waveforms are brought out with respected to same axis.

V. SIMULATION RESULTS

Figure 7 shows the MATLAB simulation out put voltage waveforms with 15 positive voltage levels,15 negative voltage levels and 1 zero voltage level, which constitutes a total of 31 steps in each phase. Here we can see that the waveforms are having less distortion from ideal sine wave. And the current waveforms in Fig.8are more closer to a pure sine wave. This indicates least introduction of harmonics into the supply. THD for out put currents are shown in Fig.9.and that for voltages are shown in Fig.10.

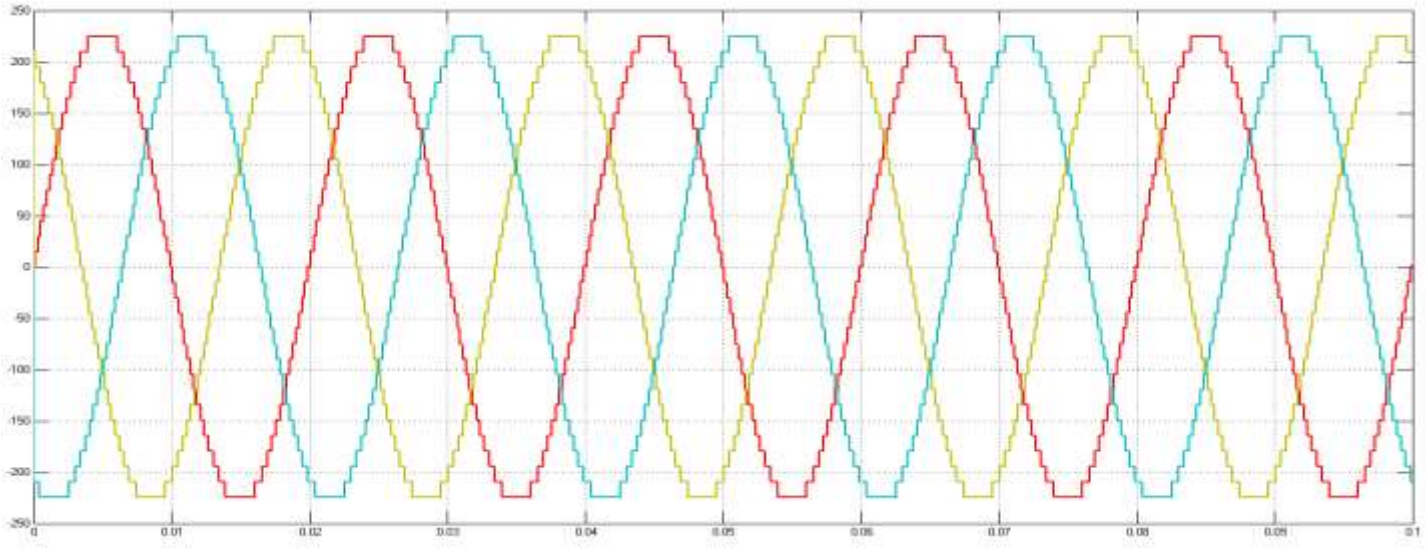

Fig.7. Output voltage waveforms

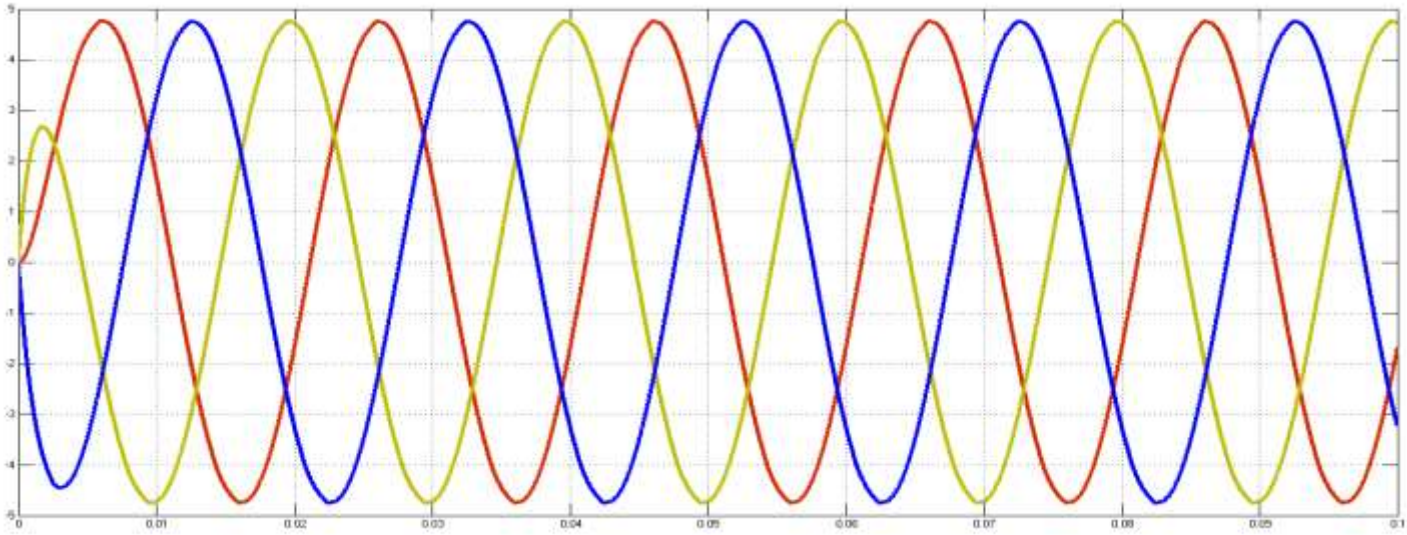

Fig.8. Output current waveforms

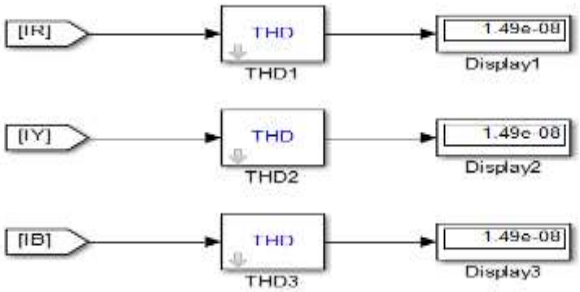

Fig.9. THD values for current waveforms.

THD values for current waveforms are very very small ,which indicates that the harmonics injected into the supply will be very less.Similarly the THD for voltages of different phases are nearly 3% only. This indicates that the harmonics introduced into the load

will be very low. From the harmonic specrum of figure 10.a, it is clear that voltage magnitude for fundamental frequency is 229V, where as that for higher frequencies are very small of the order of 0.3V and below. Also it is observed that the even harmonics are almost absent, which indicates the symmetry of the sinusoidal out put waveform. This will give confirmation of the advantage of least THD value of the proposed method.

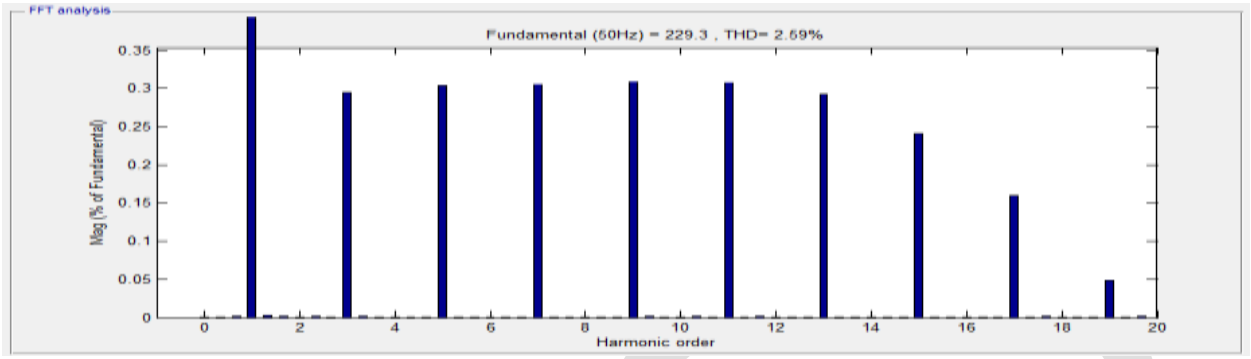

Fig.10a. Output voltage harmonic spectrum for R-phase.

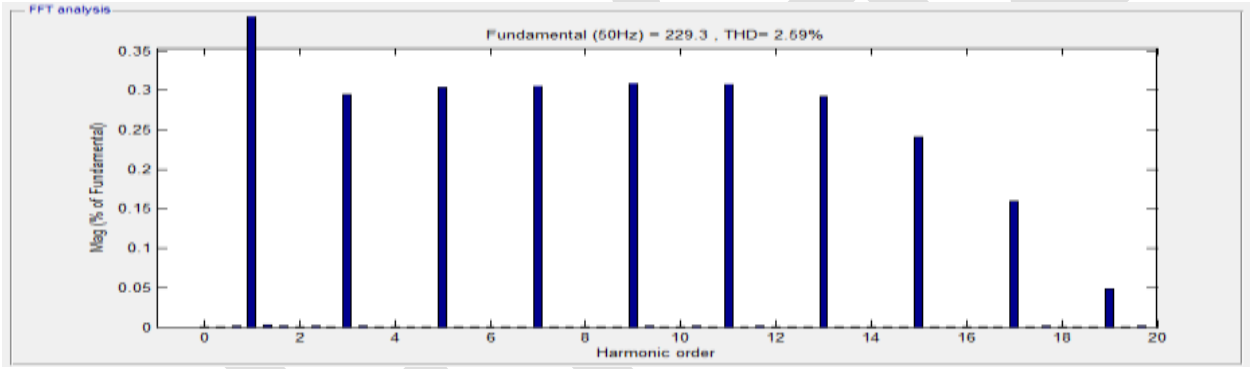

Fig.10b Output voltage harmonic spectrum for Y-phase.

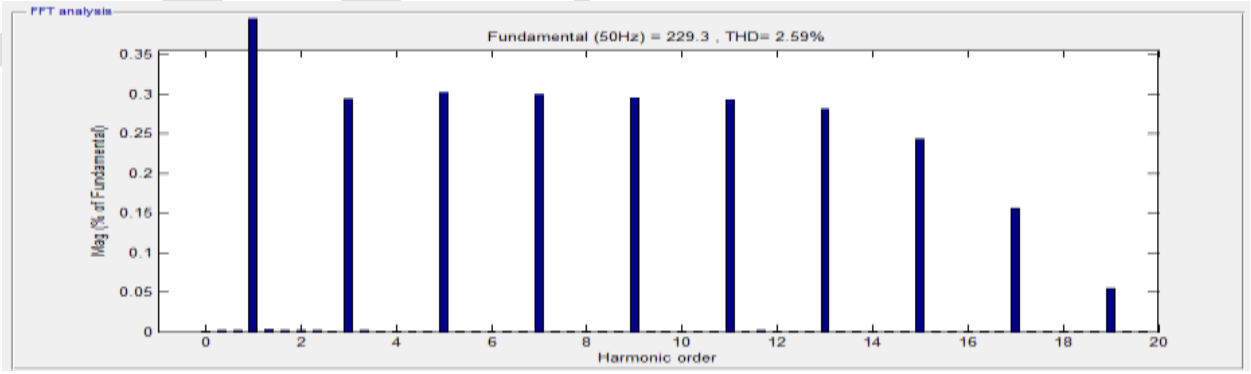

Fig.10c Output voltage harmonic spectrum for B-phase.

VI. CONCLUSION

In this paper the inverter topology for generating 31-level output voltage waveform has been proposed with the added advantage of lesser number of switches, which leads to reduced harmonics, improved efficiency and improved power factor. More over the control

circuitry became less complicated as the number of switches became lesser. Also the design steps are less complex,as there is a general topology for the proposed method. Based on the generalised method higher levels of multilevel inverters can be designed in future. In literature survey the proposed topology was compared with other topologies which had highligted the advantages of proposed method over the conventional methods. The performance accuracy of the proposed three phase 31-level inverter circuit had been verified using MATLAB simulation.

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