International Journal of Engineering Research and General Science Volume 3, Issue 2, March-April, 2015
ISSN 2091-2730

Design of DRAM with Coupled Sense Amplifier for Low Power Applications

T.Boobalan, Anila Ramachandran,V.Kavitha, S.Rathimeena
Assistant professor, ECE Department,Anna university,Tamilnadu,India.
ME-VLSI design students,Anna university,Tamilnadu,India.
Email:anila.ramachandran@yahoo.com

***Abstract*—**For more than four decades the simple structure of the dynamic RAM cell and continuous improvement in lithography and dry etching technology has made DRAM to grow exponentially in a large scale integration and has decreased the minimum feature size in memory chips. The 2010 ITRS roadmap reports that the minimum feature size of DRAM will be 20 nm in 2017 and 10 nm in 2023. Sense amplifier which is a part of DRAM circuit consumes a power of 0.422µw.But circuit level modifications in sense amplifier circuitry will help to achieve a power reduction of 5-10%.

Keywords-DRAM, Feature size, Large scale integration, memory chips, lithography, etching, circuit level techniques

I.INTRODUCTION

Very-large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip.VLSI began in the 1970s when complex semiconductor and various communication techn-ologies were being developed[1]. The microprocessor is a VLSI device. Before the introduction of VLSI technology most ICs had a limited set of functions they could perform.

VLSI lets IC makers add all of these into one chip. The increasing speed and complexity of today's designs implies a significant increase in the power consumption of VLSI chips. To meet this challenge researchers have developed many different design techniques to reduce power. The complexity of today's ICs with over 100 million transistors, clocked at over 1 GHz means manual power optimization would be hopelessly slow and all too likely to contain errors. One of the key features that led to the success of complementary metal-oxide semiconductor or CMOS technology was its intrinsic low-power consumption. This meant that circuit designers and electronic design automation (EDA) tools could afford to concentrate on maximizing circuit performance and minimizing circuit area. Another interesting feature of CMOS technology is its nice scaling properties, which has permitted a steady decrease in the feature size (Moore's law) allowing for more and more complex systems on a single chip, and working at higher clock frequencies.

Dynamic Random Access Memory (DRAM) devices are used in a wide range of electronics applications. Although they are produced in many sizes and sold in a variety of packages, their overall operation is essentially the same. DRAMs are designed for the sole purpose of storing data. The only valid operations on a memory device are reading the data stored in the device, writing (or storing) data in the device, and refreshing the data periodically. To improve efficiency and speed, a number of methods for reading and writing the memory have been developed. DRAMs evolved from the earliest 1-kilobit generation to the recent 1-gigabit (Gb) generation through advances in both semiconductor process and circuit design technology. Tremendous advances in process technology have dramatically reduced feature size, permitting ever higher levels of integration. These increases in integration have been accompanied by major improvements in component yield to ensure that overall process solutions remain cost effective and competitive. Technology improvements, however, are not limited to semiconductor processing. Many of the advances in process technology have been accompanied or enabled by advances in circuit design technology. In most cases, advances in one have enabled advances in the other. A DRAM circuit consists of row decoder, column decoder, input and output buffers, sense amplifier and memory array.

This paper is organized as follows. Section II introduces the simplified DRAM architecture. Section III explains simulation results obtained by using Tanner13.0.Finally Section IV concludes the paper.

II. BACKGROUND

A.DRAM OVERVIEW

Figure 1 shows a circuit diagram of the basic one transistor one capacitor (1T1C) cell structure used in modern DRAM devices as the basic storage unit. In the structure illustrated in figure 1 when the access transistor is turned on
by applying a voltage on the gate of the access transistor a voltage representing the data value may be placed onto the bit line and used to charge the storage capacitor. The storage capacitor then retains the stored charge for a limited period of time after the voltage on the

word line is removed and the access transistor is turned off. However due to leakage currents through the access transistor the electrical charge stored in the storage capacitor gradually dissipates. As a result before the stored charge decays to indistinguishable values the data stored in DRAM cells must be periodically read-out and written back in a process known as refresh. Otherwise the stored electrical charge will gradually leak away and the value stored in the capacitor will no longer be resolvable after some time.

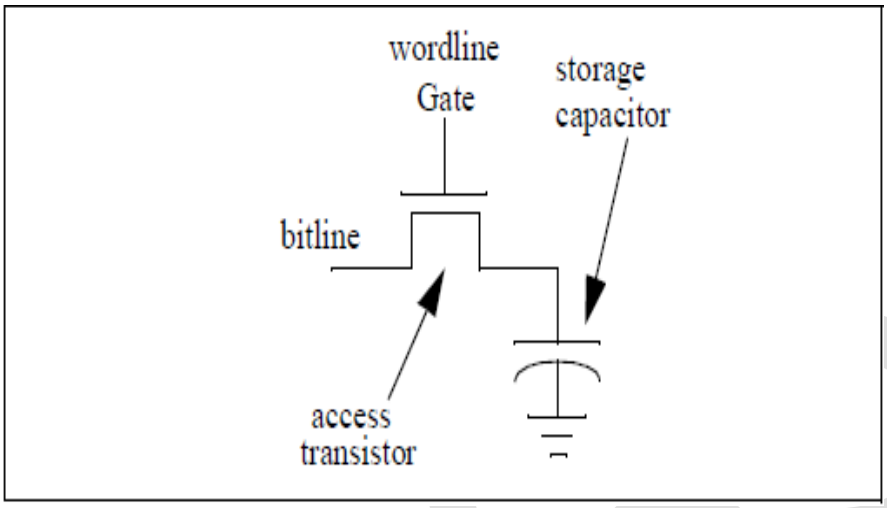


Figure 1. Basic 1T1C DRAM Cell structure

B.DRAM ARCHITECTURE

DRAM chips are large, rectangular arrays of memory cells with support logic that is used for reading and writing data in the arrays, and refresh circuitry to maintain the integrity of stored data. The gates of the DRAM cells are tied to the row decoder and the bit-line pairs are connected to the sense amplifier as shown in figure2 [2].The bit-line pairs are connected in parallel to the sense amplifier to reduce the bit-line coupling noise. This array architecture is called the folded bit-line array. This array usually has a small feature size of $8F^2$ (F: feature size) and has proven to be the most reliable design. Another array scheme called the open bit-line array has smaller feature sizes ($6F^2$or $4F^2$) than the folded bit line[3]. This scheme has high density and cell efficiency, and is also used when reducing the number of word lines to ease the impact of a bit-line interference noise on DRAM scaling. But there is no difference in operating the DRAM cells between the folded bit line and open bit-line architecture[4]. Therefore the folded bit-line array architecture is used here for better understanding. With the down-scaling trend of the minimum feature size and power, many problems (capacitor/bit-line/word-line bridges, coupling noise, P-MOS/N-MOS ratio, leakage current and so on) need to be considered. With the short length of the word-line channel, the sub threshold leakage current will increase more. To prevent this sub threshold leakage-current problem, channel doping should be increased in order to maintain adequate control of short-channel effects. However, junction leakage current due to band-to-band tunneling and gate-induced drain leakage current may increase as a result of high channel doping. The variability of the threshold voltage can also increase due to defects resulting from manufacturing aberrations [5]–[9].

Memory Arrays

Memory arrays are arranged in rows and columns of memory cells called word lines and bit lines respectively. Each memory cell has a unique location or address defined by the intersection of a row and a column.

Memory Cells

A DRAM memory cell is a capacitor that is charged to produce a 1 or a 0. Over the years several different structures have been used to create the memory cells on a chip. In today's technologies, trenches filled with dielectric material are used to create the capacitive storage element of the memory cell.

Support Circuitry

The memory chip's support circuitry allows the user to read the data stored in the memory's cells, write to the memory cells, and refresh memory cells. This circuitry generally includes:-

- Sense amplifiers to amplify the signal or charge detected on a memory cell
- Address logic to select rows and columns
- Row Address Select (RAS) and Column address Select (CAS) logic to latch and resolve row and column addresses and to initiate and terminate read and write operations.

The gates of the DRAM cells are tied to the row decoder and the bit-line pairs are connected to the sense amplifier as shown in figure2. A sense amplifier is composed of a pair of cross-connected inverters between the bit lines[10].

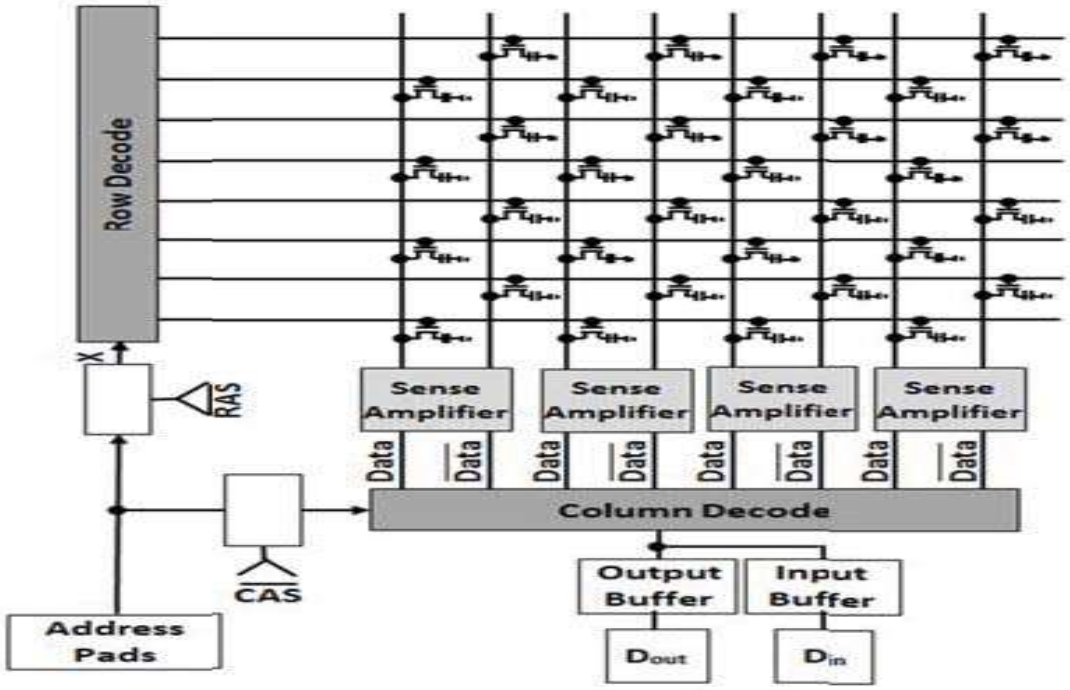


Figure 2.Simplified DRAM diagram

III.SIMULATION RESULTS

Today's computers CPUs and cell phone make use of CMOS technology due to several key advantages. CMOS offer low power dissipation, relatively high speed and high noise margin. So here we are designing row decoder, sense amplifier, column decoder and thus the DRAM circuit and simulation is done using Tanner tool.

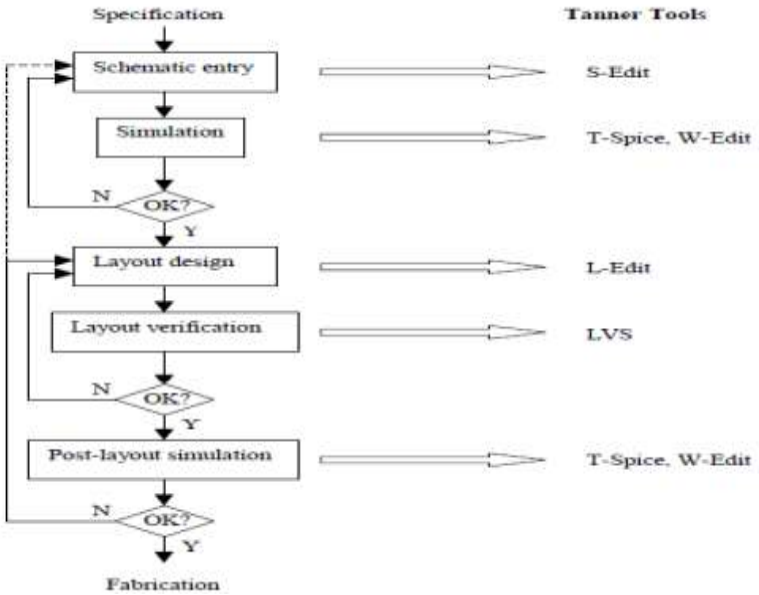


Figure 3.Steps of methodology and implementation plan for Tanner13.0

A.ROW DECODER

Decoders address a specific cell in the memory cell array[11]. Row decoders are used to select a particular row of cells in the memory array.Decoders can be implemented using simple logic gates.In the DRAM circuit (fig.2.) gates of transistors are tied to the row decoder.Fig.4.shows row decoder circuit schematic diagram using nand,nor (universal gates) and not gates in s-edit.

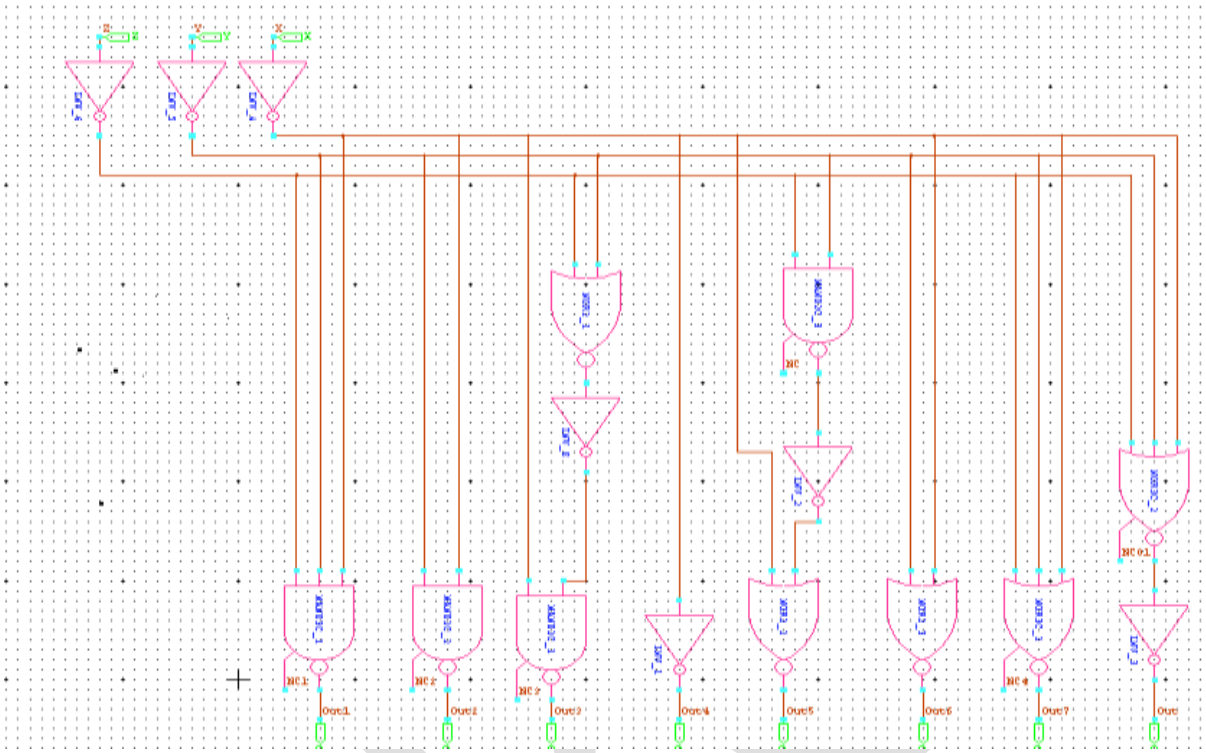
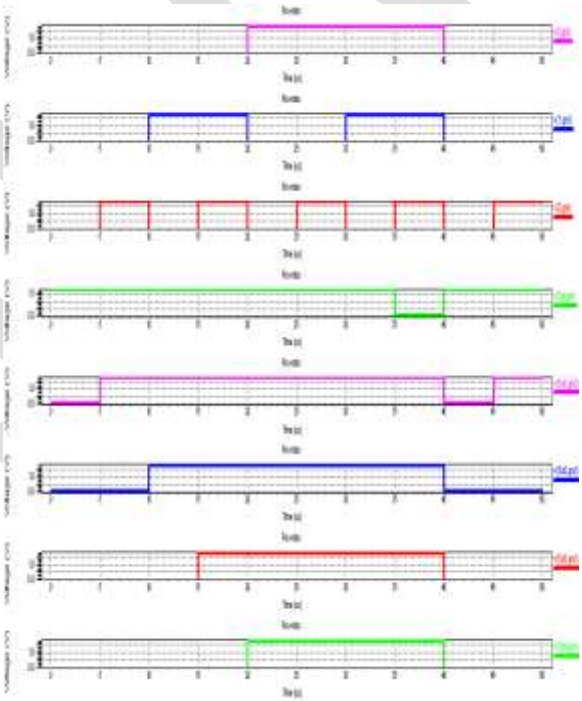


Figure 4.Row decoder circuit schematic



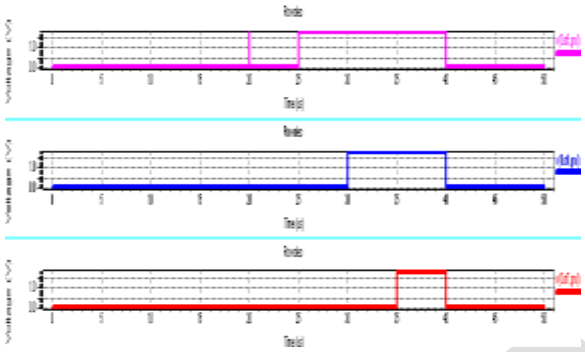


Figure 5. Input and output waveforms of row decoder in w-edit

Row decoder circuit schematic (fig.4) is designed in s-edit and simulated to obtain output waveforms which can be viewed in w-edit. Here we designed a 3 to 8 decoder circuit. So it has 8 decoded outputs. When address and RAS (Row Access Signal) are loaded a specific row of cells will get selected using this row decoder. When we simulate the row decoder circuit output waveforms are obtained as shown in figure 5.

B.SENSE AMPLIFIER

Sense amplifier is not only an amplifier but a positive feedback device that quickly pushes the readout voltage to 1 or 0. The gates of the DRAM cells are tied to the row decoder and the bit-line pairs are connected to the sense amplifier. A sense amplifier is composed of a pair of cross-connected inverters between the bit lines. When the address and Row Access Signal (RAS) instruction are loaded to the device each row of the selected cells is active. In this operation, the data stored in the cells of the selected row address are amplified and stored again by the sense amplifiers. The bit-line pairs are connected in parallel to the sense amplifier.

The sense amplifier circuit (figure 6) schematic is designed in s-edit and simulated to obtain output waveforms in w-edit which is shown in figure 8.The symbol for sense amplifier is shown in figure 7.Sense amplifier will work properly when enable line is high. But this high enable line turn on all four sense amplifiers since we use a single enable line for all sense amplifiers. So this leads to higher power consumption.

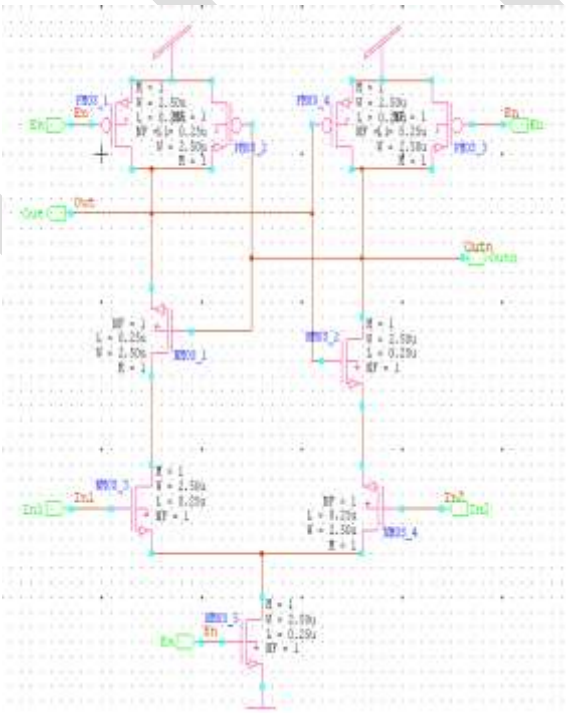


Figure 6.Sense amplifier circuit schematic in s-edit

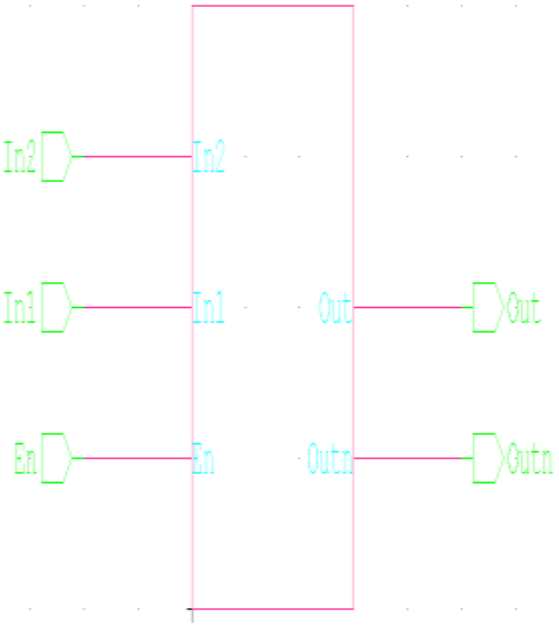


Figure 7.Symbol for sense amplifier

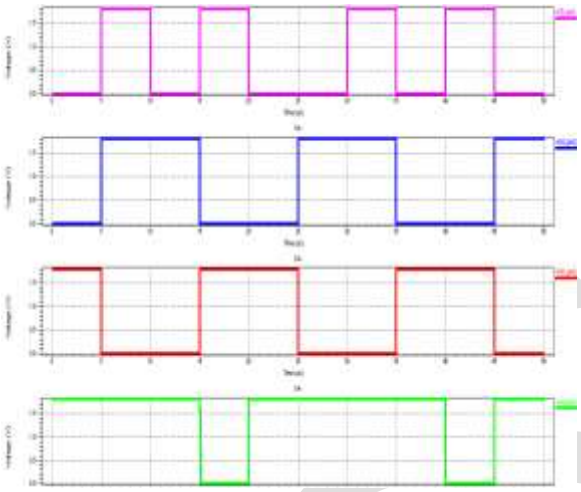


Figure 8.Input and output waveforms of sense amplifier circuit

C.COUPLED SENSE AMPLIFIER

We can employ coupling technique in sense amplifier to achieve power reduction. The normal sense amplifier consumes a power of 0.422 micro watts. Coupled sense amplifier requires only 0.01628 micro watts. So we can achieve approximately 5% power reduction by this technique. Figure 9 shows coupled sense amplifier. Figure 10 shows its output and input waveforms. Sense amplifier is connected to column decoder. So there is a chance to occur coupling fault in the transistors. This modified sense amplifier will reduce the effect of coupling fault.

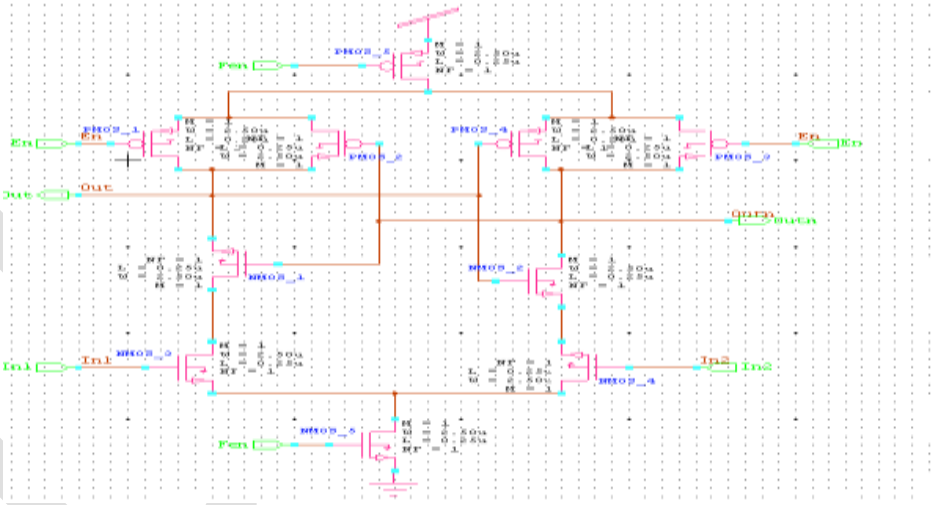


Figure 9. Coupled sense amplifier

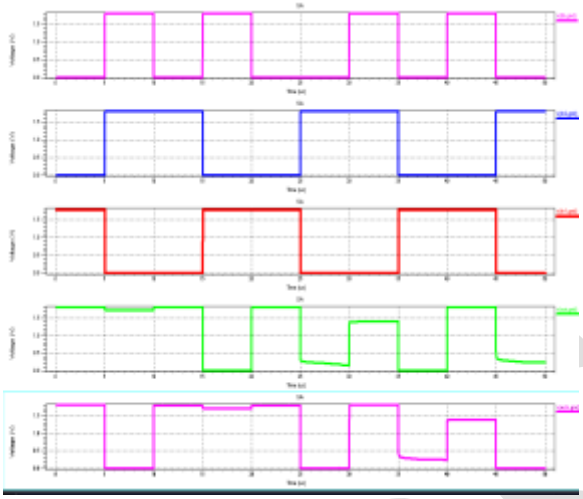


Figure 10. Input and output waveforms of coupled sense amplifier

D.DRAM CIRCUIT

Using the row decoder circuit and sense amplifier we can design the final DRAM circuit along with column decoder. For the proper working of DRAM circuit enable line of sense amplifier must be high. DRAM circuit with coupled sense amplifier and its waveforms are shown below.

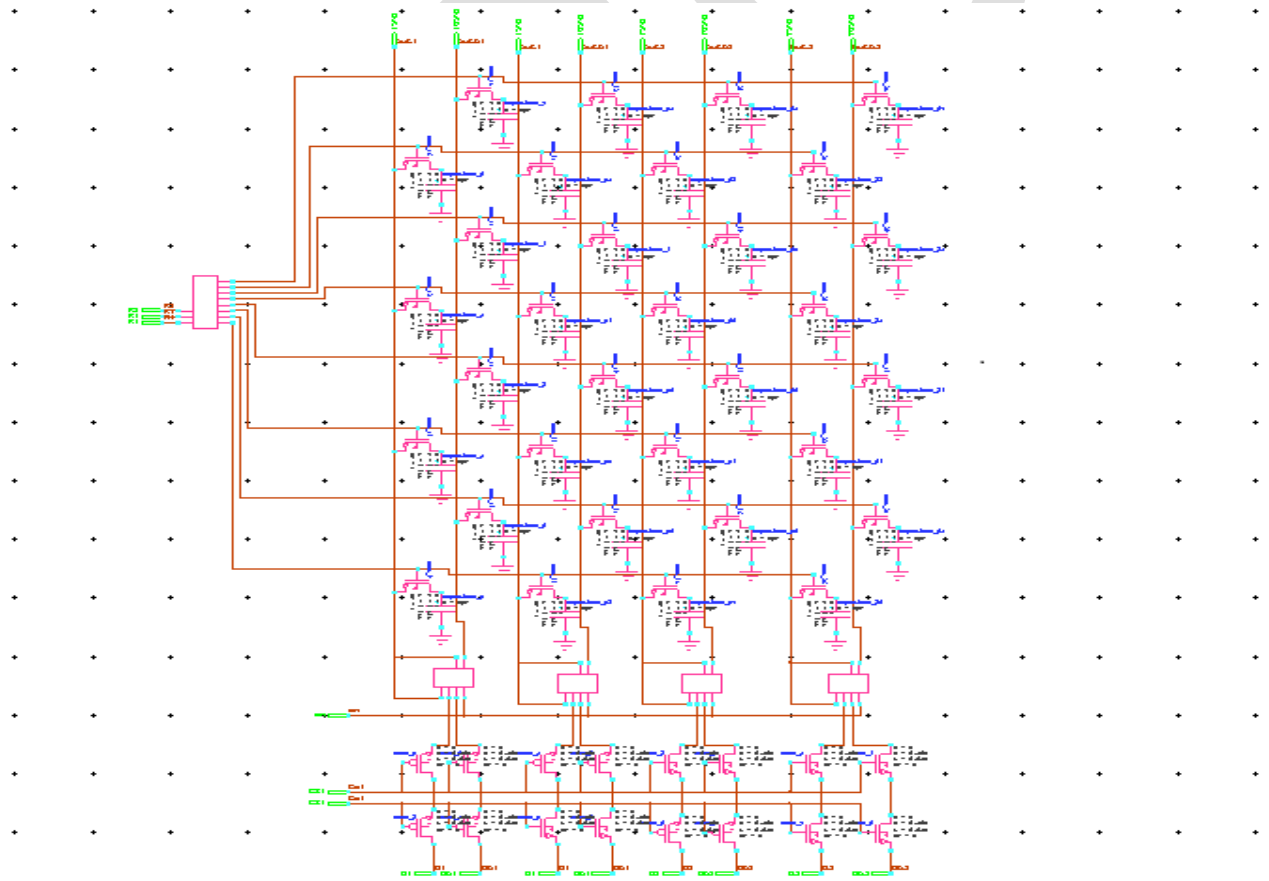


Figure 11. DRAM circuit with coupled sense amplifier

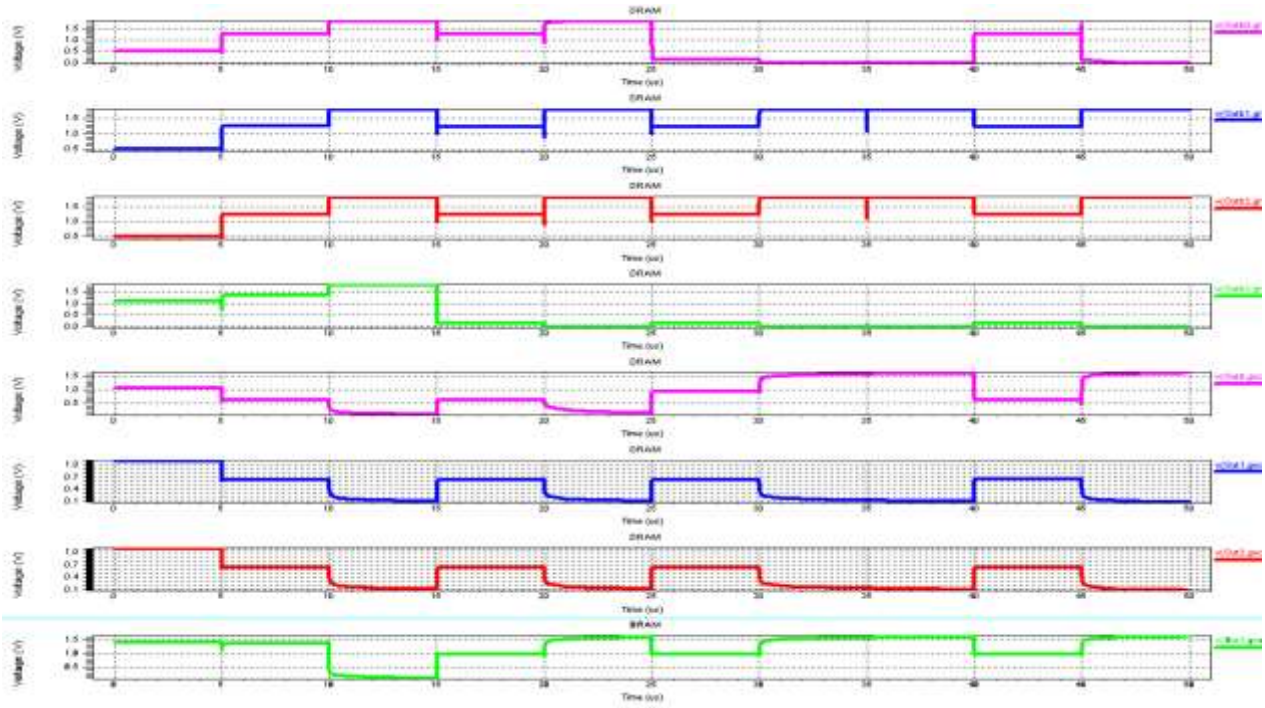


Figure 12. Output waveforms of DRAM circuit with coupled sense amplifier

E.COMPARISON OF PARAMETERS

For normal sense amplifier and coupled sense amplifier parameters such as power, static current, power delay product and energy delay product are calculated and shown in table 1.

Table 1. Comparison of parameters for normal and coupled sense amplifiers

PARAMETERS	NORMAL SENSE AMPLIFIER	COUPLED SENSE AMPLIFIER
Average power	0.422 µw	0.01628 µw
Static power	431 µw	333 µw
Static current	239.4 µA	185 µA
Power delay product	6.465 nws	4.995 nws
Energy delay product	0.0969 pws²	0.0749 pws²

For DRAM circuit with normal sense amplifier and DRAM circuit with coupled sense amplifier parameters such as static power, static current, power delay product and energy delay product are calculated and listed in table 2.

Table 2. Comparison of parameters for DRAM with normal sense amplifier and DRAM with coupled sense amplifier

PARAMETERS	DRAM with normal sense amplifier	DRAM with coupled sense amplifier
Static power	14.53 mw	12.1 mw
Static current	8.072 mA	6.72 mA
Power delay product	0.5812 mws	0.484 mws
Energy delay product	23.25 pws^2	19.36 pws^2

IV. CONCLUSION

DRAM circuit consists of row decoder, column decoder, memory array, input and output buffers and sense amplifier. In a DRAM circuit more than 80% of power is consumed by sense amplifier. DRAM circuit designed in s-edit consumes a static power of 14.53 milli watts. Circuit level modification in sense amplifier circuitry will help to achieve a power reduction of 5-10%.This modified sense amplifier also help to reduce coupling faults occurring in DRAM circuits.

REFERENCES:

[1]International Technology Roadmap for Semiconductors 2010 [online]
[2]*Memory*,Integr.CircuitEng. Corporation, Phoenix, AZ, USA, 1997
[3] D. Takashima, S. Watanabe, H. Nakano, Y. Oowaki, and K. Ohuchi, "Open/folded bit-line arrangement for ultra-high-density DRAM's,"*Proc. IEEE J. Solid, State Circuits*, vol. 29, no. 4, pp. 539–542,Apr. 1994.

[4] T. Sekiguchi, K. Itoh, T. Takahashi, M. Sugaya,H.Fujisawa,M.Nakamura,K.Kajigaya, and K. Kimura, "A low impe-dance open-bit line array for multi gigabit DRAM," *Proc. IEEE J. Solid, State Circuits*, vol. 37,no. 4, pp. 487–498, Apr. 2002.

[5] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanism and leakage reduction techniques in deep sub micrometer CMOS circuits," *Proc. IEEE*, vol. 9, no. 2, pp. 305–327,Feb. 2003.
[6] N. Yamauchi, K. Kato, and T. Wada, "Channel edge doping (CED)
method for reducing the short-channel effect," *Proc. IEEE Electron Device Lett.*, vol. 4, no. 11, pp. 406–408, Nov. 1983.
[7] M. F. Zakaria, Z. A. Kassim, M. P.-L. Ooi, and S. Demidenko, "Reducing burn-in time through high-voltage stress test and Weibull statistical analysis," *Proc. IEEE Design Test Comput.*, vol. 23, no. 2, pp. 88–98, Mar.-Apr. 2006.
[8] M. Meterelliyoz, H. Mahmoodi,and K. Roy, "A leakage control system for thermal stability during burn-in test," in *Proc. Int. Test Conf.*,Nov. 2005, pp. 991–1000.
[9] C. Minki, S. Nikhil, R. Arijit, and M. Saibal, "Optimization of burn in test for many-core processors through adaptive spatiotemporal power migration," in *Proc. Int. Test Conf.*, Nov. 2010, pp. 1–9.
[10]Interleaving Test Algorithm for Subthreshold Leakage-Current Defects in
DRAM Considering the Equal Bit Line Stress Hyoyoung Shin,Youngkyu Park, Gihwa Lee, Jungsik Park, and Sungho Kang, *Member, IEEE*, IEEE transactions on very large scale integration (vlsi) systems, vol. 22, no. 4, april 2014

[11]Vineet Tiwari, Sanjeev Ranjan,Vivek Baghel,"Design of 8 bit current steering DAC",International Journal of Engineering Research and Technology(IJERT) ,vol 1.issue 5,july 2012